



Welcome to [E-XFL.COM](#)

**[Embedded - Microcontrollers - Application Specific](#): Tailored Solutions for Precision and Performance**

**[Embedded - Microcontrollers - Application Specific](#)** represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

**What Are [Embedded - Microcontrollers - Application Specific](#)?**

Application specific microcontrollers are engineered to

#### Details

Product Status	Obsolete
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (8kB)
Controller Series	CY8C20xx6
RAM Size	1K x 8
Interface	I <sup>2</sup> C, SPI
Number of I/O	20
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	24-UFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20336-24lqxit">https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20336-24lqxit</a>

## PSoC® Functional Overview

The PSoC family consists of on-chip Controller devices. These devices are designed to replace multiple traditional MCU-based components with one, low cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the [Logic Block Diagram on page 2](#), is comprised of three main areas: the Core, the CapSense Analog System, and the System Resources (including a full speed USB port). A common, versatile bus allows connection between I/O and the analog system. Each CY8C20x36/46/66/96 PSoC Device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 36 general purpose IO (GPIO) are also included. The GPIO provides access to the MCU and analog mux.

### PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO (internal main oscillator) and ILO (internal low speed oscillator). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-MIPS, 8-bit Harvard architecture microprocessor.

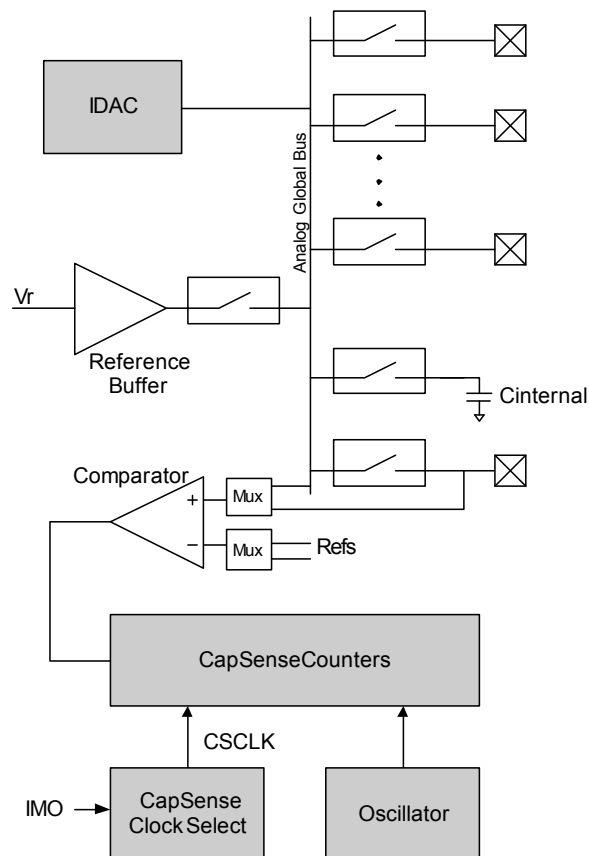
System Resources provide additional capability, such as configurable USB and I2C slave/SPI master-slave communication interface, three 16-bit programmable timers, and various system resets supported by the M8C.

The Analog System is composed of the CapSense PSoC block and an internal 1.2V analog reference, which together support capacitive sensing of up to 36 inputs.

### CapSense Analog System

The Analog System contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins are completed quickly and easily across multiple ports.

**Figure 1. Analog System Block Diagram**



### Analog Multiplexer System

The Analog Mux Bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces, such as sliders and touchpads.
- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

When designing capacitive sensing applications, refer to the latest signal-to-noise signal level requirements Application Notes, which can be found under <http://www.cypress.com> > Documentation > Application Notes. In general, and unless otherwise noted in the relevant Application Notes, the minimum signal-to-noise ratio (SNR) for CapSense applications is 5:1.

## Additional System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The merits of each system resource are listed here:

- The I2C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I2C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power-On-Reset) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO.
- Standard Cypress PSoC IDE tools are available for debugging the CY8C20x36/46/66/96 family of parts. However, the additional trace length and a minimal ground plane in the Flex-Pod can create noise problems that make it difficult to debug the design. A custom bonded On-Chip Debug (OCD) device is available in an 48-pin QFN package. The OCD device is recommended for debugging designs that have high current and/or high analog accuracy requirements. The QFN package is compact and is connected to the ICE through a high density connector.

## Getting Started

The quickest way to understand PSoC silicon is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the PSoC® Programmable System-on-Chip™ Technical Reference Manual for CY8C20x36/46/66/96 PSoC Devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at [www.cypress.com/psoc](http://www.cypress.com/psoc).

## Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located here: [www.cypress.com/psoc](http://www.cypress.com/psoc). Select Application Notes under the Documentation tab.

## Development Kits

PSoC Development Kits are available online from Cypress at [www.cypress.com/shop](http://www.cypress.com/shop) and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

## Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at [www.cypress.com/training](http://www.cypress.com/training). The training covers a wide variety of topics and skill levels to assist you in your designs.

## CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to [www.cypress.com/cypros](http://www.cypress.com/cypros).

## Solutions Library

Visit our growing library of solution focused designs at [www.cypress.com/solutions](http://www.cypress.com/solutions). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

## Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at [www.cypress.com/support](http://www.cypress.com/support). If you cannot find an answer to your question, call technical support at 1-800-541-4736.

## Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows XP and Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

### PSoC Designer Software Subsystems

#### *System-Level View*

The system-level view is a drag-and-drop visual embedded system design environment based on PSoC Express. In this view you solve design problems the same way you might think about the system. Select input and output devices based upon system requirements. Add a communication interface and define the interface to the system (registers). Define when and how an output device changes state based upon any/all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC devices that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

#### *Chip-Level View*

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer 4.x. You choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. You configure the user modules for your chosen application and connect them to each other and to the proper pins. Then you generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows for changing configurations at run time.

#### *Hybrid Designs*

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share common code editor, builder, and common debug, emulation, and programming tools.

#### *Code Generation Tools*

PSoC Designer supports multiple third-party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

**Assemblers.** The assemblers allow assembly code to be merged seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

**C Language Compilers.** C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

#### *Debugger*

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

#### *Online Help System*

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

#### *In-Circuit Emulator*

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

## Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select Components
2. Configure Components
3. Organize and Connect
4. Generate, Verify, and Debug

### Select Components

Both the system-level and chip-level views provide a library of pre-built, pre-tested hardware peripheral components. In the system-level view these components are called “drivers” and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces (I<sup>2</sup>C-bus, for example), and the logic to control how they interact with one another (called valuator).

In the chip-level view the components are called “user modules.” User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and programmable system-on-chip varieties.

### Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

### Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins, or connect system-level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view selecting a potentiometer driver to control a variable speed fan driver and setting up the valuator to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog-to-digital converter (ADC) to convert the potentiometer's output to a digital signal, and a PWM to control the fan.

In the chip-level view, you perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

### Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed. The system-level design also generates a C main() program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

## Document Conventions

### Acronyms Used

The following table lists the acronyms that are used in this document.

**Table 1. Acronyms**

Acronym	Description
AC	alternating current
API	application programming interface
CPU	central processing unit
DC	direct current
FSR	full scale range
GPIO	general purpose I/O
GUI	graphical user interface
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™
SLIMO	slow IMO
SRAM	static random access memory

### Units of Measure

A units of measure table is located in the Electrical Specifications section. [Table 11 on page 17](#) lists all the abbreviations used to measure the PSoC devices.

### Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimal.



## Pinouts

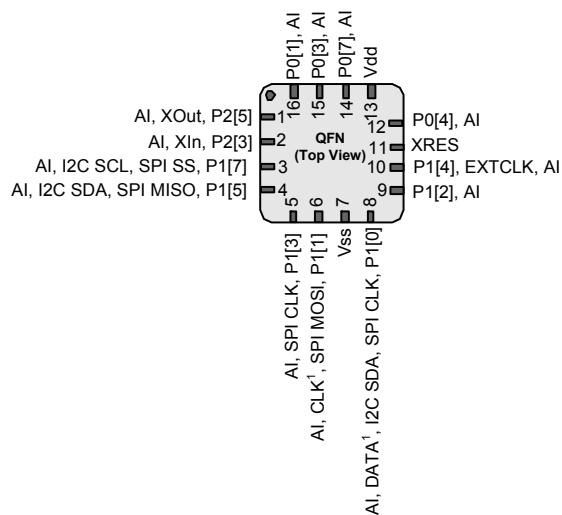
The CY8C20x36/46/66/96 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O and connection to the common analog bus. However, Vss, Vdd, and XRES are not capable of Digital I/O.

### 16-Pin QFN (No E-Pad)

**Table 2. Pin Definitions - CY8C20236, CY8C20246 PSoC Device** <sup>[2]</sup>

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	IOHR	I	P1[7]	I2C SCL, SPI SS
4	IOHR	I	P1[5]	I2C SDA, SPI MISO
5	IOHR	I	P1[3]	SPI CLK
6	IOHR	I	P1[1]	ISSP CLK <sup>[1]</sup> , I2C SCL, SPI MOSI
7	Power		Vss	Ground connection
8	IOHR	I	P1[0]	ISSP DATA <sup>[1]</sup> , I2C SDA, SPI CLK
9	IOHR	I	P1[2]	
10	IOHR	I	P1[4]	Optional external clock (EXTCLK)
11	Input		XRES	Active high external reset with internal pull down
12	IOH	I	P0[4]	
13	Power		Vdd	Supply voltage
14	IOH	I	P0[7]	
15	IOH	I	P0[3]	Integrating input
16	IOH	I	P0[1]	Integrating input

**Figure 2. CY8C20236, CY8C20246 PSoC Device**



**LEGEND** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

#### Notes

- These are the ISSP pins, which are not High Z at POR (Power On Reset).
- During power up or reset event, device P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter any issues.

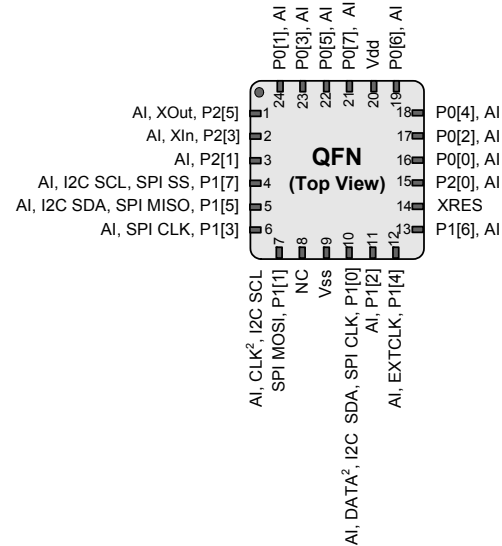
## 24-Pin QFN

**Table 3. Pin Definitions - CY8C20336, CY8C20346** [2, 3]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I2C SCL, SPI SS
5	IOHR	I	P1[5]	I2C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK <sup>[1]</sup> , I2C SCL, SPI MOSI
8			NC	No connection
9	Power		Vss	Ground connection
10	IOHR	I	P1[0]	ISSP DATA <sup>[1]</sup> , I2C SDA, SPI CLK
11	IOHR	I	P1[2]	
12	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
13	IOHR	I	P1[6]	
14	Input		XRES	Active high external reset with internal pull down
15	I/O	I	P2[0]	
16	IOH	I	P0[0]	
17	IOH	I	P0[2]	
18	IOH	I	P0[4]	
19	IOH	I	P0[6]	
20	Power		Vdd	Supply voltage
21	IOH	I	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input
24	IOH	I	P0[1]	Integrating input
CP	Power		Vss	Center pad must be connected to ground

**LEGEND** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

**Figure 3. CY8C20336, CY8C20346 PSoC Device**



### Note

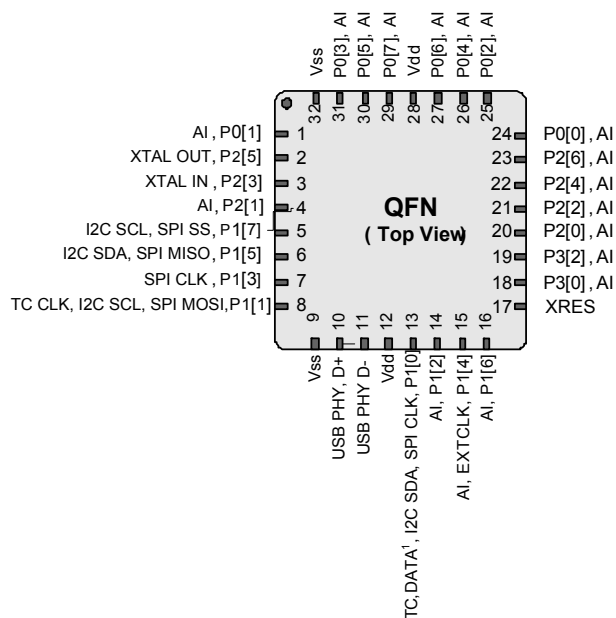
- The center pad (CP) on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.



**32-Pin QFN (with USB)**
**Table 6. Pin Definitions - CY8C20496 PSoC Device** [2, 3]

Pin No.	Type		Name	Description
	Digital	Analog		
1	IOH	I	P0[1]	
2	I/O	I	P2[5]	XTAL Out
3	I/O	I	P2[3]	XTAL In
4	I/O	I	P2[1]	
5	IOHR	I	P1[7]	I2C SCL, SPI SS
6	IOHR	I	P1[5]	I2C SDA, SPI MISO
7	IOHR	I	P1[3]	SPI CLK
8	IOHR	I	P1[1]	TC CLK, I2C SCL, SPI MOSI
9	Power		V <sub>SS</sub>	Ground Pin
10	I I		D+	USB PHY
11			D-	USB PHY
12	Power		V <sub>dd</sub>	Power pin
13	IOHR	I	P1[0]	TC DATA*, I2C SDA, SPI CLKI
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	EXTCLK
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	IOH	I	P0[0]	
25	IOH	I	P0[2]	
26	IOH	I	P0[4]	
27	IOH	I	P0[6]	
28	Power		V <sub>dd</sub>	Power Pin
29	IOH	I	P0[7]	
30	IOH	I	P0[5]	
31	IOH	I	P0[3]	
32	Power		V <sub>ss</sub>	Ground Pin

**LEGEND** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

**Figure 5. CY8C20496 PSoC Device**


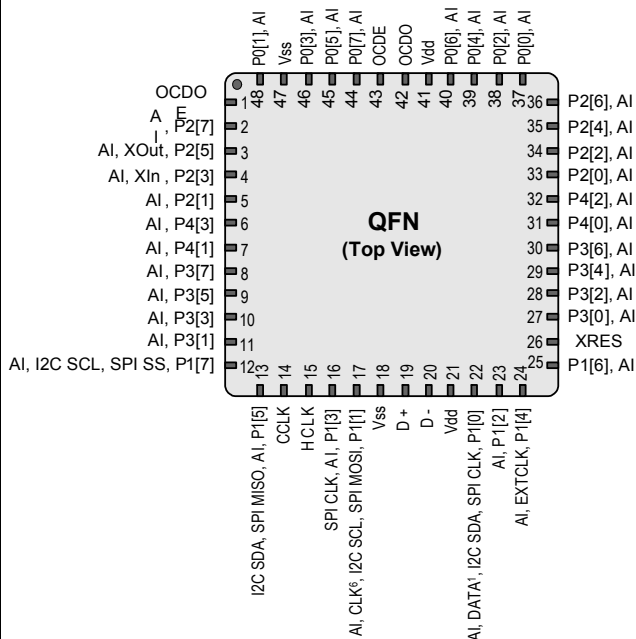
## 48-Pin QFN OCD

The 48-pin QFN part is for the CY8C20066 On-Chip Debug (OCD) PSoC device. Note that this part is only used for in-circuit debugging.<sup>[4]</sup>

**Table 10. Pin Definitions - CY8C20066 PSoC Device** <sup>[2, 3]</sup>

Pin No.	Digital	Analog	Name	Description
1			OCDOE	OCD mode direction pin
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I2C SCL, SPI SS
13	IOHR	I	P1[5]	I2C SDA, SPI MISO
14			CCLK	OCD CPU clock output
15			HCLK	OCD high speed clock output
16	IOHR	I	P1[3]	SPI CLK.
17	IOHR	I	P1[1]	ISSP CLK <sup>(1)</sup> , I2C SCL, SPI MOSI
18	Power		Vss	Ground connection
19	I/O		D+	USB D+
20	I/O		D-	USB D-
21	Power		Vdd	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA <sup>(1)</sup> , I2C SDA, SPI CLK
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	

**Figure 9. CY8C20066 PSoC Device**



Pin No.	Digital	Analog	Name	Description
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		Vdd	Supply voltage
42			OCDO	OCD even data I/O
43			OCDE	OCD odd data output
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		Vss	Ground connection
48	IOH	I	P0[1]	
CP	Power		Vss	Center pad must be connected to ground

**LEGEND** A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

### Note

4. This part is available in limited quantities for In-Circuit Debugging during prototype development. It is not available in production volumes.

## Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

**Table 12. Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Typ	Max	Units
T <sub>STG</sub>	Storage Temperature	Higher storage temperatures reduces data retention time. Recommended Storage Temperature is +25°C ± 25°C. Extended duration storage temperatures above 85°C degrades reliability.	–55	+25	+125	°C
V <sub>DD</sub>	Supply Voltage Relative to V <sub>SS</sub>		–0.5	–	+6.0	V
V <sub>IO</sub>	DC Input Voltage		V <sub>SS</sub> – 0.5	–	V <sub>DD</sub> + 0.5	V
V <sub>IOZ</sub>	DC Voltage Applied to Tri-state		V <sub>SS</sub> – 0.5	–	V <sub>DD</sub> + 0.5	V
I <sub>MIO</sub>	Maximum Current into any Port Pin		–25	–	+50	mA
ESD	Electro Static Discharge Voltage	Human Body Model ESD	2000	–	–	V
LU	Latch up Current	In accordance with JESD78 standard	–	–	200	mA

## Operating Temperature

**Table 13. Operating Temperature**

Symbol	Description	Conditions	Min	Typ	Max	Units
T <sub>A</sub>	Ambient Temperature		–40	–	+85	°C
T <sub>J</sub>	Operational Die Temperature	The temperature rise from ambient to junction is package specific. Refer the table <a href="#">Thermal Impedances per Package on page 34</a> . The user must limit the power consumption to comply with this requirement.	–40	–	+100	°C

**Table 15. 3.0V to 5.5V DC GPIO Specifications** *(continued)*

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>OH10</sub>	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	IOH = 1 mA, V <sub>dd</sub> > 2.7V, maximum of 20 mA source current in all IOs	1.20	–	–	V
V <sub>OL</sub>	Low Output Voltage	IOL = 25 mA, V <sub>dd</sub> > 3.3V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V <sub>IL</sub>	Input Low Voltage		–	–	0.80	V
V <sub>IH</sub>	Input High Voltage		2.00	–		V
V <sub>H</sub>	Input Hysteresis Voltage		–	80	–	mV
I <sub>IL</sub>	Input Leakage (Absolute Value)		–	0.001	1	μA
C <sub>PIN</sub>	Pin Capacitance	Package and pin dependent Temp = 25°C	0.5	1.7	5	pF

## AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 25. AC Chip-Level Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
F <sub>CPU</sub>	CPU Frequency		5.7	–	25.2	MHz
F <sub>32K1</sub>	Internal Low Speed Oscillator Frequency		19	32	50	kHz
F <sub>IMO24</sub>	Internal Main Oscillator Frequency at 24 MHz Setting		22.8	24	25.2	MHz
F <sub>IMO12</sub>	Internal Main Oscillator Frequency at 12 MHz Setting		11.4	12	12.6	MHz
F <sub>IMO6</sub>	Internal Main Oscillator Frequency at 6 MHz Setting		5.7	6.0	6.3	MHz
DC <sub>IMO</sub>	Duty Cycle of IMO		40	50	60	%
T <sub>RAMP</sub>	Supply Ramp Time		20	–	–	μs
T <sub>XRST</sub>	External Reset Pulse Width at Power Up	After supply voltage is valid	1			ms
T <sub>XRST2</sub>	External Reset Pulse Width after Power Up <sup>[10]</sup>	Applies after part has booted	10			μs

### Note

10. The minimum required XRES pulse length is longer when programming the device (see [Table 32 on page 28](#)).

**Table 27.AC Characteristics – USB Data Timings**

Symbol	Description	Conditions	Min	Typ	Max	Units
Td <sub>rate</sub>	Full speed data rate	Average bit rate	12–0.25%	12	12 + 0.25%	MHz
Td <sub>j1</sub>	Receiver data jitter tolerance	To next transition	-18.5	–	18.5	ns
Td <sub>j2</sub>	Receiver data jitter tolerance	To pair transition	-9	–	9	ns
Tud <sub>j1</sub>	Driver differential jitter	To next transition	-3.5	–	3.5	ns
Tud <sub>j2</sub>	Driver differential jitter	To pair transition	-4.0	–	4.0	ns
Tf <sub>deop</sub>	Source jitter for differential transition	To SE0 transition	-2	–	5	ns
Tf <sub>eopt</sub>	Source SE0 interval of EOP		160	–	175	ns
Tf <sub>eopr</sub>	Receiver SE0 interval of EOP		82	–		ns
Tf <sub>st</sub>	Width of SE0 interval during differential transition			–	14	ns

**Table 28.AC Characteristics – USB Driver**

Symbol	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time	50 pF	4	–	20	ns
Tf	Transition fall time	50 pF	4	–	20	ns
TR	Rise/fall time matching		90.00	–	111.1	%
V <sub>crs</sub>	Output signal crossover voltage		1.3	–	2.0	V

### AC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 29. AC Low Power Comparator Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
T <sub>LPC</sub>	Comparator Response Time, 50 mV Overdrive	50 mV overdrive does not include offset voltage.			100	ns

### AC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 30. AC Analog Mux Bus Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
F <sub>SW</sub>	Switch Rate	Maximum pin voltage when measuring switch rate is 1.8Vp-p	–	–	6.3	MHz

### AC External Clock Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

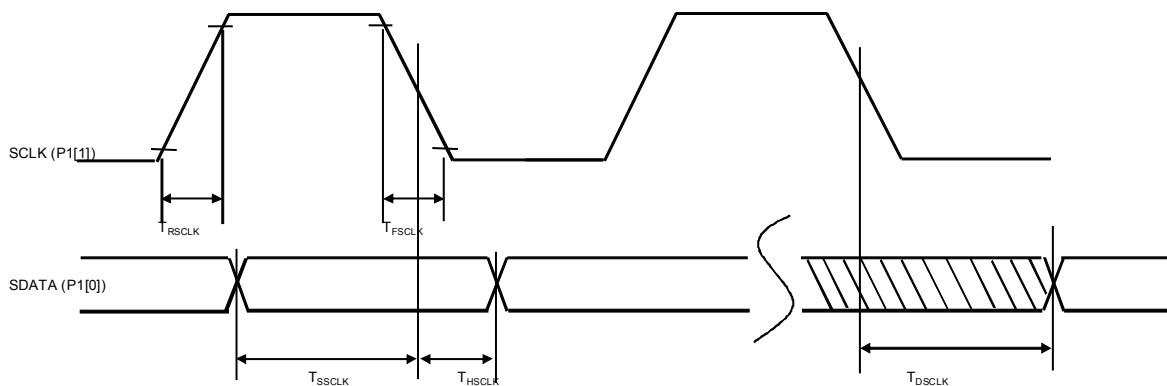
**Table 31. AC External Clock Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
F <sub>OSCEXT</sub>	Frequency		0.750	–	25.2	MHz
–	High Period		20.6	–	5300	ns
–	Low Period		20.6	–	–	ns
–	Power Up IMO to Switch		150	–	–	μs



## AC Programming Specifications

**Figure 13. AC Waveform**



The following table lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 32. AC Programming Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$T_{RCLK}$	Rise Time of SCLK		1	–	20	ns
$T_{FCLK}$	Fall Time of SCLK		1	–	20	ns
$T_{SSCLK}$	Data Set up Time to Falling Edge of SCLK		40	–	–	ns
$T_{HSCLK}$	Data Hold Time from Falling Edge of SCLK		40	–	–	ns
$F_{SCLK}$	Frequency of SCLK		0	–	8	MHz
$T_{ERASEB}$	Flash Erase Time (Block)		–	–	18	ms
$T_{WRITE}$	Flash Block Write Time		–	–	25	ms
$T_{DSCLK}$	Data Out Delay from Falling Edge of SCLK	$3.6 < V_{dd}$	–	–	60	ns
$T_{DSCLK3}$	Data Out Delay from Falling Edge of SCLK	$3.0 \leq V_{dd} \leq 3.6$	–	–	85	ns
$T_{DSCLK2}$	Data Out Delay from Falling Edge of SCLK	$1.71 \leq V_{dd} \leq 3.0$	–	–	130	ns
$T_{XRST3}$	External Reset Pulse Width after Power Up	Required to enter programming mode when coming out of sleep	263	–	–	$\mu$ s

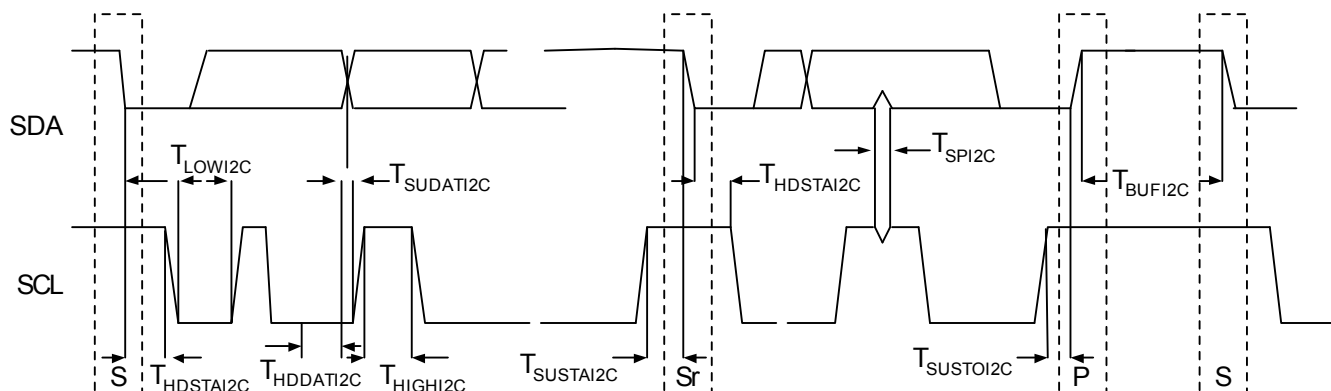
## AC I2C Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 33. AC Characteristics of the I2C SDA and SCL Pins**

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
$F_{SCL I2C}$	SCL Clock Frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	$\mu$ s
$T_{LOWI2C}$	LOW Period of the SCL Clock	4.7	–	1.3	–	$\mu$ s
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	$\mu$ s
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	$\mu$ s
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	$\mu$ s
$T_{SUDATI2C}$	Data Setup Time	250	–	100 <sup>[11]</sup>	–	ns
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	0.6	–	$\mu$ s
$T_{BUFI2C}$	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	$\mu$ s
$T_{SPI2C}$	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns

**Figure 14. Definition for Timing for Fast/Standard Mode on the I<sup>2</sup>C Bus**



### Note

11. A Fast-Mode I2C-bus device can be used in a Standard Mode I2C-bus system, but the requirement  $t_{SU,DAT} \geq 250$  ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_{rmax} + t_{SU,DAT} = 1000 + 250 = 1250$  ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

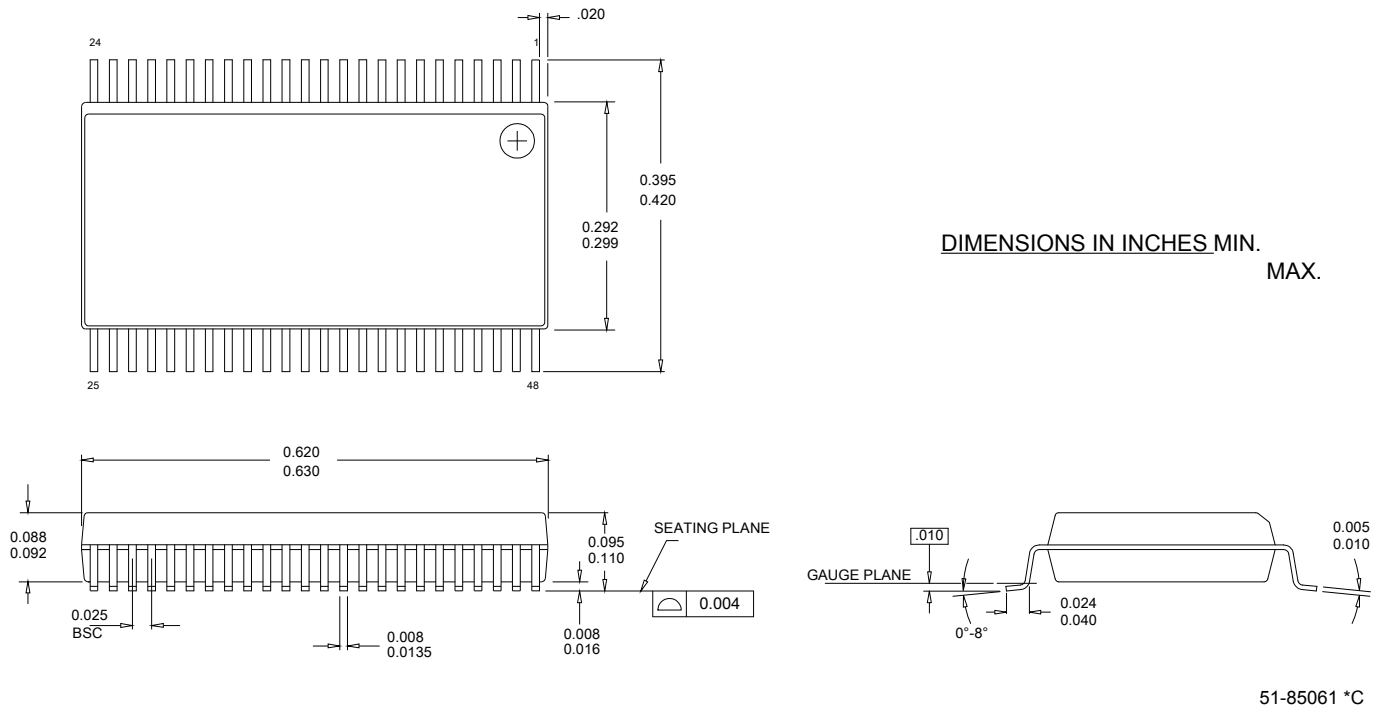
**Table 34. SPI Master AC Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$F_{SCLK}$	SCLK clock frequency	$V_{DD} \geq 2.4V$ $V_{DD} < 2.4V$			6 3	MHz
DC	SCLK duty cycle			50		%
$T_{SETUP}$	MISO to SCLK setup time	$V_{DD} \geq 2.4V$ $V_{DD} < 2.4V$	60 100			ns
$T_{HOLD}$	SCLK to MISO hold time		40			ns
$T_{OUT\_VAL}$	SCLK to MOSI valid time				40	ns
$T_{OUT\_HIGH}$	MOSI high time		40			ns

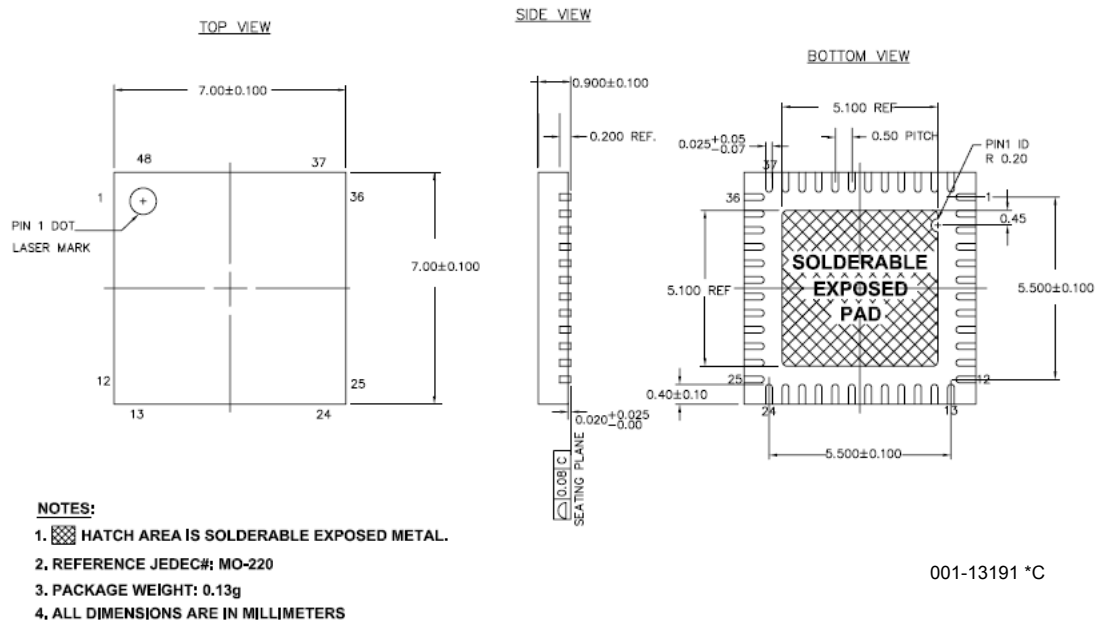
**Table 35. SPI Slave AC Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$F_{SCLK}$	SCLK clock frequency	$V_{DD} \geq 2.4V$ $V_{DD} < 2.4V$			12 6	MHz
$T_{LOW}$	SCLK low time		41.67			ns
$T_{HIGH}$	SCLK high time		41.67			ns
$T_{SETUP}$	MOSI to SCLK setup time		30			ns
$T_{HOLD}$	SCLK to MOSI hold time		50			ns
$T_{SS\_MISO}$	SS high to MISO valid				153	ns
$T_{SCLK\_MISO}$	SCLK to MISO valid				125	ns
$T_{SS\_HIGH}$	SS high time				50	ns
$T_{SS\_CLK}$	Time from SS low to first SCLK		2/SCLK			ns
$T_{CLK\_SS}$	Time from last SCLK to SS high		2/SCLK			ns

**Figure 18. 48-Pin (300 MIL) SSOP**



**Figure 19. 48-Pin (7x7 mm) QFN**



### Important Notes

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at [http://www.amkor.com/products/notes\\_papers/MLFAppNote.pdf](http://www.amkor.com/products/notes_papers/MLFAppNote.pdf).
- Pinned vias for thermal conduction are not required for the low power PSoC device.

## Device Programmers

All device programmers are purchased from the Cypress Online Store.

### CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- Three Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

### CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment.

Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

## Accessories (Emulation and Programming)

**Table 38. Emulation and Programming Accessories**

Part Number	Pin Package	Flex-Pod Kit <sup>[15]</sup>	Foot Kit <sup>[16]</sup>	Adapter <sup>[17]</sup>
CY8C20236-24LKXI	16 QFN	CY3250-20266QFN	CY3250-16QFN-RK	See note 15
CY8C20246-24LKXI	16 QFN	CY3250-20266QFN	CY3250-16QFN-FK	See note 17
CY8C20336-24LQXI	24 QFN	CY3250-20366QFN	CY3250-24QFN-FK	See note 15
CY8C20346-24LQXI	24 QFN	CY3250-20366QFN	CY3250-24QFN-FK	See note 17
CY8C20396-24LQXI	24 QFN	Not Available		
CY8C20436-24LQXI	32 QFN	CY3250-20466QFN	CY3250-32QFN-RK	See note 15
CY8C20446-24LQXI	32 QFN	CY3250-20466QFN	CY3250-32QFN-FK	See note 17
CY8C20466-24LQXI	32 QFN	CY3250-20466QFN	CY3250-32QFN-FK	See note 17
CY8C20496-24LQXI	32 QFN	Not Available		
CY8C20536-24PVXI	48 SSOP	CY3250-20X66	CY3250-48SSOP-FK	See note 17
CY8C20546-24PVXI	48 SSOP	CY3250-20X66	CY3250-48SSOP-FK	See note 17
CY8C20566-24PVXI	48 SSOP	CY3250-20X66	CY3250-48SSOP-FK	See note 17
CY8C20636-24LTXI	48 QFN	CY3250-20666QFN	CY3250-48QFN-FK	See note 17
CY8C20646-24LTXI	48 QFN	CY3250-20666QFN	CY3250-48QFN-FK	See note 17
CY8C20666-24LTXI	48 QFN	CY3250-20666QFN	CY3250-48QFN-FK	See note 17

## Third-Party Tools

Several tools have been specially designed by the following third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at <http://www.cypress.com> under Documentation > Evaluation Boards.

### Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, refer Application Note "Debugging - Build a PSoC Emulator into Your Board - AN2323" at <http://www.cypress.com/?rID2748>.

#### Notes

15. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.

16. Foot kit includes surface mount feet that can be soldered to the target PCB.

17. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at <http://www.emulation.com>.

## Ordering Information

The following table lists the CY8C20x36/46/66/96 PSoC devices' key package features and ordering codes.

**Table 39. PSoC Device Key Features and Ordering Information**

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	CapSense Blocks	Digital I/O Pins	Analog Inputs <sup>[18]</sup>	XRES Pin	USB
16-Pin (3x3x0.6mm) QFN	CY8C20236-24LKXI	8K	1K	1	13	13	Yes	No
16-Pin (3x3x0.6mm) QFN (Tape and Reel)	CY8C20236-24LKXIT	8K	1K	1	13	13	Yes	No
16 Pin (3x3 x 0.6 mm) QFN	CY8C20246-24LKXI	16K	2K	1	13	13	Yes	No
16 Pin (3x3 x 0.6 mm) QFN (Tape and Reel)	CY8C20246-24LKXIT	16K	2K	1	13	13	Yes	No
24-Pin (4x4x0.6mm) QFN	CY8C20336-24LQXI	8K	1K	1	20	20	Yes	No
24-Pin (4x4x0.6mm) QFN (Tape and Reel)	CY8C20336-24LQXIT	8K	1K	1	20	20	Yes	No
24 Pin (4x4 x 0.6 mm) QFN	CY8C20346-24LQXI	16K	2K	1	20	20	Yes	No
24 Pin (4x4 x 0.6 mm) QFN (Tape and Reel)	CY8C20346-24LQXIT	16K	2K	1	20	20	Yes	No
24-Pin (4x4x0.6mm) QFN	CY8C20396-24LQXI	16K	2K	1	19	19	Yes	Yes
24-Pin (4x4x0.6mm) QFN (Tape and Reel)	CY8C20396-24LQXIT	16K	2K	1	19	19	Yes	Yes
32-Pin (5x5x0.6mm) QFN	CY8C20436-24LQXI	8K	1K	1	28	28	Yes	No
32-Pin (5x5x0.6mm) QFN (Tape and Reel)	CY8C20436-24LQXIT	8K	1K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20446-24LQXI	16K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20446-24LQXIT	16K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20466-24LQXI	32K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20466-24LQXIT	32K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20496-24LQXI	16K	2K	1	25	25	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20496-24LQXIT	16K	2K	1	25	25	Yes	No
48-Pin SSOP	CY8C20536-24PVXI	8K	1K	1	36	36	Yes	No
48-Pin SSOP (Tape and Reel)	CY8C20536-24PVXIT	8K	1K	1	36	36	Yes	No
48-Pin SSOP	CY8C20546-24PVXI	16K	2K	1	36	36	Yes	No
48-Pin SSOP (Tape and Reel)	CY8C20546-24PVXIT	16K	2K	1	36	36	Yes	No
48-Pin SSOP	CY8C20566-24PVXI	32K	2K	1	36	36	Yes	No
48-Pin SSOP (Tape and Reel)	CY8C20566-24PVXIT	32K	2K	1	36	36	Yes	No
48 Pin (7x7 mm) QFN	CY8C20636-24LTXI	8K	1K	1	36	36	Yes	No
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20636-24LTXIT	8K	1K	1	36	36	Yes	No
48 Pin (7x7 mm) QFN	CY8C20646-24LTXI	16K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20646-24LTXIT	16K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN	CY8C20666-24LTXI	32K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20666-24LTXIT	32K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN (OCD) <sup>[4]</sup>	CY8C20066-24LTXI	32K	2K	1	36	36	Yes	Yes

### Notes

18. Dual-function Digital I/O Pins also connect to the common analog mux.



## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [cypress.com/sales](http://cypress.com/sales).

#### Products

PSoC	<a href="http://psoc.cypress.com">psoc.cypress.com</a>
Clocks & Buffers	<a href="http://clocks.cypress.com">clocks.cypress.com</a>
Wireless	<a href="http://wireless.cypress.com">wireless.cypress.com</a>
Memories	<a href="http://memory.cypress.com">memory.cypress.com</a>
Image Sensors	<a href="http://image.cypress.com">image.cypress.com</a>

#### PSoC Solutions

General	<a href="http://psoc.cypress.com/solutions">psoc.cypress.com/solutions</a>
Low Power/Low Voltage	<a href="http://psoc.cypress.com/low-power">psoc.cypress.com/low-power</a>
Precision Analog	<a href="http://psoc.cypress.com/precision-analog">psoc.cypress.com/precision-analog</a>
LCD Drive	<a href="http://psoc.cypress.com/lcd-drive">psoc.cypress.com/lcd-drive</a>
CAN 2.0b	<a href="http://psoc.cypress.com/can">psoc.cypress.com/can</a>
USB	<a href="http://psoc.cypress.com/usb">psoc.cypress.com/usb</a>

© Cypress Semiconductor Corporation, 2007-2009. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.