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What Are Embedded - Microcontrollers - Application Specific?

Application specific microcontrollers are engineered to

Details

Product Status	Obsolete
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (16kB)
Controller Series	CY8C20xx6
RAM Size	2K x 8
Interface	I ² C, SPI, USB
Number of I/O	19
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	24-UFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20396-24lqxit

PSoC® Functional Overview

The PSoC family consists of on-chip Controller devices. These devices are designed to replace multiple traditional MCU-based components with one, low cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the [Logic Block Diagram on page 2](#), is comprised of three main areas: the Core, the CapSense Analog System, and the System Resources (including a full speed USB port). A common, versatile bus allows connection between I/O and the analog system. Each CY8C20x36/46/66/96 PSoC Device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 36 general purpose IO (GPIO) are also included. The GPIO provides access to the MCU and analog mux.

PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO (internal main oscillator) and ILO (internal low speed oscillator). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-MIPS, 8-bit Harvard architecture microprocessor.

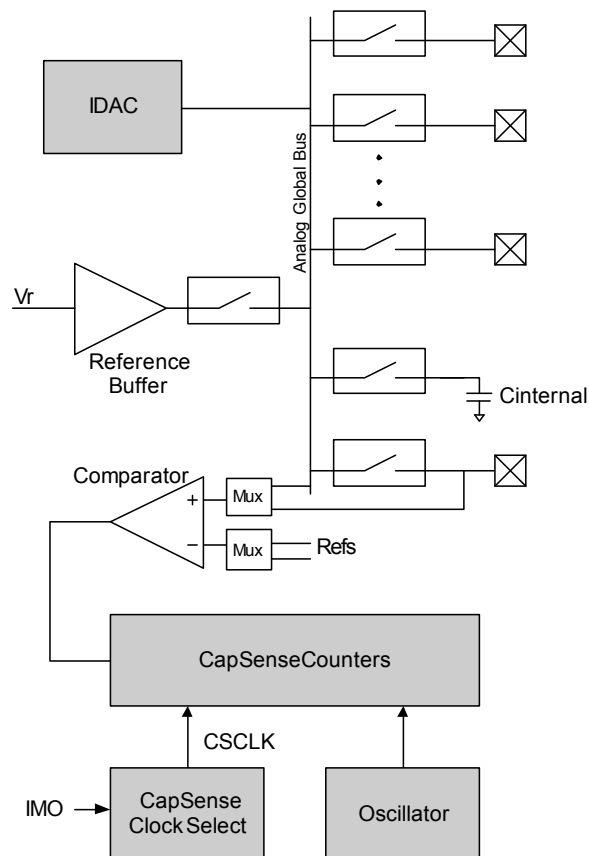
System Resources provide additional capability, such as configurable USB and I2C slave/SPI master-slave communication interface, three 16-bit programmable timers, and various system resets supported by the M8C.

The Analog System is composed of the CapSense PSoC block and an internal 1.2V analog reference, which together support capacitive sensing of up to 36 inputs.

CapSense Analog System

The Analog System contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins are completed quickly and easily across multiple ports.

Figure 1. Analog System Block Diagram



Analog Multiplexer System

The Analog Mux Bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces, such as sliders and touchpads.
- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

When designing capacitive sensing applications, refer to the latest signal-to-noise signal level requirements Application Notes, which can be found under <http://www.cypress.com> > Documentation > Application Notes. In general, and unless otherwise noted in the relevant Application Notes, the minimum signal-to-noise ratio (SNR) for CapSense applications is 5:1.

Additional System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The merits of each system resource are listed here:

- The I2C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I2C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power-On-Reset) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO.
- Standard Cypress PSoC IDE tools are available for debugging the CY8C20x36/46/66/96 family of parts. However, the additional trace length and a minimal ground plane in the Flex-Pod can create noise problems that make it difficult to debug the design. A custom bonded On-Chip Debug (OCD) device is available in an 48-pin QFN package. The OCD device is recommended for debugging designs that have high current and/or high analog accuracy requirements. The QFN package is compact and is connected to the ICE through a high density connector.

Getting Started

The quickest way to understand PSoC silicon is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the PSoC® Programmable System-on-Chip™ Technical Reference Manual for CY8C20x36/46/66/96 PSoC Devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at www.cypress.com/psoc.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located here: www.cypress.com/psoc. Select Application Notes under the Documentation tab.

Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

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Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select Components
2. Configure Components
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

Both the system-level and chip-level views provide a library of pre-built, pre-tested hardware peripheral components. In the system-level view these components are called “drivers” and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces (I²C-bus, for example), and the logic to control how they interact with one another (called valuator).

In the chip-level view the components are called “user modules.” User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and programmable system-on-chip varieties.

Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins, or connect system-level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view selecting a potentiometer driver to control a variable speed fan driver and setting up the valuator to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog-to-digital converter (ADC) to convert the potentiometer's output to a digital signal, and a PWM to control the fan.

In the chip-level view, you perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed. The system-level design also generates a C main() program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Table 1. Acronyms

Acronym	Description
AC	alternating current
API	application programming interface
CPU	central processing unit
DC	direct current
FSR	full scale range
GPIO	general purpose I/O
GUI	graphical user interface
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™
SLIMO	slow IMO
SRAM	static random access memory

Units of Measure

A units of measure table is located in the Electrical Specifications section. [Table 11 on page 17](#) lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or '0x' are decimal.

Pinouts

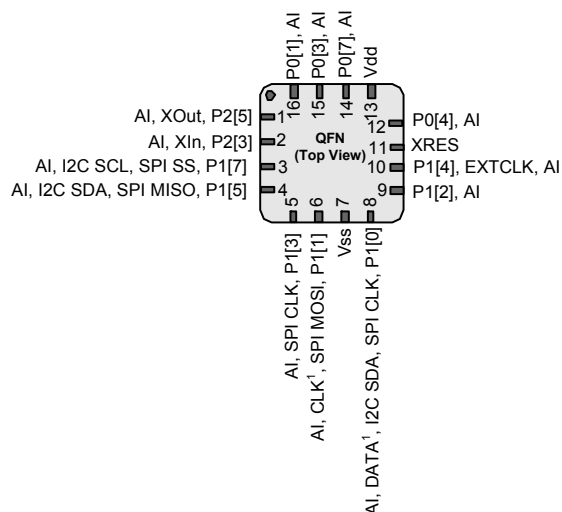
The CY8C20x36/46/66/96 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O and connection to the common analog bus. However, Vss, Vdd, and XRES are not capable of Digital I/O.

16-Pin QFN (No E-Pad)

Table 2. Pin Definitions - CY8C20236, CY8C20246 PSoC Device ^[2]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	IOHR	I	P1[7]	I2C SCL, SPI SS
4	IOHR	I	P1[5]	I2C SDA, SPI MISO
5	IOHR	I	P1[3]	SPI CLK
6	IOHR	I	P1[1]	ISSP CLK ^[1] , I2C SCL, SPI MOSI
7	Power		Vss	Ground connection
8	IOHR	I	P1[0]	ISSP DATA ^[1] , I2C SDA, SPI CLK
9	IOHR	I	P1[2]	
10	IOHR	I	P1[4]	Optional external clock (EXTCLK)
11	Input		XRES	Active high external reset with internal pull down
12	IOH	I	P0[4]	
13	Power		Vdd	Supply voltage
14	IOH	I	P0[7]	
15	IOH	I	P0[3]	Integrating input
16	IOH	I	P0[1]	Integrating input

Figure 2. CY8C20236, CY8C20246 PSoC Device



LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Notes

- These are the ISSP pins, which are not High Z at POR (Power On Reset).
- During power up or reset event, device P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter any issues.

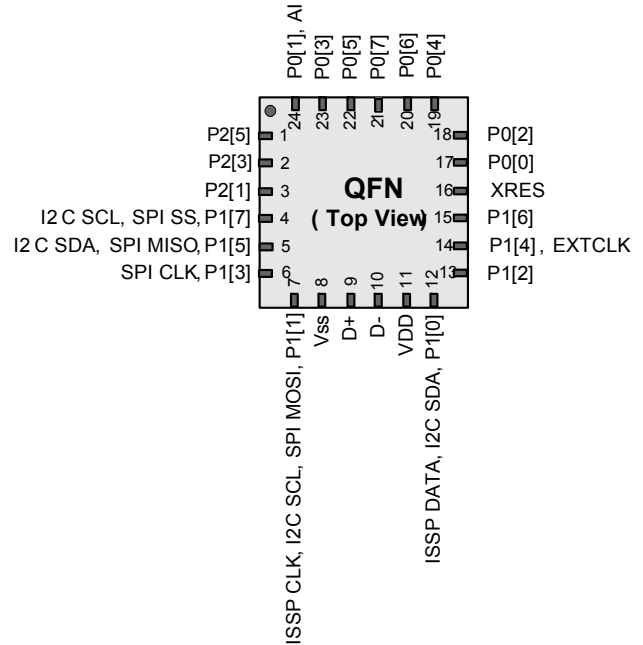
24-Pin QFN with USB

Table 4. Pin Definitions - CY8C20396 PSoC Device [2, 3]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	
2	I/O	I	P2[3]	
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I2C SCL, SPI SS
5	IOHR	I	P1[5]	I2C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK, I2C SCL, SPI MOSI
8	Power		VSS	Ground
9	I/O	I	D+	USB D+
10	I/O	I	D-	USB D-
11	Power		VDD	Supply
12	IOHR	I	P1[0]	ISSP DATA, I2C SDA
13	IOHR	I	P1[2]	
14	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
15	IOHR	I	P1[6]	
16	RESET INPUT		XRES	Active high external reset with internal pull down
17	IOH	I	P0[0]	
18	IOH	I	P0[2]	
19	IOH	I	P0[4]	
20	IOH	I	P0[6]	
21	IOH	I	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input
24	IOH	I	P0[1]	Integrating input
CP	Power		VSS	Thermal pad must be connected to Ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

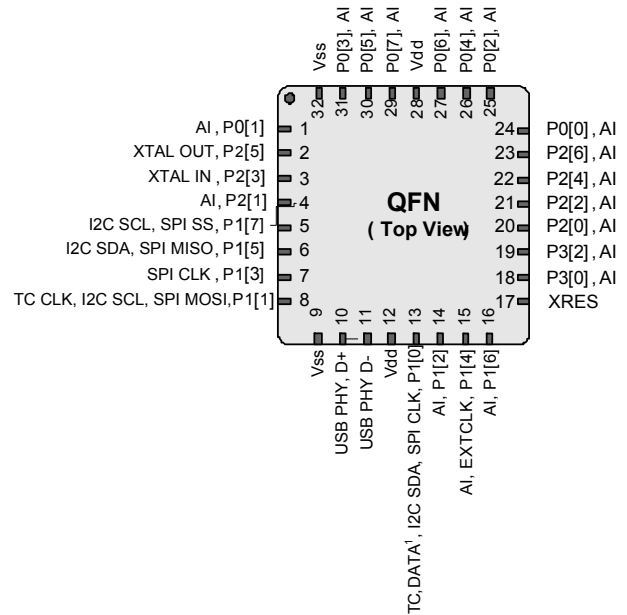
Figure 4. CY8C20396 PSoC Device



32-Pin QFN (with USB)
Table 6. Pin Definitions - CY8C20496 PSoC Device [2, 3]

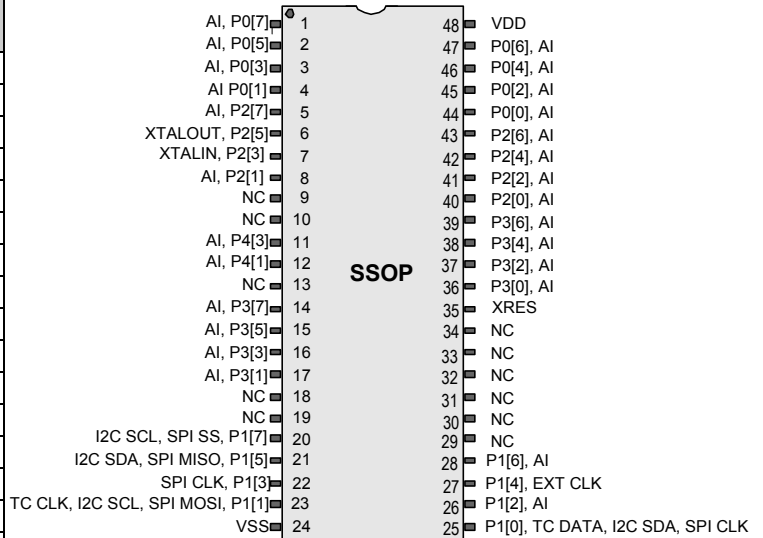
Pin No.	Type		Name	Description
	Digital	Analog		
1	IOH	I	P0[1]	
2	I/O	I	P2[5]	XTAL Out
3	I/O	I	P2[3]	XTAL In
4	I/O	I	P2[1]	
5	IOHR	I	P1[7]	I2C SCL, SPI SS
6	IOHR	I	P1[5]	I2C SDA, SPI MISO
7	IOHR	I	P1[3]	SPI CLK
8	IOHR	I	P1[1]	TC CLK, I2C SCL, SPI MOSI
9	Power		V _{SS}	Ground Pin
10	I I		D+	USB PHY
11			D-	USB PHY
12	Power		V _{dd}	Power pin
13	IOHR	I	P1[0]	TC DATA*, I2C SDA, SPI CLKI
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	EXTCLK
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	IOH	I	P0[0]	
25	IOH	I	P0[2]	
26	IOH	I	P0[4]	
27	IOH	I	P0[6]	
28	Power		V _{dd}	Power Pin
29	IOH	I	P0[7]	
30	IOH	I	P0[5]	
31	IOH	I	P0[3]	
32	Power		V _{ss}	Ground Pin

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 5. CY8C20496 PSoC Device


48-Pin SSOP
Table 7. Pin Definitions - CY8C20536, CY8C20546, and CY8C20566 PSoC Device^[2]

Pin No.	Digital	Analog	Name	Description
1	IOH	I	P0[7]	
2	IOH	I	P0[5]	
3	IOH	I	P0[3]	
4	IOH	I	P0[1]	
5	I/O	I	P2[7]	
6	I/O	I	P2[5]	XTAL Out
7	I/O	I	P2[3]	XTAL In
8	I/O	I	P2[1]	
9			NC	No connection
10			NC	No connection
11	I/O	I	P4[3]	
12	I/O	I	P4[1]	
13			NC	No connection
14	I/O	I	P3[7]	
15	I/O	I	P3[5]	
16	I/O	I	P3[3]	
17	I/O	I	P3[1]	
18			NC	No connection
19			NC	No connection
20	IOHR	I	P1[7]	I2C SCL, SPI SS
21	IOHR	I	P1[5]	I2C SDA, SPI MISO
22	IOHR	I	P1[3]	SPI CLK
23	IOHR	I	P1[1]	TC CLK ^[1] , I2C SCL, SPI MOSI
24			VSS	Ground Pin
25	IOHR	I	P1[0]	TC DATA ^[1] , I2C SDA, SPI CLK
26	IOHR	I	P1[2]	
27	IOHR	I	P1[4]	EXT CLK
28	IOHR	I	P1[6]	
29			NC	No connection
30			NC	No connection
31			NC	No connection
32			NC	No connection
33			NC	No connection
34			NC	No connection
35			XRES	Active high external reset with internal pull down
36	I/O	I	P3[0]	
37	I/O	I	P3[2]	
38	I/O	I	P3[4]	
39	I/O	I	P3[6]	
40	I/O	I	P2[0]	

Figure 6. CY8C20536, CY8C20546, and CY8C20566 PSoC Device


Pin No.	Digital	Analog	Name	Description
41	I/O	I	P2[2]	
42	I/O	I	P2[4]	
43	I/O	I	P2[6]	
44	IOH	I	P0[0]	
45	IOH	I	P0[2]	
46	IOH	I	P0[4]	
47	IOH	I	P0[6]	
48	Power		Vdd	Power Pin

LEGEND A = Analog, I = Input, O = Output, NC = No Connection, H = 5 mA High Output Drive, R = Regulated Output Option.

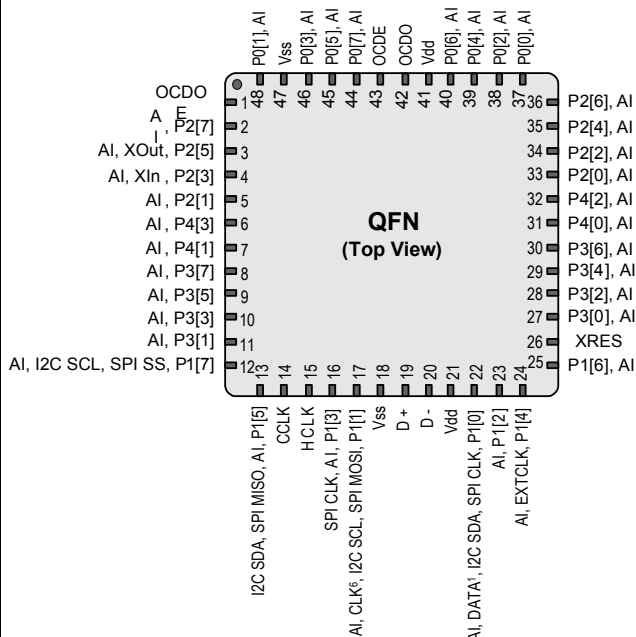
48-Pin QFN OCD

The 48-pin QFN part is for the CY8C20066 On-Chip Debug (OCD) PSoC device. Note that this part is only used for in-circuit debugging.^[4]

Table 10. Pin Definitions - CY8C20066 PSoC Device ^[2, 3]

Pin No.	Digital	Analog	Name	Description
1			OCDOE	OCD mode direction pin
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I2C SCL, SPI SS
13	IOHR	I	P1[5]	I2C SDA, SPI MISO
14			CCLK	OCD CPU clock output
15			HCLK	OCD high speed clock output
16	IOHR	I	P1[3]	SPI CLK.
17	IOHR	I	P1[1]	ISSP CLK ⁽¹⁾ , I2C SCL, SPI MOSI
18	Power		Vss	Ground connection
19	I/O		D+	USB D+
20	I/O		D-	USB D-
21	Power		Vdd	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA ⁽¹⁾ , I2C SDA, SPI CLK
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	

Figure 9. CY8C20066 PSoC Device



Pin No.	Digital	Analog	Name	Description
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		Vdd	Supply voltage
42			OCDO	OCD even data I/O
43			OCDE	OCD odd data output
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		Vss	Ground connection
48	IOH	I	P0[1]	
CP	Power		Vss	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

Note

4. This part is available in limited quantities for In-Circuit Debugging during prototype development. It is not available in production volumes.

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 14. DC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V _{DD}	Supply Voltage	Refer the table DC POR and LVD Specifications on page 24	1.71	–	5.5	V
I _{DD24}	Supply Current, IMO = 24 MHz	Conditions are V _{DD} = 3.0V, T _A = 25°C, CPU = 24 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	2.88	4.0	mA
I _{DD12}	Supply Current, IMO = 12 MHz	Conditions are V _{DD} = 3.0V, T _A = 25°C, CPU = 12 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	1.71	2.6	mA
I _{DD6}	Supply Current, IMO = 6 MHz	Conditions are V _{DD} = 3.0V, T _A = 25°C, CPU = 6 MHz. CapSense running at 6 MHz, no I/O sourcing current	–	1.16	1.8	mA
I _{SB0}	Deep Sleep Current	V _{DD} = 3.0V, T _A = 25°C, I/O regulator turned off	–	0.1	–	μA
I _{SB1}	Standby Current with POR, LVD and Sleep Timer	V _{DD} = 3.0V, T _A = 25°C, I/O regulator turned off	–	1.07	1.5	μA

DC General Purpose IO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 5.5V and –40°C ≤ T_A ≤ 85°C, 2.4V to 3.0V and –40°C ≤ T_A ≤ 85°C, or 1.71V to 2.4V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 15. 3.0V to 5.5V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R _{PU}	Pull up Resistor		4	5.6	8	kΩ
V _{OH1}	High Output Voltage Port 2 or 3 Pins	IOH ≤ 10 μA, maximum of 10 mA source current in all IOs	V _{DD} - 0.2	–	–	V
V _{OH2}	High Output Voltage Port 2 or 3 Pins	IOH = 1 mA, maximum of 20 mA source current in all IOs	V _{DD} - 0.9	–	–	V
V _{OH3}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	IOH < 10 μA, maximum of 10 mA source current in all IOs	V _{DD} - 0.2	–	–	V
V _{OH4}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	IOH = 5 mA, maximum of 20 mA source current in all IOs	V _{DD} - 0.9	–	–	V
V _{OH5}	High Output Voltage Port 1 Pins with LDO Regulator Enabled for 3V Out	IOH < 10 μA, V _{DD} > 3.1V, maximum of 4 IOs all sourcing 5 mA	2.85	3.00	3.3	V
V _{OH6}	High Output Voltage Port 1 Pins with LDO Regulator Enabled for 3V Out	IOH = 5 mA, V _{DD} > 3.1V, maximum of 20 mA source current in all IOs	2.20	–	–	V
V _{OH7}	High Output Voltage Port 1 Pins with LDO Enabled for 2.5V Out	IOH < 10 μA, V _{DD} > 2.7V, maximum of 20 mA source current in all IOs	2.35	2.50	2.75	V
V _{OH8}	High Output Voltage Port 1 Pins with LDO Enabled for 2.5V Out	IOH = 2 mA, V _{DD} > 2.7V, maximum of 20 mA source current in all IOs	1.90	–	–	V
V _{OH9}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	IOH < 10 μA, V _{DD} > 2.7V, maximum of 20 mA source current in all IOs	1.60	1.80	2.1	V

Table 15. 3.0V to 5.5V DC GPIO Specifications *(continued)*

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OH10}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	$I_{OH} = 1\text{ mA}$, $V_{dd} > 2.7\text{V}$, maximum of 20 mA source current in all IOs	1.20	–	–	V
V_{OL}	Low Output Voltage	$I_{OL} = 25\text{ mA}$, $V_{dd} > 3.3\text{V}$, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input Low Voltage		–	–	0.80	V
V_{IH}	Input High Voltage		2.00	–		V
V_H	Input Hysteresis Voltage		–	80	–	mV
I_{IL}	Input Leakage (Absolute Value)		–	0.001	1	μA
C_{PIN}	Pin Capacitance	Package and pin dependent Temp = 25°C	0.5	1.7	5	pF

Table 16. 2.4V to 3.0V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R _{PU}	Pull up Resistor		4	5.6	8	kΩ
V _{OH1}	High Output Voltage Port 2 or 3 Pins	I _{OH} < 10 μA, maximum of 10 mA source current in all IOs	V _{dd} - 0.2	–	–	V
V _{OH2}	High Output Voltage Port 2 or 3 Pins	I _{OH} = 0.2 mA, maximum of 10 mA source current in all IOs	V _{dd} - 0.4	–	–	V
V _{OH3}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I _{OH} < 10 μA, maximum of 10 mA source current in all IOs	V _{dd} - 0.2	–	–	V
V _{OH4}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I _{OH} = 2 mA, maximum of 10 mA source current in all IOs	V _{dd} - 0.5	–	–	V
V _{OH5A}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	I _{OH} < 10 μA, V _{dd} > 2.4V, maximum of 20 mA source current in all IOs	1.50	1.80	2.1	V
V _{OH6A}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	I _{OH} = 1 mA, V _{dd} > 2.4V, maximum of 20 mA source current in all IOs	1.20	–	–	V
V _{OL}	Low Output Voltage	I _{OL} = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V _{IL}	Input Low Voltage		–	–	0.72	V
V _{IH}	Input High Voltage		1.4	–		V
V _H	Input Hysteresis Voltage		–	80	–	mV
I _{IL}	Input Leakage (Absolute Value)		–	0.001	1	μA
C _{PIN}	Capacitive Load on Pins	Package and pin dependent Temp = 25°C	0.5	1.7	5	pF

Table 17. 1.71V to 2.4V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R _{PU}	Pull up Resistor		4	5.6	8	kΩ
V _{OH1}	High Output Voltage Port 2 or 3 Pins	I _{OH} = 10 μA, maximum of 10 mA source current in all I/Os	V _{dd} - 0.2	–	–	V
V _{OH2}	High Output Voltage Port 2 or 3 Pins	I _{OH} = 0.5 mA, maximum of 10 mA source current in all I/Os	V _{dd} - 0.5	–	–	V
V _{OH3}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I _{OH} = 100 μA, maximum of 10 mA source current in all I/Os	V _{dd} - 0.2	–	–	V
V _{OH4}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I _{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V _{dd} - 0.5	–	–	V
V _{OL}	Low Output Voltage	I _{OL} = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.4	V
V _{IL}	Input Low Voltage		–	–	0.3 x V _{dd}	V
V _{IH}	Input High Voltage		0.65 x V _{dd}	–		V

Comparator User Module Electrical Specifications

The following table lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: $-40^{\circ}\text{C} \leq \text{TA} \leq 85^{\circ}\text{C}$, $1.71\text{V} \leq \text{Vdd} \leq 5.5\text{V}$.

Table 21. Comparator User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{COMP}	Comparator Response Time	50 mV overdrive		70	100	ns
Offset				2.5	30	mV
Current		Average DC current, 50 mV overdrive		20	80	μA
PSRR	Supply voltage $>2\text{V}$	Power Supply Rejection Ratio		80		dB
	Supply voltage $<2\text{V}$	Power Supply Rejection Ratio		40		dB
Input Range			0		1.5	V

ADC Electrical Specifications

Table 22. ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input Voltage Range	This gives 72% of maximum code	V_{SS}		1.3	V
C_{IN}	Input Capacitance				5	pF
RES	Resolution	Settings 8, 9, or 10	8		10	Bits
S8	8-Bit Sample Rate	Data Clock set to 6 MHz. Sample Rate = $0.001 / (2^{\text{Resolution}} / \text{Data clock})$		23.4375		ksps
S10	10-Bit Sample Rate	Data Clock set to 6 MHz. Sample Rate = $0.001 / (2^{\text{Resolution}} / \text{Data clock})$		5.859		ksps
DC Accuracy						
DNL ^[5]	Differential Nonlinearity	For any configuration	-1		+2	LSB
INL	Integral Nonlinearity	For any configuration	-2		+2	LSB
Eoffset	Offset Error		0	15	90	mV
I_{ADC}	Operating Current			275	350	μA
F_{CLK}	Data Clock	Source is chip's internal main oscillator. See device data sheet for accuracy.	2.25		12	MHz
PSRR	Power Supply Rejection Ration					
	PSRR ($V_{\text{dd}} > 3.0\text{V}$)			24	dB	
	PSRR ($2.2 < V_{\text{dd}} < 3.0$)			30	dB	
	PSRR ($2.0 < V_{\text{dd}} < 2.2$)			12	dB	
	PSRR ($V_{\text{dd}} < 2.0$)			0	dB	
Egain	Gain Error	For any resolution	1		5	%FSR
R_{IN}	Input Resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution.	$1 / (500\text{fF} * \text{Data-Clock})$	$1 / (400\text{fF} * \text{Data-Clock})$	$1 / (300\text{fF} * \text{Data-Clock})$	Ω

Note

5. Monotonicity is not guaranteed.

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 25. AC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F _{CPU}	CPU Frequency		5.7	–	25.2	MHz
F _{32K1}	Internal Low Speed Oscillator Frequency		19	32	50	kHz
F _{IMO24}	Internal Main Oscillator Frequency at 24 MHz Setting		22.8	24	25.2	MHz
F _{IMO12}	Internal Main Oscillator Frequency at 12 MHz Setting		11.4	12	12.6	MHz
F _{IMO6}	Internal Main Oscillator Frequency at 6 MHz Setting		5.7	6.0	6.3	MHz
DC _{IMO}	Duty Cycle of IMO		40	50	60	%
T _{RAMP}	Supply Ramp Time		20	–	–	μs
T _{XRST}	External Reset Pulse Width at Power Up	After supply voltage is valid	1			ms
T _{XRST2}	External Reset Pulse Width after Power Up ^[10]	Applies after part has booted	10			μs

Note

10. The minimum required XRES pulse length is longer when programming the device (see [Table 32 on page 28](#)).

Table 27.AC Characteristics – USB Data Timings

Symbol	Description	Conditions	Min	Typ	Max	Units
Td _{rate}	Full speed data rate	Average bit rate	12–0.25%	12	12 + 0.25%	MHz
Td _{j1}	Receiver data jitter tolerance	To next transition	-18.5	–	18.5	ns
Td _{j2}	Receiver data jitter tolerance	To pair transition	-9	–	9	ns
Tud _{j1}	Driver differential jitter	To next transition	-3.5	–	3.5	ns
Tud _{j2}	Driver differential jitter	To pair transition	-4.0	–	4.0	ns
Tf _{deop}	Source jitter for differential transition	To SE0 transition	-2	–	5	ns
Tf _{eopt}	Source SE0 interval of EOP		160	–	175	ns
Tf _{eopr}	Receiver SE0 interval of EOP		82	–		ns
Tf _{st}	Width of SE0 interval during differential transition			–	14	ns

Table 28.AC Characteristics – USB Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time	50 pF	4	–	20	ns
Tf	Transition fall time	50 pF	4	–	20	ns
TR	Rise/fall time matching		90.00	–	111.1	%
V _{crs}	Output signal crossover voltage		1.3	–	2.0	V

AC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 29. AC Low Power Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T _{LPC}	Comparator Response Time, 50 mV Overdrive	50 mV overdrive does not include offset voltage.			100	ns

AC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 30. AC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F _{SW}	Switch Rate	Maximum pin voltage when measuring switch rate is 1.8Vp-p	–	–	6.3	MHz

AC External Clock Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 31. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F _{OSCEXT}	Frequency		0.750	–	25.2	MHz
–	High Period		20.6	–	5300	ns
–	Low Period		20.6	–	–	ns
–	Power Up IMO to Switch		150	–	–	μs

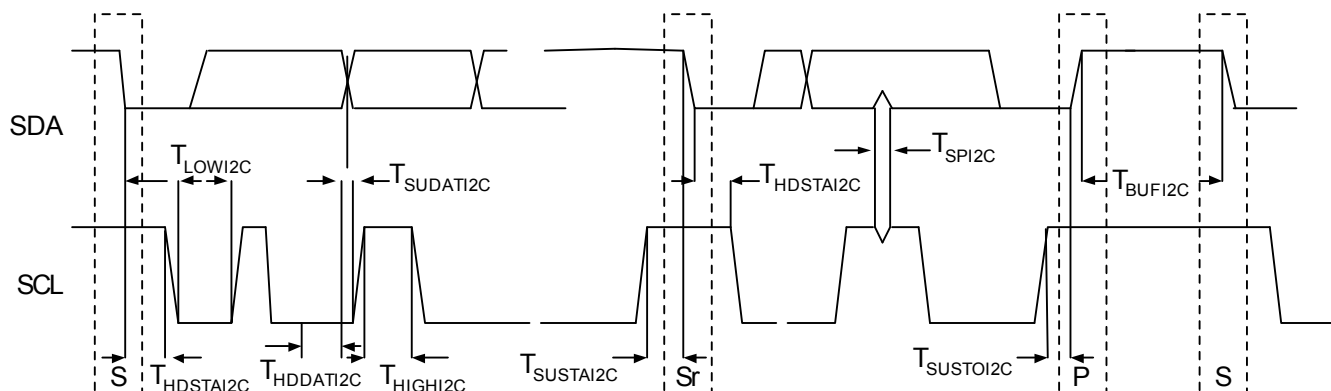
AC I2C Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 33. AC Characteristics of the I2C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
$F_{SCL I2C}$	SCL Clock Frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	—	0.6	—	μ s
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	—	1.3	—	μ s
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	—	0.6	—	μ s
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	—	0.6	—	μ s
$T_{HDDATI2C}$	Data Hold Time	0	—	0	—	μ s
$T_{SUDATI2C}$	Data Setup Time	250	—	100 ^[11]	—	ns
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	—	0.6	—	μ s
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	—	1.3	—	μ s
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	—	—	0	50	ns

Figure 14. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note

11. A Fast-Mode I2C-bus device can be used in a Standard Mode I2C-bus system, but the requirement $t_{SU,DAT} \geq 250$ ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU,DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Figure 18. 48-Pin (300 MIL) SSOP

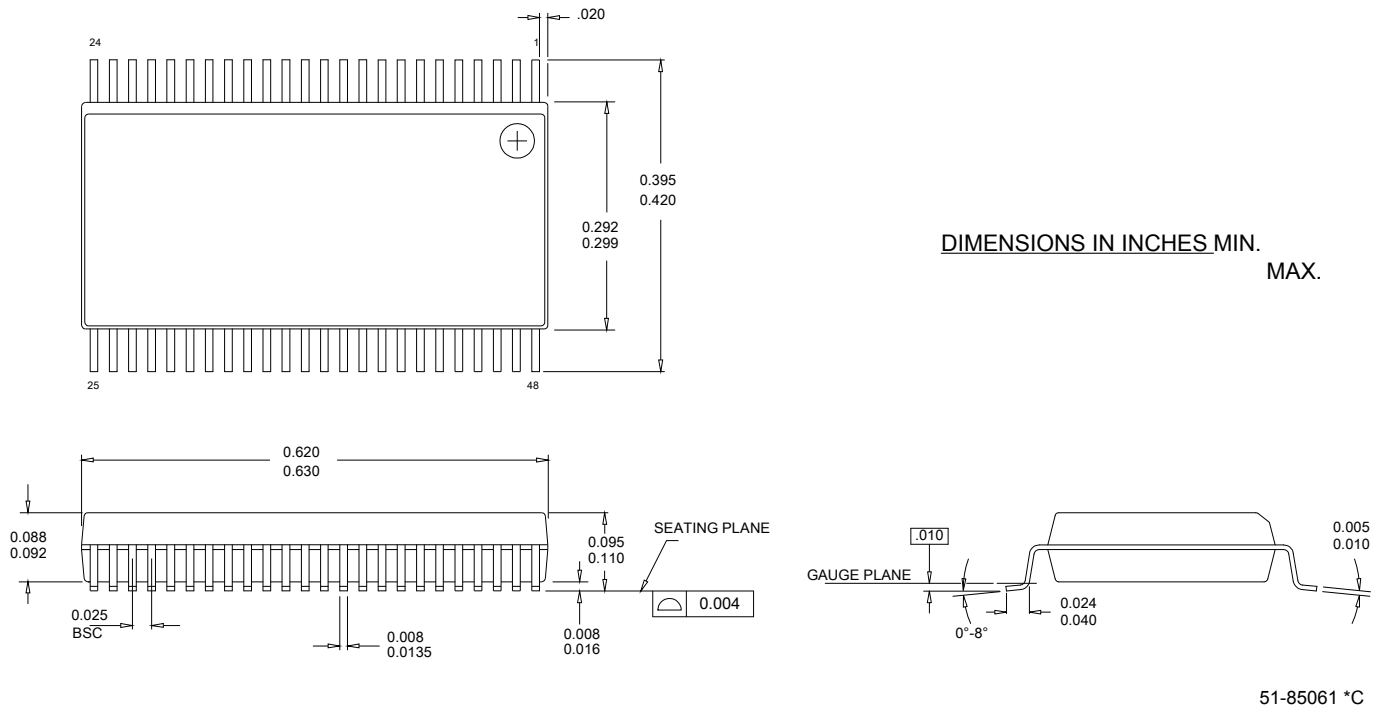
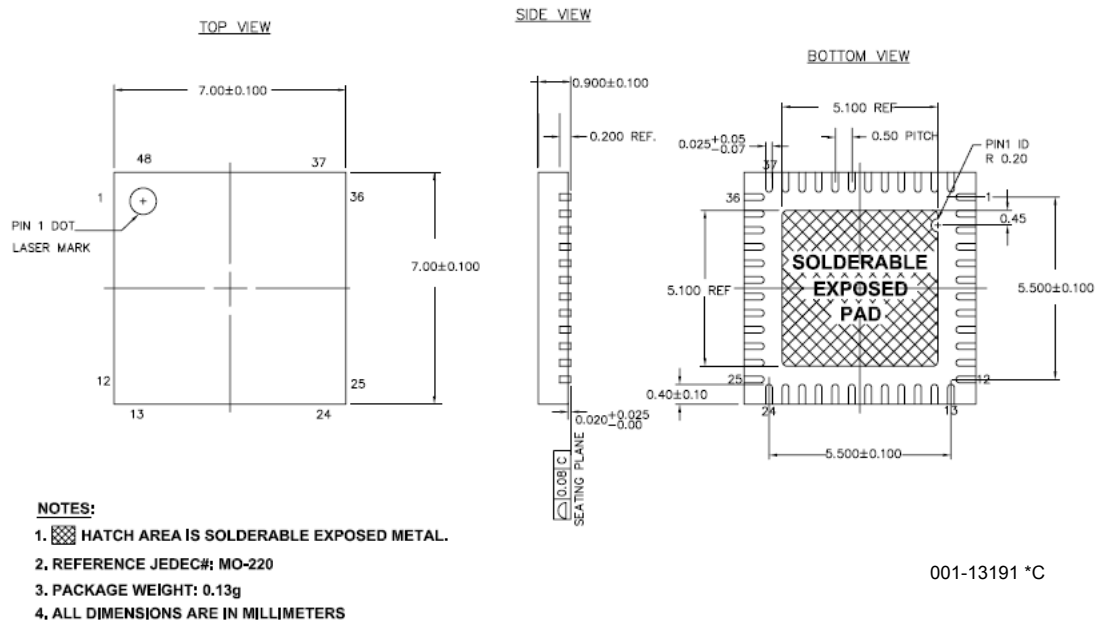


Figure 19. 48-Pin (7x7 mm) QFN



Important Notes

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.
- Pinned vias for thermal conduction are not required for the low power PSoC device.

Ordering Information

The following table lists the CY8C20x36/46/66/96 PSoC devices' key package features and ordering codes.

Table 39. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	CapSense Blocks	Digital I/O Pins	Analog Inputs ^[18]	XRES Pin	USB
16-Pin (3x3x0.6mm) QFN	CY8C20236-24LKXI	8K	1K	1	13	13	Yes	No
16-Pin (3x3x0.6mm) QFN (Tape and Reel)	CY8C20236-24LKXIT	8K	1K	1	13	13	Yes	No
16 Pin (3x3 x 0.6 mm) QFN	CY8C20246-24LKXI	16K	2K	1	13	13	Yes	No
16 Pin (3x3 x 0.6 mm) QFN (Tape and Reel)	CY8C20246-24LKXIT	16K	2K	1	13	13	Yes	No
24-Pin (4x4x0.6mm) QFN	CY8C20336-24LQXI	8K	1K	1	20	20	Yes	No
24-Pin (4x4x0.6mm) QFN (Tape and Reel)	CY8C20336-24LQXIT	8K	1K	1	20	20	Yes	No
24 Pin (4x4 x 0.6 mm) QFN	CY8C20346-24LQXI	16K	2K	1	20	20	Yes	No
24 Pin (4x4 x 0.6 mm) QFN (Tape and Reel)	CY8C20346-24LQXIT	16K	2K	1	20	20	Yes	No
24-Pin (4x4x0.6mm) QFN	CY8C20396-24LQXI	16K	2K	1	19	19	Yes	Yes
24-Pin (4x4x0.6mm) QFN (Tape and Reel)	CY8C20396-24LQXIT	16K	2K	1	19	19	Yes	Yes
32-Pin (5x5x0.6mm) QFN	CY8C20436-24LQXI	8K	1K	1	28	28	Yes	No
32-Pin (5x5x0.6mm) QFN (Tape and Reel)	CY8C20436-24LQXIT	8K	1K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20446-24LQXI	16K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20446-24LQXIT	16K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20466-24LQXI	32K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20466-24LQXIT	32K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20496-24LQXI	16K	2K	1	25	25	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20496-24LQXIT	16K	2K	1	25	25	Yes	No
48-Pin SSOP	CY8C20536-24PVXI	8K	1K	1	36	36	Yes	No
48-Pin SSOP (Tape and Reel)	CY8C20536-24PVXIT	8K	1K	1	36	36	Yes	No
48-Pin SSOP	CY8C20546-24PVXI	16K	2K	1	36	36	Yes	No
48-Pin SSOP (Tape and Reel)	CY8C20546-24PVXIT	16K	2K	1	36	36	Yes	No
48-Pin SSOP	CY8C20566-24PVXI	32K	2K	1	36	36	Yes	No
48-Pin SSOP (Tape and Reel)	CY8C20566-24PVXIT	32K	2K	1	36	36	Yes	No
48 Pin (7x7 mm) QFN	CY8C20636-24LTXI	8K	1K	1	36	36	Yes	No
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20636-24LTXIT	8K	1K	1	36	36	Yes	No
48 Pin (7x7 mm) QFN	CY8C20646-24LTXI	16K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20646-24LTXIT	16K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN	CY8C20666-24LTXI	32K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20666-24LTXIT	32K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN (OCD) ^[4]	CY8C20066-24LTXI	32K	2K	1	36	36	Yes	Yes

Notes

18. Dual-function Digital I/O Pins also connect to the common analog mux.

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