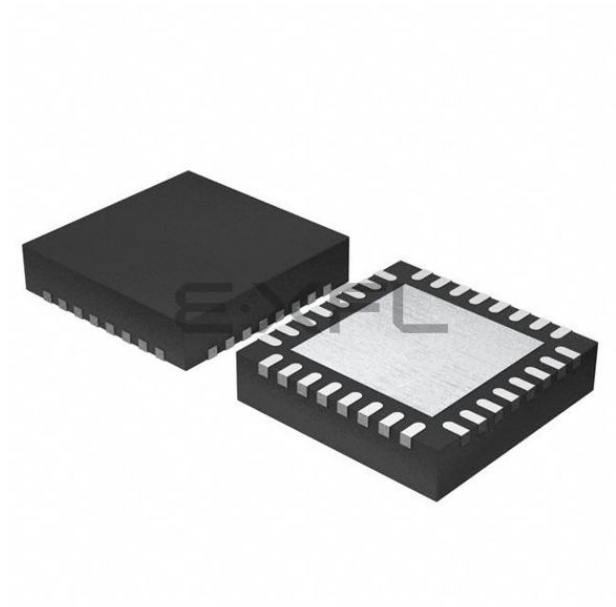

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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (16kB)
Controller Series	CY8C20xx6
RAM Size	2K x 8
Interface	I²C, SPI
Number of I/O	28
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20446-24lqxit

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select Components
2. Configure Components
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

Both the system-level and chip-level views provide a library of pre-built, pre-tested hardware peripheral components. In the system-level view these components are called “drivers” and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces (I^2C-bus, for example), and the logic to control how they interact with one another (called valuators).

In the chip-level view the components are called “user modules.” User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and programmable system-on-chip varieties.

Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins, or connect system-level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view selecting a potentiometer driver to control a variable speed fan driver and setting up the valuators to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog-to-digital converter (ADC) to convert the potentiometer’s output to a digital signal, and a PWM to control the fan.

In the chip-level view, you perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed. The system-level design also generates a C main() program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s Debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Pinouts

The CY8C20x36/46/66/96 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O and connection to the common analog bus. However, Vss, Vdd, and XRES are not capable of Digital I/O.

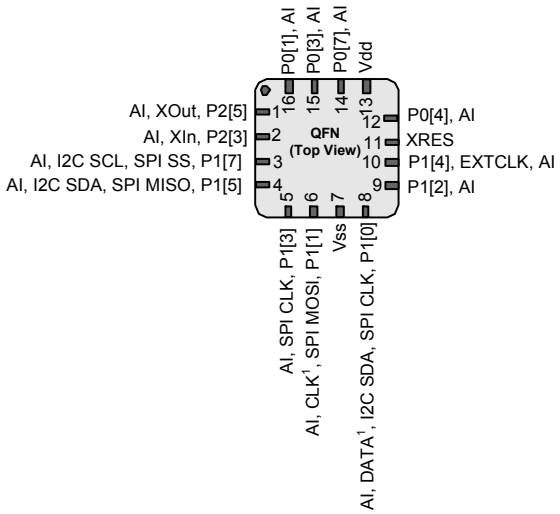
16-Pin QFN (No E-Pad)

Table 2. Pin Definitions - CY8C20236, CY8C20246 PSoC Device [2]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	IOHR	I	P1[7]	I2C SCL, SPI SS
4	IOHR	I	P1[5]	I2C SDA, SPI MISO
5	IOHR	I	P1[3]	SPI CLK
6	IOHR	I	P1[1]	ISSP CLK[1], I2C SCL, SPI MOSI
7	Power		Vss	Ground connection
8	IOHR	I	P1[0]	ISSP DATA[1], I2C SDA, SPI CLK
9	IOHR	I	P1[2]	
10	IOHR	I	P1[4]	Optional external clock (EXTCLK)
11	Input		XRES	Active high external reset with internal pull down
12	IOH	I	P0[4]	
13	Power		Vdd	Supply voltage
14	IOH	I	P0[7]	
15	IOH	I	P0[3]	Integrating input
16	IOH	I	P0[1]	Integrating input

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 2. CY8C20236, CY8C20246 PSoC Device



Notes
1. These are the ISSP pins, which are not High Z at POR (Power On Reset).
2. During power up or reset event, device P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter any issues.

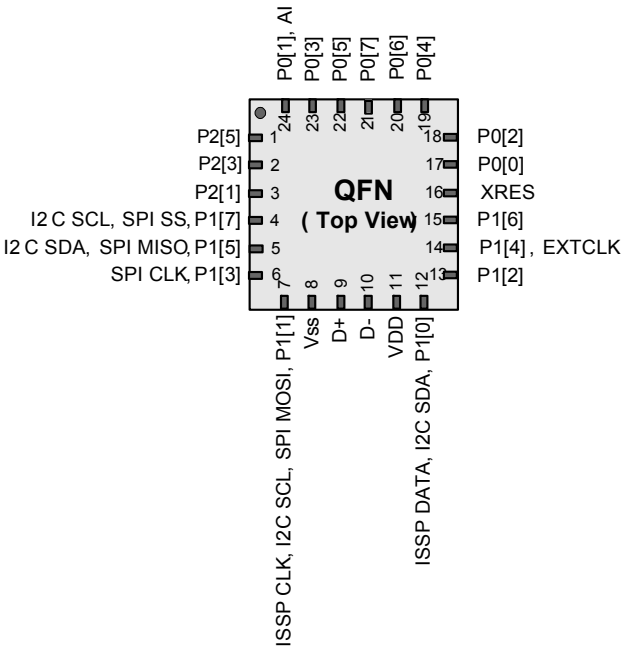
24-Pin QFN with USB

Table 4. Pin Definitions - CY8C20396 PSoC Device [2, 3]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	
2	I/O	I	P2[3]	
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I2C SCL, SPI SS
5	IOHR	I	P1[5]	I2C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK, I2C SCL, SPI MOSI
8	Power		VSS	Ground
9	I/O	I	D+	USB D+
10	I/O	I	D-	USB D-
11	Power		VDD	Supply
12	IOHR	I	P1[0]	ISSP DATA, I2C SDA
13	IOHR	I	P1[2]	
14	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
15	IOHR	I	P1[6]	
16	RESET INPUT		XRES	Active high external reset with internal pull down
17	IOH	I	P0[0]	
18	IOH	I	P0[2]	
19	IOH	I	P0[4]	
20	IOH	I	P0[6]	
21	IOH	I	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input
24	IOH	I	P0[1]	Integrating input
CP	Power		VSS	Thermal pad must be connected to Ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Figure 4. CY8C20396 PSoC Device



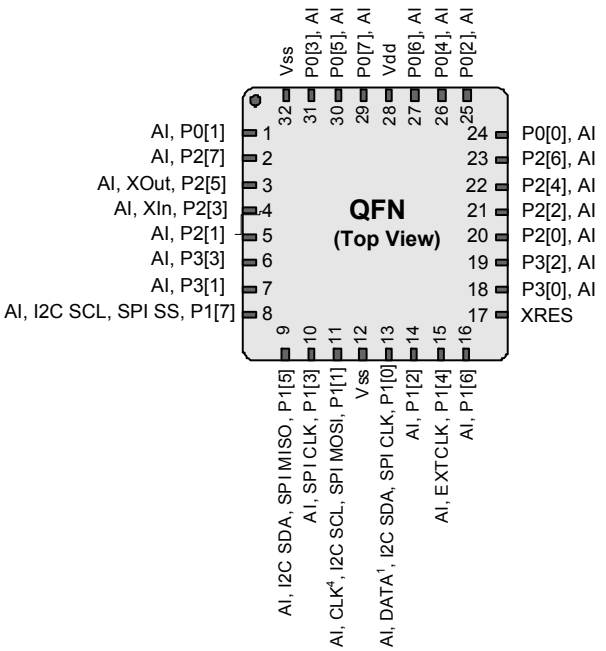
32-Pin QFN

Table 5. Pin Definitions - CY8C20436, CY8C20446, CY8C20466 PSoC Device [2, 3]

Pin No.	Type		Name	Description
	Digital	Analog		
1	IOH	I	P0[1]	Integrating input
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	IOHR	I	P1[7]	I2C SCL, SPI SS
9	IOHR	I	P1[5]	I2C SDA, SPI MISO
10	IOHR	I	P1[3]	SPI CLK.
11	IOHR	I	P1[1]	ISSP CLK[1], I2C SCL, SPI MOSI.
12	Power		Vss	Ground connection.
13	IOHR	I	P1[0]	ISSP DATA[1], I2C SDA., SPI CLK
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	IOH	I	P0[0]	
25	IOH	I	P0[2]	
26	IOH	I	P0[4]	
27	IOH	I	P0[6]	
28	Power		Vdd	Supply voltage
29	IOH	I	P0[7]	
30	IOH	I	P0[5]	
31	IOH	I	P0[3]	Integrating input
32	Power		Vss	Ground connection
CP	Power		Vss	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 5. CY8C20436, CY8C20446, CY8C20466 PSoC Device

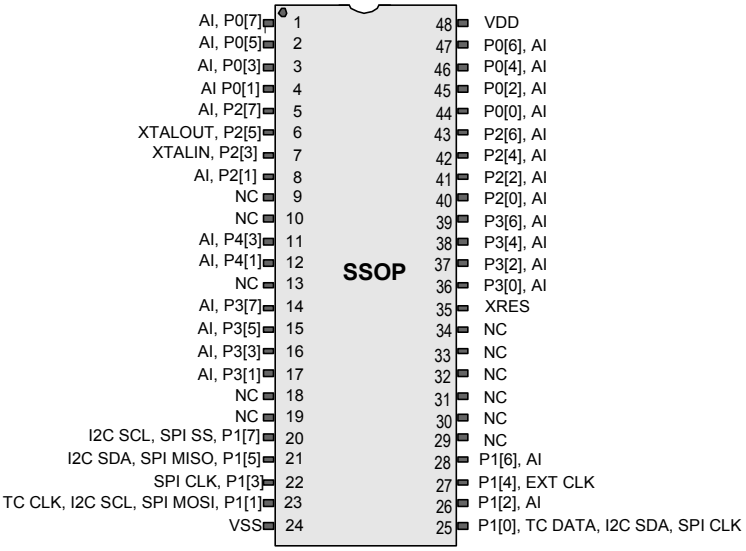


48-Pin SSOP

Table 7. Pin Definitions - CY8C20536, CY8C20546, and CY8C20566 PSoC Device[2]

Pin No.	Digital	Analog	Name	Description
1	IOH	I	P0[7]	
2	IOH	I	P0[5]	
3	IOH	I	P0[3]	
4	IOH	I	P0[1]	
5	I/O	I	P2[7]	
6	I/O	I	P2[5]	XTAL Out
7	I/O	I	P2[3]	XTAL In
8	I/O	I	P2[1]	
9			NC	No connection
10			NC	No connection
11	I/O	I	P4[3]	
12	I/O	I	P4[1]	
13			NC	No connection
14	I/O	I	P3[7]	
15	I/O	I	P3[5]	
16	I/O	I	P3[3]	
17	I/O	I	P3[1]	
18			NC	No connection
19			NC	No connection
20	IOHR	I	P1[7]	I2C SCL, SPI SS
21	IOHR	I	P1[5]	I2C SDA, SPI MISO
22	IOHR	I	P1[3]	SPI CLK
23	IOHR	I	P1[1]	TC CLK[1], I2C SCL, SPI MOSI
24			VSS	Ground Pin
25	IOHR	I	P1[0]	TC DATA[1], I2C SDA, SPI CLK
26	IOHR	I	P1[2]	
27	IOHR	I	P1[4]	EXT CLK
28	IOHR	I	P1[6]	
29			NC	No connection
30			NC	No connection
31			NC	No connection
32			NC	No connection
33			NC	No connection
34			NC	No connection
35			XRES	Active high external reset with internal pull down
36	I/O	I	P3[0]	
37	I/O	I	P3[2]	
38	I/O	I	P3[4]	
39	I/O	I	P3[6]	
40	I/O	I	P2[0]	
41	I/O	I	P2[2]	
42	I/O	I	P2[4]	
43	I/O	I	P2[6]	
44	IOH	I	P0[0]	
45	IOH	I	P0[2]	
46	IOH	I	P0[4]	
47	IOH	I	P0[6]	
48	Power		Vdd	Power Pin

Figure 6. CY8C20536, CY8C20546, and CY8C20566 PSoC Device



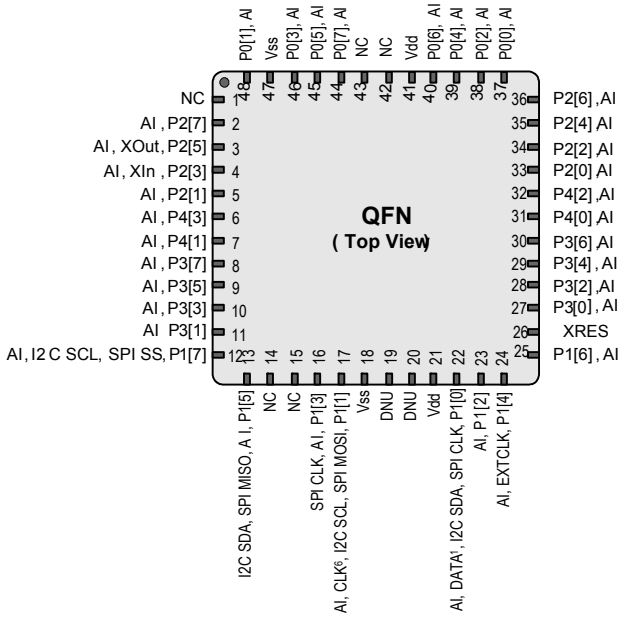
LEGEND A = Analog, I = Input, O = Output, NC = No Connection, H = 5 mA High Output Drive, R = Regulated Output Option.

48-Pin QFN

Table 8. Pin Definitions - CY8C20636 PSoC Device [2, 3]

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I2C SCL, SPI SS
13	IOHR	I	P1[5]	I2C SDA, SPI MISO
14			NC	No connection
15			NC	No connection
16	IOHR	I	P1[3]	SPI CLK
17	IOHR	I	P1[1]	ISSP CLK[1], I2C SCL, SPI MOSI
18	Power		Vss	Ground connection
19			DNU	
20			DNU	
21	Power		Vdd	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA[1], I2C SDA, SPI CLK
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		Vdd	Supply voltage
42			NC	No connection
43			NC	No connection
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		Vss	Ground connection
48	IOH	I	P0[1]	
CP	Power		Vss	Center pad must be connected to ground

Figure 7. CY8C20636 PSoC Device



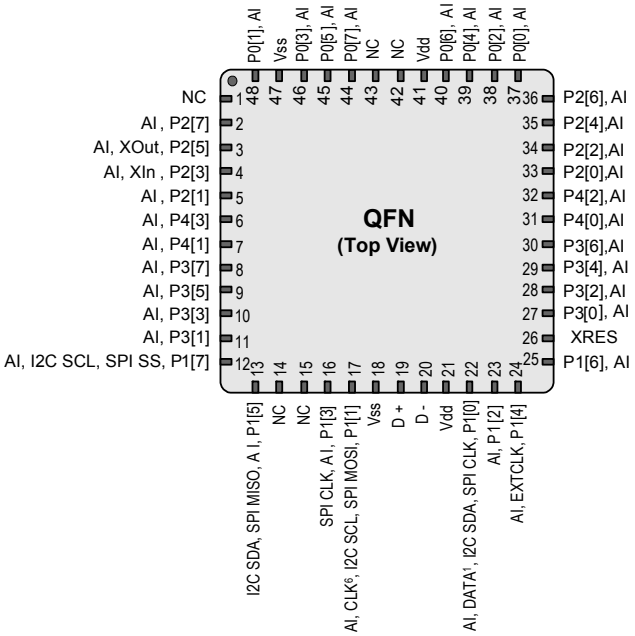
LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

48-Pin QFN with USB

Table 9. Pin Definitions - CY8C20646, CY8C20666 PSoC Device [2, 3]

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I2C SCL, SPI SS
13	IOHR	I	P1[5]	I2C SDA, SPI MISO
14			NC	No connection
15			NC	No connection
16	IOHR	I	P1[3]	SPI CLK
17	IOHR	I	P1[1]	ISSP CLK[1], I2C SCL, SPI MOSI
18	Power		Vss	Ground connection
19	I/O		D+	USB D+
20	I/O		D-	USB D-
21	Power		Vdd	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA[1], I2C SDA, SPI CLK
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	

Figure 8. CY8C20646, CY8C20666 PSoC Device



Pin No.	Digital	Analog	Name	Description
40	IOH	I	P0[6]	
41	Power		Vdd	Supply voltage
42			NC	No connection
43			NC	No connection
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		Vss	Ground connection
48	IOH	I	P0[1]	
CP	Power		Vss	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 12. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage Temperature	Higher storage temperatures reduces data retention time. Recommended Storage Temperature is +25°C ± 25°C. Extended duration storage temperatures above 85°C degrades reliability.	–55	+25	+125	°C
Vdd	Supply Voltage Relative to Vss		–0.5	–	+6.0	V
V_{IO}	DC Input Voltage		Vss – 0.5	–	Vdd + 0.5	V
V_{IOZ}	DC Voltage Applied to Tri-state		Vss –0.5	–	Vdd + 0.5	V
I_{MIO}	Maximum Current into any Port Pin		–25	–	+50	mA
ESD	Electro Static Discharge Voltage	Human Body Model ESD	2000	–	–	V
LU	Latch up Current	In accordance with JESD78 standard	–	–	200	mA

Operating Temperature

Table 13. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_A	Ambient Temperature		–40	–	+85	°C
T_J	Operational Die Temperature	The temperature rise from ambient to junction is package specific. Refer the table Thermal Impedances per Package on page 34. The user must limit the power consumption to comply with this requirement.	–40	–	+100	°C

Table 17. 1.71V to 2.4V DC GPIO Specifications *(continued)*

Symbol	Description	Conditions	Min	Typ	Max	Units
V_H	Input Hysteresis Voltage		–	80	–	mV
I_{IL}	Input Leakage (Absolute Value)		–	0.001	1	µA
C_{PIN}	Capacitive Load on Pins	Package and pin dependent Temp = 25°C	0.5	1.7	5	pF

Table 18.DC Characteristics – USB Interface

Symbol	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ Pull Up Resistance	With idle bus	0.900	-	1.575	kΩ
Rusba	USB D+ Pull Up Resistance	While receiving traffic	1.425	-	3.090	kΩ
Vohusb	Static Output High		2.8	-	3.6	V
Volusb	Static Output Low			-	0.3	V
Vdi	Differential Input Sensitivity		0.2	-		V
Vcm	Differential Input Common Mode Range		0.8	-	2.5	V
Vse	Single Ended Receiver Threshold		0.8	-	2.0	V
Cin	Transceiver Capacitance			-	50	pF
Iio	Hi-Z State Data Line Leakage	On D+ or D- line	-10	-	+10	µA
Rps2	PS/2 Pull Up Resistance		3	5	7	kΩ
Rext	External USB Series Resistor	In series with each USB pin	21.78	22.0	22.22	Ω

DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. DC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{SW}	Switch Resistance to Common Analog Bus		–	–	800	Ω
R_{GND}	Resistance of Initialization Switch to Vss		–	–	800	Ω

The maximum pin voltage for measuring R_{SW} and R_{GND} is 1.8V

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 20. DC Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{LPC}	Low Power Comparator (LPC) common mode	Maximum voltage limited to Vdd	0.0	–	1.8	V
I_{LPC}	LPC supply current		–	10	40	µA
V_{OSLPC}	LPC voltage offset		–	2.5	30	mV

Comparator User Module Electrical Specifications

The following table lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: –40°C <= TA <= 85°C, 1.71V <= Vdd <= 5.5V.

Table 21. Comparator User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{COMP}	Comparator Response Time	50 mV overdrive		70	100	ns
Offset				2.5	30	mV
Current		Average DC current, 50 mV overdrive		20	80	µA
PSRR	Supply voltage >2V	Power Supply Rejection Ratio		80		dB
	Supply voltage <2V	Power Supply Rejection Ratio		40		dB
Input Range			0		1.5	V

ADC Electrical Specifications

Table 22. ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input Voltage Range	This gives 72% of maximum code	Vss		1.3	V
C_{IN}	Input Capacitance				5	pF
RES	Resolution	Settings 8, 9, or 10	8		10	Bits
S8	8-Bit Sample Rate	Data Clock set to 6 MHz. Sample Rate = 0.001/ (2^Resolution/Data clock)		23.4375		ksps
S10	10-Bit Sample Rate	Data Clock set to 6 MHz. Sample Rate = 0.001/ (2^Resolution/Data clock)		5.859		ksps
DC Accuracy						
DNL[5]	Differential Nonlinearity	For any configuration	-1		+2	LSB
INL	Integral Nonlinearity	For any configuration	-2		+2	LSB
Eoffset	Offset Error		0	15	90	mV
I_{ADC}	Operating Current			275	350	µA
F_{CLK}	Data Clock	Source is chip's internal main oscillator. See device data sheet for accuracy.	2.25		12	MHz
PSRR	Power Supply Rejection Ration					
	PSRR (Vdd>3.0V)			24	dB	
	PSRR (2.2 < Vdd < 3.0)			30	dB	
	PSRR (2.0 < Vdd < 2.2)			12	dB	
	PSRR (Vdd < 2.0)			0	dB	
Egain	Gain Error	For any resolution	1		5	%FSR
R_{IN}	Input Resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution.	1/(500fF* Data-Clock)	1/(400fF* Data-Clock)	1/(300fF* Data-Clock)	Ω

Note
5. Monotonicity is not guaranteed.

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 25. AC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{CPU}	CPU Frequency		5.7	–	25.2	MHz
F_{32K1}	Internal Low Speed Oscillator Frequency		19	32	50	kHz
F_{IMO24}	Internal Main Oscillator Frequency at 24 MHz Setting		22.8	24	25.2	MHz
F_{IMO12}	Internal Main Oscillator Frequency at 12 MHz Setting		11.4	12	12.6	MHz
F_{IMO6}	Internal Main Oscillator Frequency at 6 MHz Setting		5.7	6.0	6.3	MHz
DC_{IMO}	Duty Cycle of IMO		40	50	60	%
T_{RAMP}	Supply Ramp Time		20	–	–	µs
T_{XRST}	External Reset Pulse Width at Power Up	After supply voltage is valid	1			ms
T_{XRST2}	External Reset Pulse Width after Power Up[10]	Applies after part has booted	10			µs

Note
10. The minimum required XRES pulse length is longer when programming the device (see Table 32 on page 28).

AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 26. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO Operating Frequency	Normal Strong Mode Port 0, 1	0 0	– –	6 MHz for 1.71V<Vdd<2.4V 12 MHz for 2.4V<Vdd<5.5V	MHz
TRise23	Rise Time, Strong Mode, Cload = 50 pF Ports 2 or 3	Vdd = 3.0 to 3.6V, 10% – 90%	15	–	80	ns
TRise23L	Rise Time, Strong Mode Low Supply, Cload = 50 pF, Ports 2 or 3	Vdd = 1.71 to 3.0V, 10% – 90%	15	–	80	ns
TRise01	Rise Time, Strong Mode, Cload = 50 pF Ports 0 or 1	Vdd = 3.0 to 3.6V, 10% – 90% LDO enabled or disabled	10	–	50	ns
TRise01L	Rise Time, Strong Mode Low Supply, Cload = 50 pF, Ports 0 or 1	Vdd = 1.71 to 3.0V, 10% – 90% LDO enabled or disabled	10	–	80	ns
TFall	Fall Time, Strong Mode, Cload = 50 pF All Ports	Vdd = 3.0 to 3.6V, 10% – 90%	10	–	50	ns
TFallL	Fall Time, Strong Mode Low Supply, Cload = 50 pF, All Ports	Vdd = 1.71 to 3.0V, 10% – 90%	10	–	70	ns

Figure 12. GPIO Timing Diagram

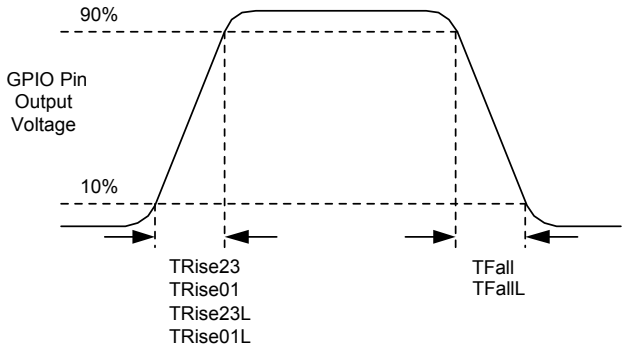


Table 27.AC Characteristics – USB Data Timings

Symbol	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full speed data rate	Average bit rate	12–0.25%	12	12 + 0.25%	MHz
Tdjr1	Receiver data jitter tolerance	To next transition	-18.5	–	18.5	ns
Tdjr2	Receiver data jitter tolerance	To pair transition	-9	–	9	ns
Tudj1	Driver differential jitter	To next transition	-3.5	–	3.5	ns
Tudj2	Driver differential jitter	To pair transition	-4.0	–	4.0	ns
Tfdeop	Source jitter for differential transition	To SE0 transition	-2	–	5	ns
Tfeopt	Source SE0 interval of EOP		160	–	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	–		ns
Tfst	Width of SE0 interval during differential transition			–	14	ns

Table 28.AC Characteristics – USB Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time	50 pF	4	–	20	ns
Tf	Transition fall time	50 pF	4	–	20	ns
TR	Rise/fall time matching		90.00	–	111.1	%
Vcrs	Output signal crossover voltage		1.3	–	2.0	V

AC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 29. AC Low Power Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{LPC}	Comparator Response Time, 50 mV Overdrive	50 mV overdrive does not include offset voltage.			100	ns

AC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 30. AC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SW}	Switch Rate	Maximum pin voltage when measuring switch rate is 1.8Vp-p	–	–	6.3	MHz

AC External Clock Specifications

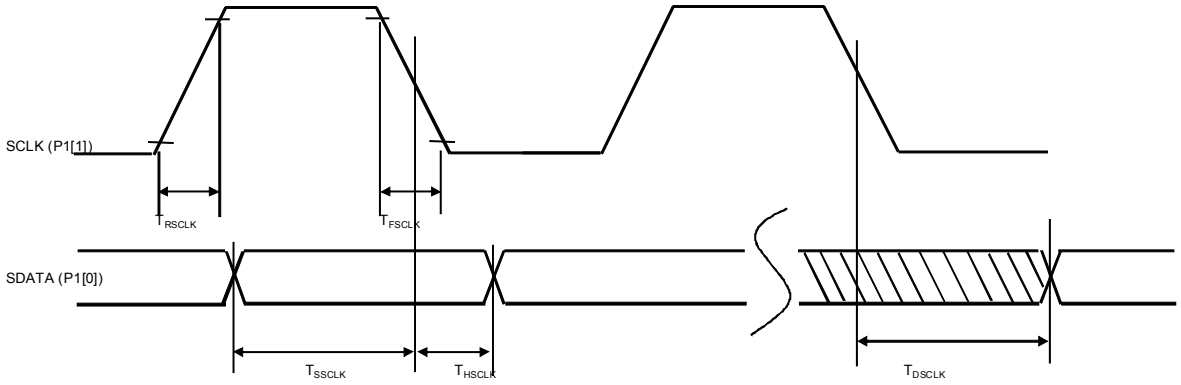
The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 31. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency		0.750	–	25.2	MHz
–	High Period		20.6	–	5300	ns
–	Low Period		20.6	–	–	ns
–	Power Up IMO to Switch		150	–	–	µs

AC Programming Specifications

Figure 13. AC Waveform



The following table lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 32. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{RSCLK}	Rise Time of SCLK		1	–	20	ns
T_{FSCLK}	Fall Time of SCLK		1	–	20	ns
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK		40	–	–	ns
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK		40	–	–	ns
F_{SCLK}	Frequency of SCLK		0	–	8	MHz
T_{ERASEB}	Flash Erase Time (Block)		–	–	18	ms
T_{WRITE}	Flash Block Write Time		–	–	25	ms
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	3.6 < Vdd	–	–	60	ns
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	3.0 ≤ Vdd ≤ 3.6	–	–	85	ns
T_{DSCLK2}	Data Out Delay from Falling Edge of SCLK	1.71 ≤ Vdd ≤ 3.0	–	–	130	ns
T_{XRST3}	External Reset Pulse Width after Power Up	Required to enter programming mode when coming out of sleep	263	–	–	µs

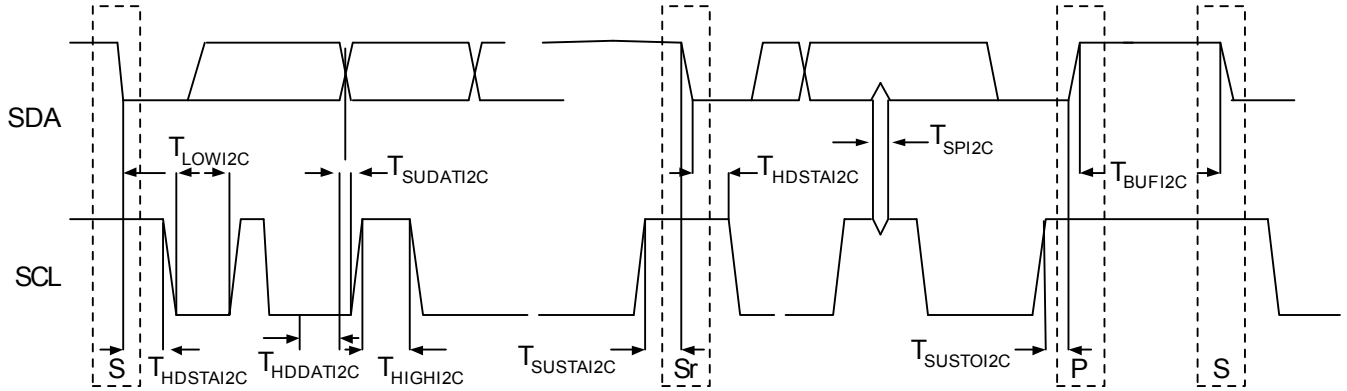
AC I2C Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 33. AC Characteristics of the I2C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs
$T_{SUDATI2C}$	Data Setup Time	250	–	100[11]	–	ns
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns

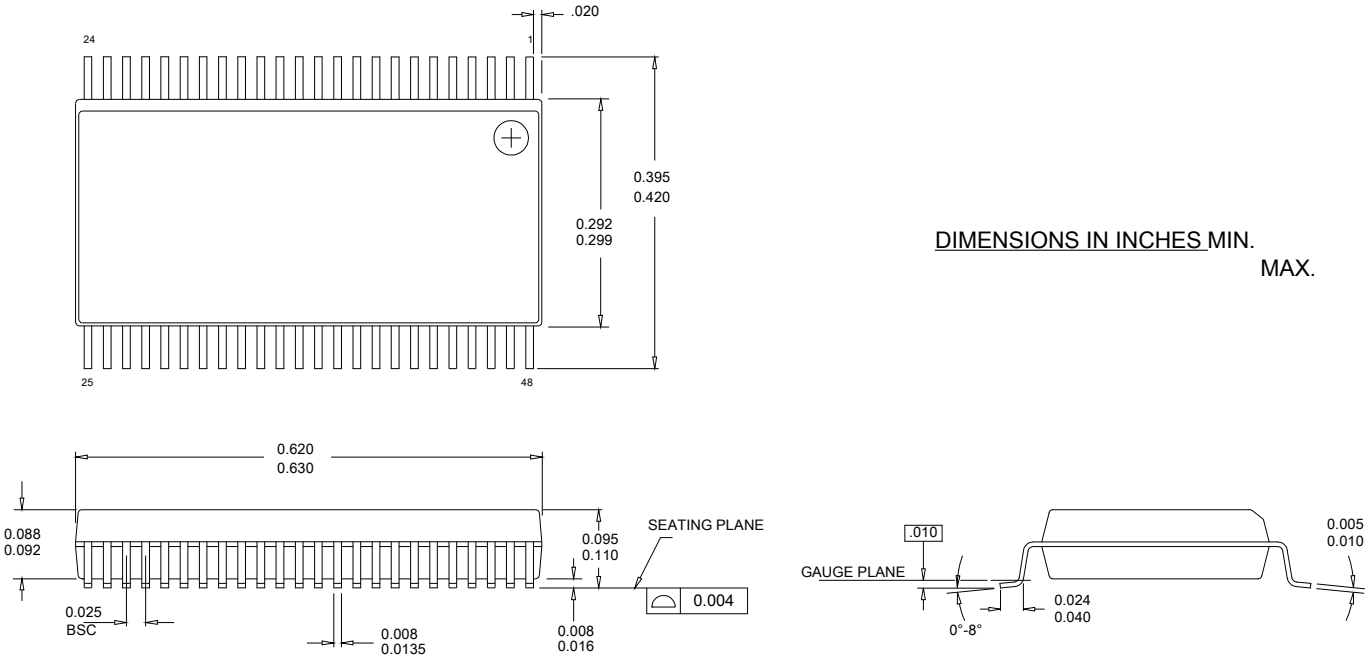
Figure 14. Definition for Timing for Fast/Standard Mode on the I^2C Bus



Note

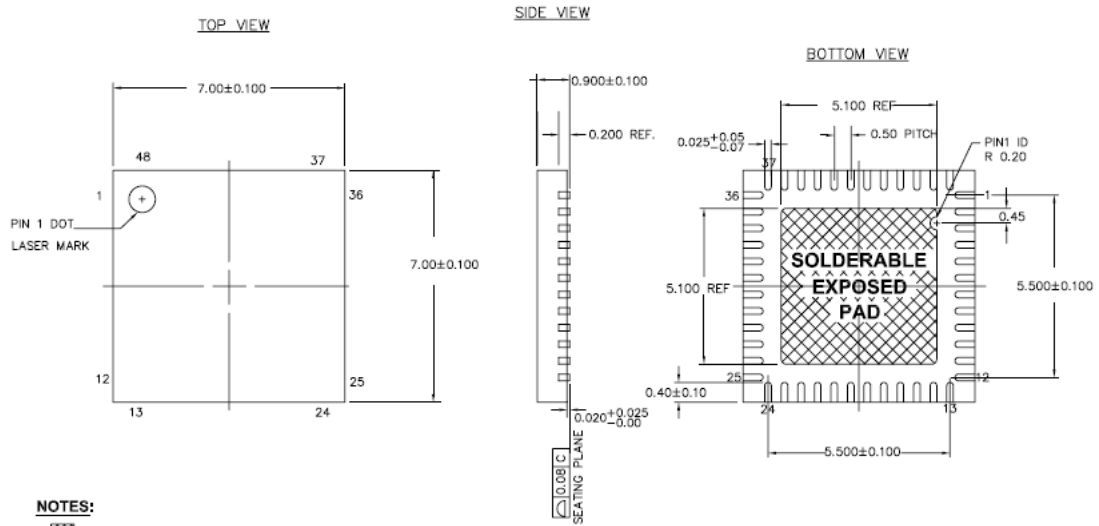
11. A Fast-Mode I2C-bus device can be used in a Standard Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Figure 18. 48-Pin (300 MIL) SSOP



51-85061 *C

Figure 19. 48-Pin (7x7 mm) QFN



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *C

Important Notes

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.
- Pinned vias for thermal conduction are not required for the low power PSoC device.

Thermal Impedances

Table 36. Thermal Impedances per Package

Package	Typical θ_{JA} [12]
16 QFN	32.69°C/W
24 QFN[13]	20.90°C/W
32 QFN[13]	19.51°C/W
48 SSOP	69°C/W
48 QFN[13]	17.68°C/W

Solder Reflow Peak Temperature

This table lists the minimum solder reflow peak temperature to achieve good solderability.

Table 37. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature[14]	Maximum Peak Temperature
16 QFN	240°C	260°C
24 QFN	240°C	260°C
32 QFN	240°C	260°C
48 SSOP	220°C	260°C
48 QFN	240°C	260°C

Notes
12. $T_J = T_A + \text{Power} \times \theta_{JA}$.
13. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.
14. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Development Tool Selection

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com/psocdesigner and includes a free C compiler.

PSoC Programmer

PSoC Programmer is flexible enough and is used on the bench in development and is also suitable for factory programming. PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of cost at http://www.cypress.com/psocprogrammer.

Development Kits

All development kits are sold at the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack

Ordering Information

The following table lists the CY8C20x36/46/66/96 PSoC devices' key package features and ordering codes.

Table 39. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	CapSense Blocks	Digital I/O Pins	Analog Inputs[18]	XRES Pin	USB
16-Pin (3x3x0.6mm) QFN	CY8C20236-24LKXI	8K	1K	1	13	13	Yes	No
16-Pin (3x3x0.6mm) QFN (Tape and Reel)	CY8C20236-24LKXIT	8K	1K	1	13	13	Yes	No
16 Pin (3x3 x 0.6 mm) QFN	CY8C20246-24LKXI	16K	2K	1	13	13	Yes	No
16 Pin (3x3 x 0.6 mm) QFN (Tape and Reel)	CY8C20246-24LKXIT	16K	2K	1	13	13	Yes	No
24-Pin (4x4x0.6mm) QFN	CY8C20336-24LQXI	8K	1K	1	20	20	Yes	No
24-Pin (4x4x0.6mm) QFN (Tape and Reel)	CY8C20336-24LQXIT	8K	1K	1	20	20	Yes	No
24 Pin (4x4 x 0.6 mm) QFN	CY8C20346-24LQXI	16K	2K	1	20	20	Yes	No
24 Pin (4x4 x 0.6 mm) QFN (Tape and Reel)	CY8C20346-24LQXIT	16K	2K	1	20	20	Yes	No
24-Pin (4x4x0.6mm) QFN	CY8C20396-24LQXI	16K	2K	1	19	19	Yes	Yes
24-Pin (4x4x0.6mm) QFN (Tape and Reel)	CY8C20396-24LQXIT	16K	2K	1	19	19	Yes	Yes
32-Pin (5x5x0.6mm) QFN	CY8C20436-24LQXI	8K	1K	1	28	28	Yes	No
32-Pin (5x5x0.6mm) QFN (Tape and Reel)	CY8C20436-24LQXIT	8K	1K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20446-24LQXI	16K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20446-24LQXIT	16K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20466-24LQXI	32K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20466-24LQXIT	32K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20496-24LQXI	16K	2K	1	25	25	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20496-24LQXIT	16K	2K	1	25	25	Yes	No
48-Pin SSOP	CY8C20536-24PVXI	8K	1K	1	36	36	Yes	No
48-Pin SSOP (Tape and Reel)	CY8C20536-24PVXIT	8K	1K	1	36	36	Yes	No
48-Pin SSOP	CY8C20546-24PVXI	16K	2K	1	36	36	Yes	No
48-Pin SSOP (Tape and Reel)	CY8C20546-24PVXIT	16K	2K	1	36	36	Yes	No
48-Pin SSOP	CY8C20566-24PVXI	32K	2K	1	36	36	Yes	No
48-Pin SSOP (Tape and Reel)	CY8C20566-24PVXIT	32K	2K	1	36	36	Yes	No
48 Pin (7x7 mm) QFN	CY8C20636-24LTXI	8K	1K	1	36	36	Yes	No
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20636-24LTXIT	8K	1K	1	36	36	Yes	No
48 Pin (7x7 mm) QFN	CY8C20646-24LTXI	16K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20646-24LTXIT	16K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN	CY8C20666-24LTXI	32K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20666-24LTXIT	32K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN (OCD)[4]	CY8C20066-24LTXI	32K	2K	1	36	36	Yes	Yes

Notes
18. Dual-function Digital I/O Pins also connect to the common analog mux.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

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