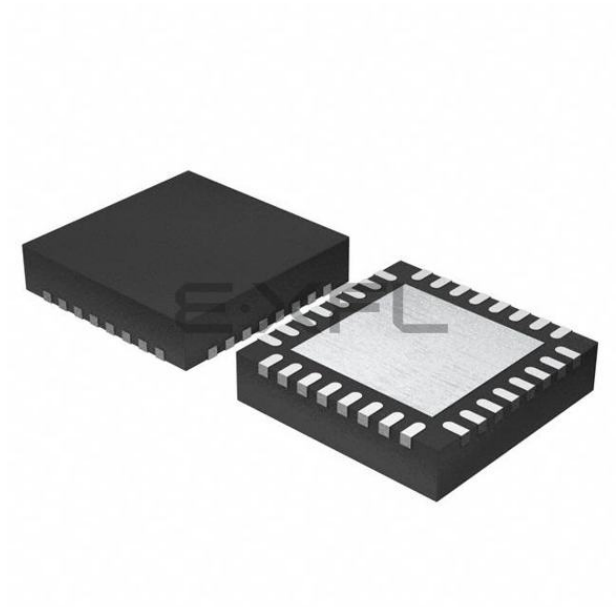


**Welcome to E-XFL.COM**

## Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

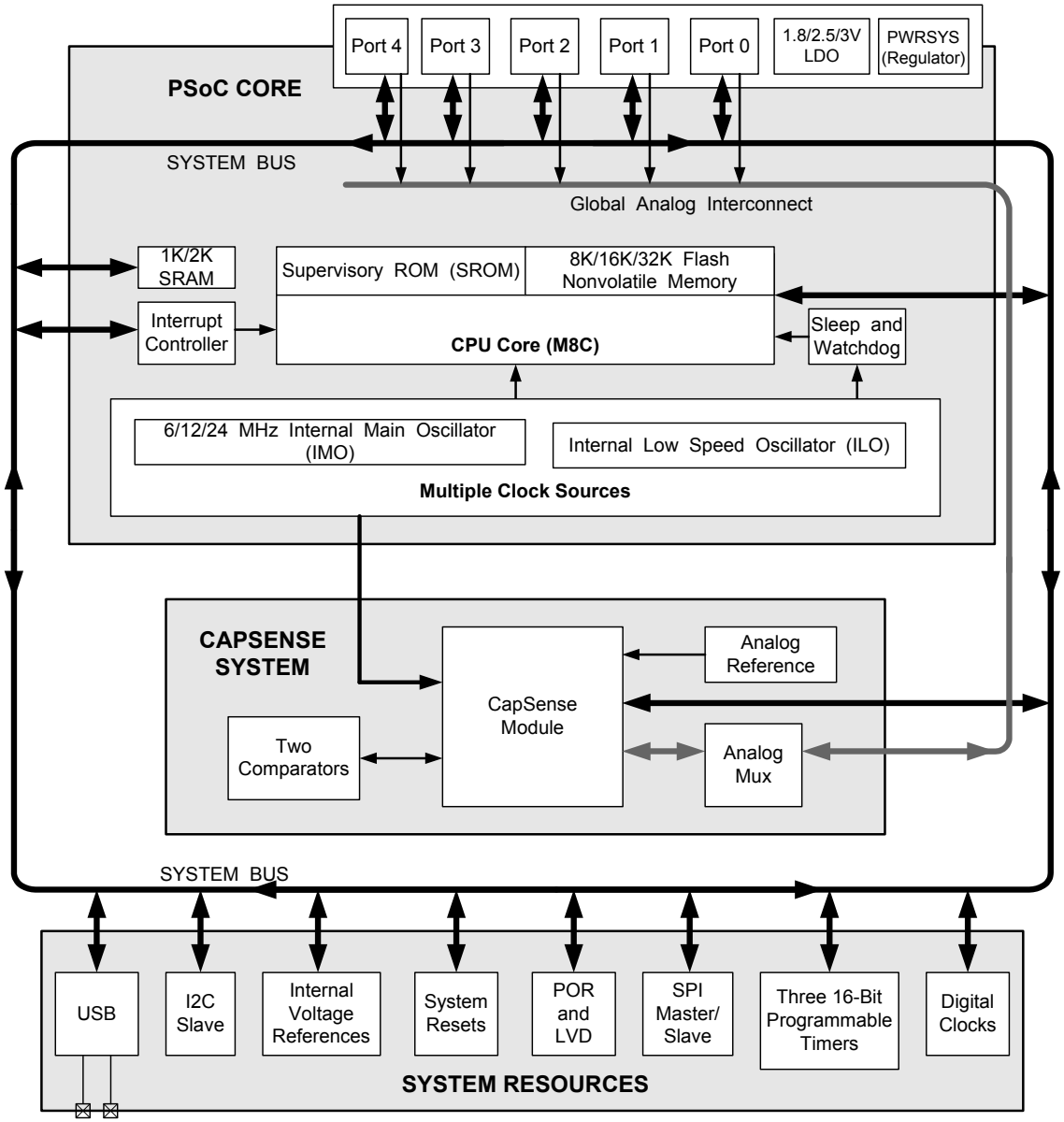
**Embedded - Microcontrollers - Application Specific** represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

## What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

| Details | |
|---|---|
| Product Status | Obsolete |
| Applications | Capacitive Sensing |
| Core Processor | M8C |
| Program Memory Type | FLASH (32kB) |
| Controller Series | CY8C20xx6 |
| RAM Size | 2K x 8 |
| Interface | I²C, SPI |
| Number of I/O | 28 |
| Voltage - Supply | 1.71V ~ 5.5V |
| Operating Temperature | -40°C ~ 85°C |
| Mounting Type | Surface Mount |
| Package / Case | 32-UFQFN Exposed Pad |
| Supplier Device Package | 32-QFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20466-24lqxi |

## Logic Block Diagram



### Additional System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The merits of each system resource are listed here:

- The I2C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I2C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power-On-Reset) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO.
- Standard Cypress PSoC IDE tools are available for debugging the CY8C20x36/46/66/96 family of parts. However, the additional trace length and a minimal ground plane in the Flex-Pod can create noise problems that make it difficult to debug the design. A custom bonded On-Chip Debug (OCD) device is available in an 48-pin QFN package. The OCD device is recommended for debugging designs that have high current and/or high analog accuracy requirements. The QFN package is compact and is connected to the ICE through a high density connector.

## Getting Started

The quickest way to understand PSoC silicon is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the PSoC® Programmable System-on-Chip™ Technical Reference Manual for CY8C20x36/46/66/96 PSoC Devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at www.cypress.com/psoc.

### Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located here: www.cypress.com/psoc. Select Application Notes under the Documentation tab.

### Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

### Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

### CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

### Solutions Library

Visit our growing library of solution focused designs at www.cypress.com/solutions. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

### Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at www.cypress.com/support. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

## Pinouts

The CY8C20x36/46/66/96 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O and connection to the common analog bus. However, Vss, Vdd, and XRES are not capable of Digital I/O.

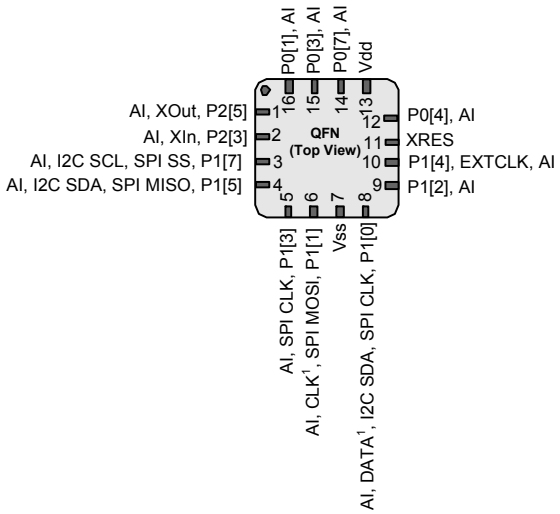
### 16-Pin QFN (No E-Pad)

**Table 2. Pin Definitions - CY8C20236, CY8C20246 PSoC Device** [2]

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | I/O | I | P2[5] | Crystal output (XOut) |
| 2 | I/O | I | P2[3] | Crystal input (XIn) |
| 3 | IOHR | I | P1[7] | I2C SCL, SPI SS |
| 4 | IOHR | I | P1[5] | I2C SDA, SPI MISO |
| 5 | IOHR | I | P1[3] | SPI CLK |
| 6 | IOHR | I | P1[1] | ISSP CLK[1], I2C SCL, SPI MOSI |
| 7 | Power | | Vss | Ground connection |
| 8 | IOHR | I | P1[0] | ISSP DATA[1], I2C SDA, SPI CLK |
| 9 | IOHR | I | P1[2] | |
| 10 | IOHR | I | P1[4] | Optional external clock (EXTCLK) |
| 11 | Input | | XRES | Active high external reset with internal pull down |
| 12 | IOH | I | P0[4] | |
| 13 | Power | | Vdd | Supply voltage |
| 14 | IOH | I | P0[7] | |
| 15 | IOH | I | P0[3] | Integrating input |
| 16 | IOH | I | P0[1] | Integrating input |

**LEGEND** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

**Figure 2. CY8C20236, CY8C20246 PSoC Device**




**Notes**
1. These are the ISSP pins, which are not High Z at POR (Power On Reset).
2. During power up or reset event, device P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter any issues.

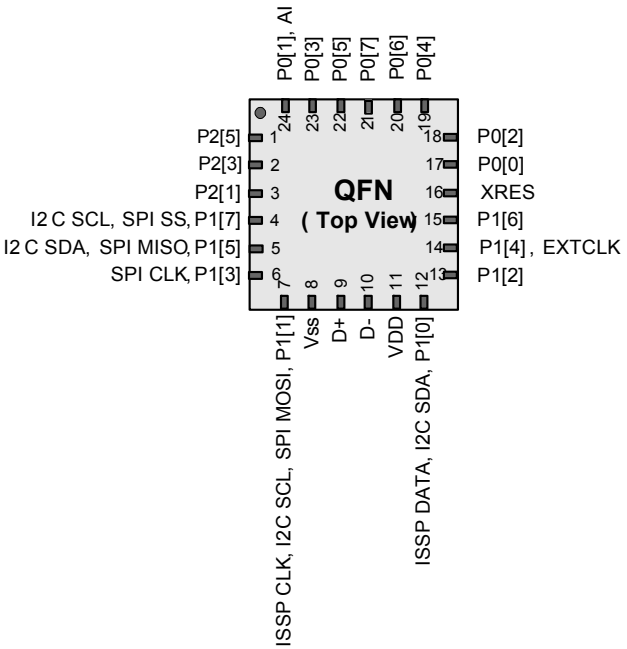
### 24-Pin QFN with USB

**Table 4. Pin Definitions - CY8C20396 PSoC Device** [2, 3]

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | I/O | I | P2[5] | |
| 2 | I/O | I | P2[3] | |
| 3 | I/O | I | P2[1] | |
| 4 | IOHR | I | P1[7] | I2C SCL, SPI SS |
| 5 | IOHR | I | P1[5] | I2C SDA, SPI MISO |
| 6 | IOHR | I | P1[3] | SPI CLK |
| 7 | IOHR | I | P1[1] | ISSP CLK, I2C SCL, SPI MOSI |
| 8 | Power | | VSS | Ground |
| 9 | I/O | I | D+ | USB D+ |
| 10 | I/O | I | D- | USB D- |
| 11 | Power | | VDD | Supply |
| 12 | IOHR | I | P1[0] | ISSP DATA, I2C SDA |
| 13 | IOHR | I | P1[2] | |
| 14 | IOHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 15 | IOHR | I | P1[6] | |
| 16 | RESET INPUT | | XRES | Active high external reset with internal pull down |
| 17 | IOH | I | P0[0] | |
| 18 | IOH | I | P0[2] | |
| 19 | IOH | I | P0[4] | |
| 20 | IOH | I | P0[6] | |
| 21 | IOH | I | P0[7] | |
| 22 | IOH | I | P0[5] | |
| 23 | IOH | I | P0[3] | Integrating input |
| 24 | IOH | I | P0[1] | Integrating input |
| CP | Power | | VSS | Thermal pad must be connected to Ground |

**LEGEND** I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

**Figure 4. CY8C20396 PSoC Device**



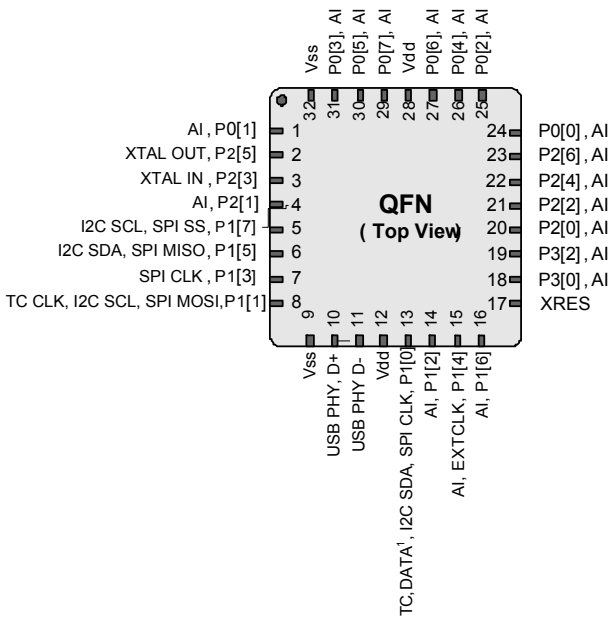
### 32-Pin QFN (with USB)

**Table 6. Pin Definitions - CY8C20496 PSoC Device** [2, 3]

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | IOH | I | P0[1] | |
| 2 | I/O | I | P2[5] | XTAL Out |
| 3 | I/O | I | P2[3] | XTAL In |
| 4 | I/O | I | P2[1] | |
| 5 | IOHR | I | P1[7] | I2C SCL, SPI SS |
| 6 | IOHR | I | P1[5] | I2C SDA, SPI MISO |
| 7 | IOHR | I | P1[3] | SPI CLK |
| 8 | IOHR | I | P1[1] | TC CLK, I2C SCL, SPI MOSI |
| 9 | Power | | $V_{SS}$ | Ground Pin |
| 10 | I | | D+ | USB PHY |
| 11 | I | | D- | USB PHY |
| 12 | Power | | Vdd | Power pin |
| 13 | IOHR | I | P1[0] | TC DATA*, I2C SDA, SPI CLKI |
| 14 | IOHR | I | P1[2] | |
| 15 | IOHR | I | P1[4] | EXTCLK |
| 16 | IOHR | I | P1[6] | |
| 17 | Input | | XRES | Active high external reset with internal pull down |
| 18 | I/O | I | P3[0] | |
| 19 | I/O | I | P3[2] | |
| 20 | I/O | I | P2[0] | |
| 21 | I/O | I | P2[2] | |
| 22 | I/O | I | P2[4] | |
| 23 | I/O | I | P2[6] | |
| 24 | IOH | I | P0[0] | |
| 25 | IOH | I | P0[2] | |
| 26 | IOH | I | P0[4] | |
| 27 | IOH | I | P0[6] | |
| 28 | Power | | Vdd | Power Pin |
| 29 | IOH | I | P0[7] | |
| 30 | IOH | I | P0[5] | |
| 31 | IOH | I | P0[3] | |
| 32 | Power | | Vss | Ground Pin |

**LEGEND** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

**Figure 5. CY8C20496 PSoC Device**

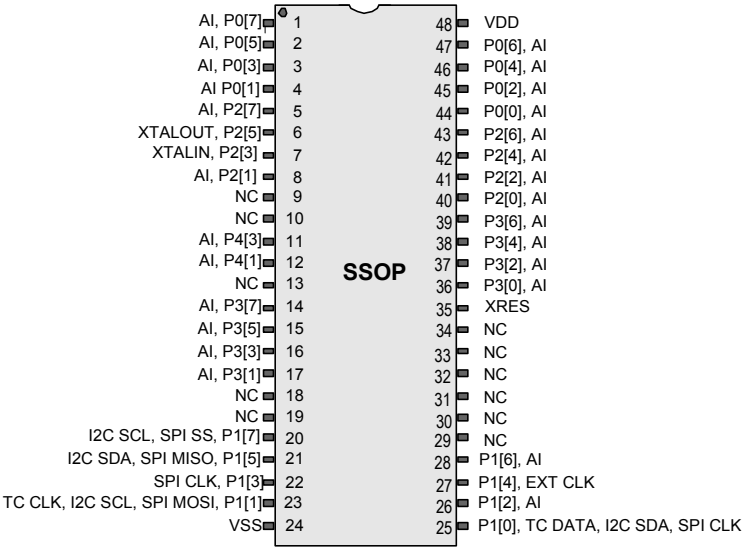


## 48-Pin SSOP

**Table 7. Pin Definitions - CY8C20536, CY8C20546, and CY8C20566 PSoC Device[2]**

| Pin No. | Digital | Analog | Name | Description |
|---|---|---|---|---|
| 1 | IOH | I | P0[7] | |
| 2 | IOH | I | P0[5] | |
| 3 | IOH | I | P0[3] | |
| 4 | IOH | I | P0[1] | |
| 5 | I/O | I | P2[7] | |
| 6 | I/O | I | P2[5] | XTAL Out |
| 7 | I/O | I | P2[3] | XTAL In |
| 8 | I/O | I | P2[1] | |
| 9 | | | NC | No connection |
| 10 | | | NC | No connection |
| 11 | I/O | I | P4[3] | |
| 12 | I/O | I | P4[1] | |
| 13 | | | NC | No connection |
| 14 | I/O | I | P3[7] | |
| 15 | I/O | I | P3[5] | |
| 16 | I/O | I | P3[3] | |
| 17 | I/O | I | P3[1] | |
| 18 | | | NC | No connection |
| 19 | | | NC | No connection |
| 20 | IOHR | I | P1[7] | I2C SCL, SPI SS |
| 21 | IOHR | I | P1[5] | I2C SDA, SPI MISO |
| 22 | IOHR | I | P1[3] | SPI CLK |
| 23 | IOHR | I | P1[1] | TC CLK[1], I2C SCL, SPI MOSI |
| 24 | | | VSS | Ground Pin |
| 25 | IOHR | I | P1[0] | TC DATA[1], I2C SDA, SPI CLK |
| 26 | IOHR | I | P1[2] | |
| 27 | IOHR | I | P1[4] | EXT CLK |
| 28 | IOHR | I | P1[6] | |
| 29 | | | NC | No connection |
| 30 | | | NC | No connection |
| 31 | | | NC | No connection |
| 32 | | | NC | No connection |
| 33 | | | NC | No connection |
| 34 | | | NC | No connection |
| 35 | | | XRES | Active high external reset with internal pull down |
| 36 | I/O | I | P3[0] | |
| 37 | I/O | I | P3[2] | |
| 38 | I/O | I | P3[4] | |
| 39 | I/O | I | P3[6] | |
| 40 | I/O | I | P2[0] | |
| 41 | I/O | I | P2[2] | |
| 42 | I/O | I | P2[4] | |
| 43 | I/O | I | P2[6] | |
| 44 | IOH | I | P0[0] | |
| 45 | IOH | I | P0[2] | |
| 46 | IOH | I | P0[4] | |
| 47 | IOH | I | P0[6] | |
| 48 | Power | | Vdd | Power Pin |

**Figure 6. CY8C20536, CY8C20546, and CY8C20566 PSoC Device**




**LEGEND** A = Analog, I = Input, O = Output, NC = No Connection, H = 5 mA High Output Drive, R = Regulated Output Option.

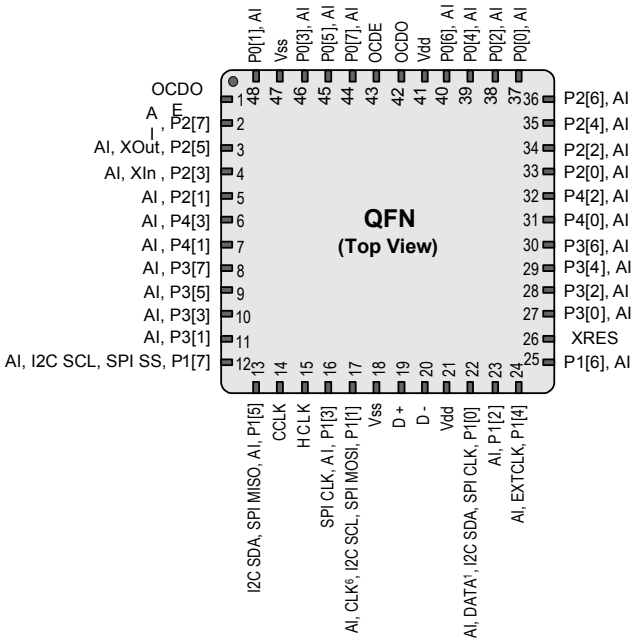
## 48-Pin QFN OCD

The 48-pin QFN part is for the CY8C20066 On-Chip Debug (OCD) PSoC device. Note that this part is only used for in-circuit debugging.[4]

**Table 10. Pin Definitions - CY8C20066 PSoC Device** [2, 3]

| Pin No. | Digital | Analog | Name | Description |
|---|---|---|---|---|
| 1 | | | OCDOE | OCD mode direction pin |
| 2 | I/O | I | P2[7] | |
| 3 | I/O | I | P2[5] | Crystal output (XOut) |
| 4 | I/O | I | P2[3] | Crystal input (XIn) |
| 5 | I/O | I | P2[1] | |
| 6 | I/O | I | P4[3] | |
| 7 | I/O | I | P4[1] | |
| 8 | I/O | I | P3[7] | |
| 9 | I/O | I | P3[5] | |
| 10 | I/O | I | P3[3] | |
| 11 | I/O | I | P3[1] | |
| 12 | IOHR | I | P1[7] | I2C SCL, SPI SS |
| 13 | IOHR | I | P1[5] | I2C SDA, SPI MISO |
| 14 | | | CCLK | OCD CPU clock output |
| 15 | | | HCLK | OCD high speed clock output |
| 16 | IOHR | I | P1[3] | SPI CLK. |
| 17 | IOHR | I | P1[1] | ISSP CLK[1], I2C SCL, SPI MOSI |
| 18 | Power | | Vss | Ground connection |
| 19 | I/O | | D+ | USB D+ |
| 20 | I/O | | D- | USB D- |
| 21 | Power | | Vdd | Supply voltage |
| 22 | IOHR | I | P1[0] | ISSP DATA(1), I2C SDA, SPI CLK |
| 23 | IOHR | I | P1[2] | |
| 24 | IOHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 25 | IOHR | I | P1[6] | |
| 26 | Input | | XRES | Active high external reset with internal pull down |
| 27 | I/O | I | P3[0] | |
| 28 | I/O | I | P3[2] | |
| 29 | I/O | I | P3[4] | |
| 30 | I/O | I | P3[6] | |
| 31 | I/O | I | P4[0] | |
| 32 | I/O | I | P4[2] | |
| 33 | I/O | I | P2[0] | |
| 34 | I/O | I | P2[2] | |
| 35 | I/O | I | P2[4] | |
| 36 | I/O | I | P2[6] | |

**Figure 9. CY8C20066 PSoC Device**




| Pin No. | Digital | Analog | Name | Description |
|---|---|---|---|---|
| 37 | IOH | I | P0[0] | |
| 38 | IOH | I | P0[2] | |
| 39 | IOH | I | P0[4] | |
| 40 | IOH | I | P0[6] | |
| 41 | Power | | Vdd | Supply voltage |
| 42 | | | OCDO | OCD even data I/O |
| 43 | | | OCDE | OCD odd data output |
| 44 | IOH | I | P0[7] | |
| 45 | IOH | I | P0[5] | |
| 46 | IOH | I | P0[3] | Integrating input |
| 47 | Power | | Vss | Ground connection |
| 48 | IOH | I | P0[1] | |
| CP | Power | | Vss | Center pad must be connected to ground |

**LEGEND** A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

**Note**
4. This part is available in limited quantities for In-Circuit Debugging during prototype development. It is not available in production volumes.

## Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20x36/46/66/96 PSoC devices. For the latest electrical specifications, confirm that you have the most recent data sheet by visiting the web at http://www.cypress.com/psoc.

**Figure 10. Voltage versus CPU Frequency**

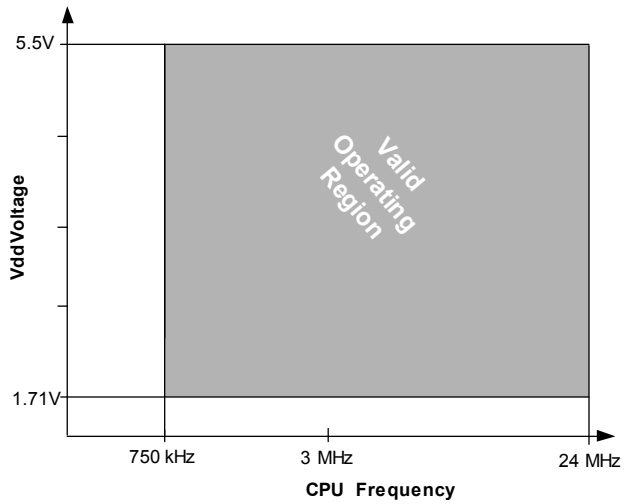
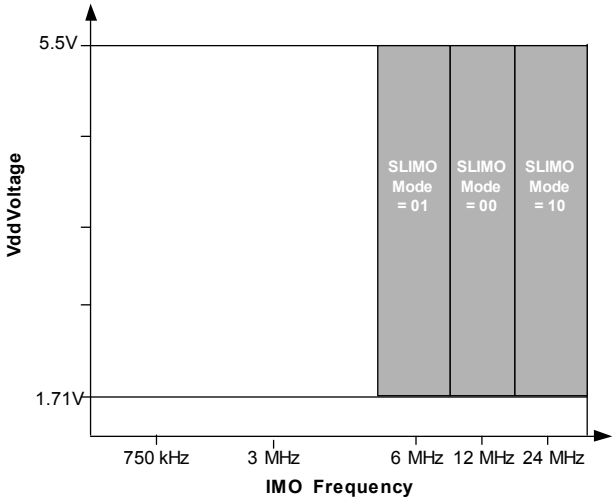



**Figure 11. IMO Frequency Trim Options**




The following table lists the units of measure that are used in this section.

**Table 11. Units of Measure**

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|---|---|---|---|
| °C | degree Celsius | mA | milli-ampere |
| dB | decibels | ms | milli-second |
| fF | femto farad | mV | milli-volts |
| Hz | hertz | nA | nanoampere |
| KB | 1024 bytes | ns | nanosecond |
| Kbit | 1024 bits | nV | nanovolts |
| kHz | kilohertz | Ω | ohm |
| ksps | kilo samples per second | pA | picoampere |
| kΩ | kilohm | pF | picofarad |
| MHz | megahertz | pp | peak-to-peak |
| MΩ | megaohm | ppm | parts per million |
| µA | microampere | ps | picosecond |
| µF | microfarad | sps | samples per second |
| µH | microhenry | s | sigma: one standard deviation |
| µs | microsecond | V | volts |
| µW | microwatts | | |

## DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 14. DC Chip-Level Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Vdd | Supply Voltage | Refer the table DC POR and LVD Specifications on page 24 | 1.71 | – | 5.5 | V |
| $I_{DD24}$ | Supply Current, IMO = 24 MHz | Conditions are Vdd = 3.0V, $T_A$ = 25°C, CPU = 24 MHz. CapSense running at 12 MHz, no I/O sourcing current | – | 2.88 | 4.0 | mA |
| $I_{DD12}$ | Supply Current, IMO = 12 MHz | Conditions are Vdd = 3.0V, $T_A$ = 25°C, CPU = 12 MHz. CapSense running at 12 MHz, no I/O sourcing current | – | 1.71 | 2.6 | mA |
| $I_{DD6}$ | Supply Current, IMO = 6 MHz | Conditions are Vdd = 3.0V, $T_A$ = 25°C, CPU = 6 MHz. CapSense running at 6 MHz, no I/O sourcing current | – | 1.16 | 1.8 | mA |
| $I_{SB0}$ | Deep Sleep Current | Vdd = 3.0V, $T_A$ = 25°C, I/O regulator turned off | – | 0.1 | – | µA |
| $I_{SB1}$ | Standby Current with POR, LVD and Sleep Timer | Vdd = 3.0V, $T_A$ = 25°C, I/O regulator turned off | – | 1.07 | 1.5 | µA |

## DC General Purpose IO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 5.5V and –40°C ≤ $T_A$ ≤ 85°C, 2.4V to 3.0V and –40°C ≤ $T_A$ ≤ 85°C, or 1.71V to 2.4V and –40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 15. 3.0V to 5.5V DC GPIO Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull up Resistor | | 4 | 5.6 | 8 | kΩ |
| $V_{OH1}$ | High Output Voltage Port 2 or 3 Pins | IOH ≤ 10 µA, maximum of 10 mA source current in all IOs | Vdd - 0.2 | – | – | V |
| $V_{OH2}$ | High Output Voltage Port 2 or 3 Pins | IOH = 1 mA, maximum of 20 mA source current in all IOs | Vdd - 0.9 | – | – | V |
| $V_{OH3}$ | High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1 | IOH < 10 µA, maximum of 10 mA source current in all IOs | Vdd - 0.2 | – | – | V |
| $V_{OH4}$ | High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1 | IOH = 5 mA, maximum of 20 mA source current in all IOs | Vdd - 0.9 | – | – | V |
| $V_{OH5}$ | High Output Voltage Port 1 Pins with LDO Regulator Enabled for 3V Out | IOH < 10 µA, Vdd > 3.1V, maximum of 4 IOs all sourcing 5 mA | 2.85 | 3.00 | 3.3 | V |
| $V_{OH6}$ | High Output Voltage Port 1 Pins with LDO Regulator Enabled for 3V Out | IOH = 5 mA, Vdd > 3.1V, maximum of 20 mA source current in all IOs | 2.20 | – | – | V |
| $V_{OH7}$ | High Output Voltage Port 1 Pins with LDO Enabled for 2.5V Out | IOH < 10 µA, Vdd > 2.7V, maximum of 20 mA source current in all IOs | 2.35 | 2.50 | 2.75 | V |
| $V_{OH8}$ | High Output Voltage Port 1 Pins with LDO Enabled for 2.5V Out | IOH = 2 mA, Vdd > 2.7V, maximum of 20 mA source current in all IOs | 1.90 | – | – | V |
| $V_{OH9}$ | High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out | IOH < 10 µA, Vdd > 2.7V, maximum of 20 mA source current in all IOs | 1.60 | 1.80 | 2.1 | V |

**Table 15. 3.0V to 5.5V DC GPIO Specifications** *(continued)*

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OH10}$ | High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out | IOH = 1 mA, Vdd > 2.7V, maximum of 20 mA source current in all IOs | 1.20 | – | – | V |
| $V_{OL}$ | Low Output Voltage | IOL = 25 mA, Vdd > 3.3V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]) | – | – | 0.75 | V |
| $V_{IL}$ | Input Low Voltage | | – | – | 0.80 | V |
| $V_{IH}$ | Input High Voltage | | 2.00 | – | | V |
| $V_H$ | Input Hysteresis Voltage | | – | 80 | – | mV |
| $I_{IL}$ | Input Leakage (Absolute Value) | | – | 0.001 | 1 | µA |
| $C_{PIN}$ | Pin Capacitance | Package and pin dependent Temp = 25°C | 0.5 | 1.7 | 5 | pF |

**Table 16. 2.4V to 3.0V DC GPIO Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull up Resistor | | 4 | 5.6 | 8 | kΩ |
| $V_{OH1}$ | High Output Voltage Port 2 or 3 Pins | IOH < 10 μA, maximum of 10 mA source current in all IOs | Vdd - 0.2 | – | – | V |
| $V_{OH2}$ | High Output Voltage Port 2 or 3 Pins | IOH = 0.2 mA, maximum of 10 mA source current in all IOs | Vdd - 0.4 | – | – | V |
| $V_{OH3}$ | High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1 | IOH < 10 μA, maximum of 10 mA source current in all IOs | Vdd - 0.2 | – | – | V |
| $V_{OH4}$ | High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1 | IOH = 2 mA, maximum of 10 mA source current in all IOs | Vdd - 0.5 | – | – | V |
| $V_{OH5A}$ | High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out | IOH < 10 μA, Vdd > 2.4V, maximum of 20 mA source current in all IOs | 1.50 | 1.80 | 2.1 | V |
| $V_{OH6A}$ | High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out | IOH = 1 mA, Vdd > 2.4V, maximum of 20 mA source current in all IOs | 1.20 | – | – | V |
| $V_{OL}$ | Low Output Voltage | IOL = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]) | – | – | 0.75 | V |
| $V_{IL}$ | Input Low Voltage | | – | – | 0.72 | V |
| $V_{IH}$ | Input High Voltage | | 1.4 | – | | V |
| $V_{H}$ | Input Hysteresis Voltage | | – | 80 | – | mV |
| $I_{IL}$ | Input Leakage (Absolute Value) | | – | 0.001 | 1 | μA |
| $C_{PIN}$ | Capacitive Load on Pins | Package and pin dependent Temp = 25°C | 0.5 | 1.7 | 5 | pF |

**Table 17. 1.71V to 2.4V DC GPIO Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull up Resistor | | 4 | 5.6 | 8 | kΩ |
| $V_{OH1}$ | High Output Voltage Port 2 or 3 Pins | IOH = 10 μA, maximum of 10 mA source current in all I/Os | Vdd - 0.2 | – | – | V |
| $V_{OH2}$ | High Output Voltage Port 2 or 3 Pins | IOH = 0.5 mA, maximum of 10 mA source current in all I/Os | Vdd - 0.5 | – | – | V |
| $V_{OH3}$ | High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1 | IOH = 100 μA, maximum of 10 mA source current in all I/Os | Vdd - 0.2 | – | – | V |
| $V_{OH4}$ | High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1 | IOH = 2 mA, maximum of 10 mA source current in all I/Os | Vdd - 0.5 | – | – | V |
| $V_{OL}$ | Low Output Voltage | IOL = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]) | – | – | 0.4 | V |
| $V_{IL}$ | Input Low Voltage | | – | – | 0.3 x Vdd | V |
| $V_{IH}$ | Input High Voltage | | 0.65 x Vdd | – | | V |

## Comparator User Module Electrical Specifications

The following table lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: –40°C <= TA <= 85°C, 1.71V <= Vdd <= 5.5V.

**Table 21. Comparator User Module Electrical Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{COMP}$ | Comparator Response Time | 50 mV overdrive | | 70 | 100 | ns |
| Offset | | | | 2.5 | 30 | mV |
| Current | | Average DC current, 50 mV overdrive | | 20 | 80 | µA |
| PSRR | Supply voltage >2V | Power Supply Rejection Ratio | | 80 | | dB |
| | Supply voltage <2V | Power Supply Rejection Ratio | | 40 | | dB |
| Input Range | | | 0 | | 1.5 | V |

## ADC Electrical Specifications

**Table 22. ADC User Module Electrical Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Input** | | | | | | |
| $V_{IN}$ | Input Voltage Range | This gives 72% of maximum code | Vss | | 1.3 | V |
| $C_{IN}$ | Input Capacitance | | | | 5 | pF |
| RES | Resolution | Settings 8, 9, or 10 | 8 | | 10 | Bits |
| S8 | 8-Bit Sample Rate | Data Clock set to 6 MHz. Sample Rate = 0.001/ (2^Resolution/Data clock) | | 23.4375 | | ksps |
| S10 | 10-Bit Sample Rate | Data Clock set to 6 MHz. Sample Rate = 0.001/ (2^Resolution/Data clock) | | 5.859 | | ksps |
| **DC Accuracy** | | | | | | |
| DNL[5] | Differential Nonlinearity | For any configuration | -1 | | +2 | LSB |
| INL | Integral Nonlinearity | For any configuration | -2 | | +2 | LSB |
| Eoffset | Offset Error | | 0 | 15 | 90 | mV |
| $I_{ADC}$ | Operating Current | | | 275 | 350 | µA |
| $F_{CLK}$ | Data Clock | Source is chip's internal main oscillator. See device data sheet for accuracy. | 2.25 | | 12 | MHz |
| PSRR | Power Supply Rejection Ration | | | | | |
| | PSRR (Vdd>3.0V) | | | 24 | dB | |
| | PSRR (2.2 < Vdd < 3.0) | | | 30 | dB | |
| | PSRR (2.0 < Vdd < 2.2) | | | 12 | dB | |
| | PSRR (Vdd < 2.0) | | | 0 | dB | |
| Egain | Gain Error | For any resolution | 1 | | 5 | %FSR |
| $R_{IN}$ | Input Resistance | Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution. | 1/(500fF* Data-Clock) | 1/(400fF* Data-Clock) | 1/(300fF* Data-Clock) | Ω |

**Note**
5. Monotonicity is not guaranteed.

## DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 23. DC POR and LVD Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Vdd Value for PPOR Trip | Vdd must be greater than or equal to 1.71V during startup, reset from the XRES pin, or reset from watchdog. | | | | |
| $V_{PPOR0}$ | PORLEV[1:0] = 00b, HPOR = 0 | | 1.61 | 1.66 | 1.71 | V |
| $V_{PPOR1}$ | PORLEV[1:0] = 00b, HPOR = 1 | | | 2.36 | 2.41 | V |
| $V_{PPOR2}$ | PORLEV[1:0] = 01b, HPOR = 1 | | – | 2.60 | 2.66 | V |
| $V_{PPOR3}$ | PORLEV[1:0] = 10b, HPOR = 1 | | | 2.82 | 2.95 | V |
| | Vdd Value for LVD Trip | | | | | |
| $V_{LVD0}$ | VM[2:0] = 000b | | 2.40[6] | 2.45 | 2.51 | V |
| $V_{LVD1}$ | VM[2:0] = 001b | | 2.64[7] | 2.71 | 2.78 | V |
| $V_{LVD2}$ | VM[2:0] = 010b | | 2.85[8] | 2.92 | 2.99 | V |
| $V_{LVD3}$ | VM[2:0] = 011b | | 2.95 | 3.02 | 3.09 | V |
| $V_{LVD4}$ | VM[2:0] = 100b | | 3.06 | 3.13 | 3.20 | V |
| $V_{LVD5}$ | VM[2:0] = 101b | | 1.84 | 1.90 | 2.32 | V |
| $V_{LVD6}$ | VM[2:0] = 110b | | 1.75[9] | 1.80 | 1.84 | V |
| $V_{LVD7}$ | VM[2:0] = 111b | | 4.62 | 4.73 | 4.83 | V |

## DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 24. DC Programming Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $Vdd_{IWRITE}$ | Supply Voltage for Flash Write Operations | | 1.71 | – | 5.25 | V |
| $I_{DDP}$ | Supply Current During Programming or Verify | | – | 5 | 25 | mA |
| $V_{ILP}$ | Input Low Voltage During Programming or Verify | See the appropriate DC General Purpose IO Specifications on page 19 | – | – | $V_{IL}$ | V |
| $V_{IHP}$ | Input High Voltage During Programming or Verify | See appropriate DC General Purpose IO Specifications on page 19 table on pages 15 or 16 | $V_{IH}$ | – | – | V |
| $I_{ILP}$ | Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify | Driving internal pull down resistor | – | – | 0.2 | mA |
| $I_{IHP}$ | Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify | Driving internal pull down resistor | – | – | 1.5 | mA |
| $V_{OLP}$ | Output Low Voltage During Programming or Verify | | – | – | Vss + 0.75 | V |
| $V_{OHP}$ | Output High Voltage During Programming or Verify | See appropriate DC General Purpose IO Specifications on page 19 table on page 16. For Vdd > 3V use $V_{OH4}$ in Table 13 on page 18. | $V_{OH}$ | – | Vdd | V |
| $Flash_{ENPB}$ | Flash Write Endurance | Erase/write cycles per block | 50,000 | – | – | - |
| $Flash_{DR}$ | Flash Data Retention | Following maximum Flash write cycles; ambient temperature of 55°C | 10 | 20 | – | Years |

**Notes**
6. Always greater than 50 mV above $V_{PPOR1}$ voltage for falling supply.
7. Always greater than 50 mV above $V_{PPOR2}$ voltage for falling supply.
8. Always greater than 50 mV above $V_{PPOR3}$ voltage for falling supply.
9. Always greater than 50 mV above $V_{PPOR0}$ voltage for falling supply.

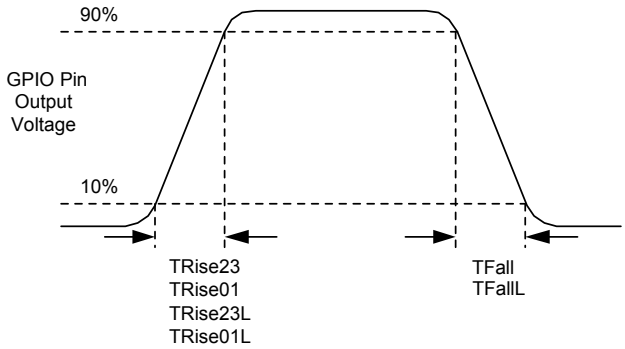
## AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 26. AC GPIO Specifications**

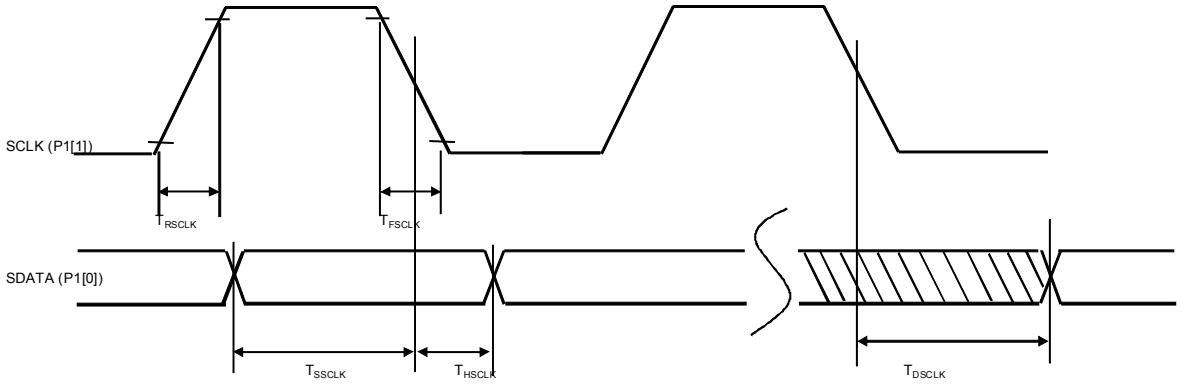
| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GPIO}$ | GPIO Operating Frequency | Normal Strong Mode Port 0, 1 | 0<br><br>0 | –<br><br>– | 6 MHz for 1.71V<Vdd<2.4V<br><br>12 MHz for 2.4V<Vdd<5.5V | MHz |
| TRise23 | Rise Time, Strong Mode, Cload = 50 pF Ports 2 or 3 | Vdd = 3.0 to 3.6V, 10% – 90% | 15 | – | 80 | ns |
| TRise23L | Rise Time, Strong Mode Low Supply, Cload = 50 pF, Ports 2 or 3 | Vdd = 1.71 to 3.0V, 10% – 90% | 15 | – | 80 | ns |
| TRise01 | Rise Time, Strong Mode, Cload = 50 pF Ports 0 or 1 | Vdd = 3.0 to 3.6V, 10% – 90% LDO enabled or disabled | 10 | – | 50 | ns |
| TRise01L | Rise Time, Strong Mode Low Supply, Cload = 50 pF, Ports 0 or 1 | Vdd = 1.71 to 3.0V, 10% – 90% LDO enabled or disabled | 10 | – | 80 | ns |
| TFall | Fall Time, Strong Mode, Cload = 50 pF All Ports | Vdd = 3.0 to 3.6V, 10% – 90% | 10 | – | 50 | ns |
| TFallL | Fall Time, Strong Mode Low Supply, Cload = 50 pF, All Ports | Vdd = 1.71 to 3.0V, 10% – 90% | 10 | – | 70 | ns |

**Figure 12. GPIO Timing Diagram**



## AC Programming Specifications

**Figure 13. AC Waveform**




The following table lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 32. AC Programming Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{RSCLK}$ | Rise Time of SCLK | | 1 | – | 20 | ns |
| $T_{FSCLK}$ | Fall Time of SCLK | | 1 | – | 20 | ns |
| $T_{SSCLK}$ | Data Set up Time to Falling Edge of SCLK | | 40 | – | – | ns |
| $T_{HSCLK}$ | Data Hold Time from Falling Edge of SCLK | | 40 | – | – | ns |
| $F_{SCLK}$ | Frequency of SCLK | | 0 | – | 8 | MHz |
| $T_{ERASEB}$ | Flash Erase Time (Block) | | – | – | 18 | ms |
| $T_{WRITE}$ | Flash Block Write Time | | – | – | 25 | ms |
| $T_{DSCLK}$ | Data Out Delay from Falling Edge of SCLK | 3.6 < Vdd | – | – | 60 | ns |
| $T_{DSCLK3}$ | Data Out Delay from Falling Edge of SCLK | 3.0 ≤ Vdd ≤ 3.6 | – | – | 85 | ns |
| $T_{DSCLK2}$ | Data Out Delay from Falling Edge of SCLK | 1.71 ≤ Vdd ≤ 3.0 | – | – | 130 | ns |
| $T_{XRST3}$ | External Reset Pulse Width after Power Up | Required to enter programming mode when coming out of sleep | 263 | – | – | µs |

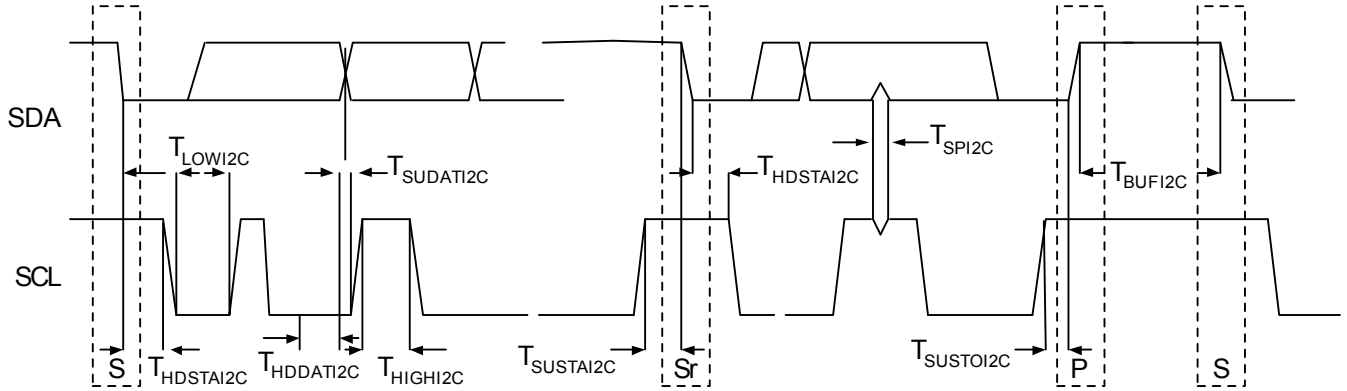
## AC I2C Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 33. AC Characteristics of the I2C SDA and SCL Pins**

| Symbol | Description | Standard Mode | | Fast Mode | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $F_{SCLI2C}$ | SCL Clock Frequency | 0 | 100 | 0 | 400 | kHz |
| $T_{HDSTAI2C}$ | Hold Time (repeated) START Condition. After this period, the first clock pulse is generated. | 4.0 | – | 0.6 | – | µs |
| $T_{LOWI2C}$ | LOW Period of the SCL Clock | 4.7 | – | 1.3 | – | µs |
| $T_{HIGHI2C}$ | HIGH Period of the SCL Clock | 4.0 | – | 0.6 | – | µs |
| $T_{SUSTAI2C}$ | Setup Time for a Repeated START Condition | 4.7 | – | 0.6 | – | µs |
| $T_{HDDATI2C}$ | Data Hold Time | 0 | – | 0 | – | µs |
| $T_{SUDATI2C}$ | Data Setup Time | 250 | – | 100[11] | – | ns |
| $T_{SUSTOI2C}$ | Setup Time for STOP Condition | 4.0 | – | 0.6 | – | µs |
| $T_{BUFI2C}$ | Bus Free Time Between a STOP and START Condition | 4.7 | – | 1.3 | – | µs |
| $T_{SPI2C}$ | Pulse Width of spikes are suppressed by the input filter. | – | – | 0 | 50 | ns |

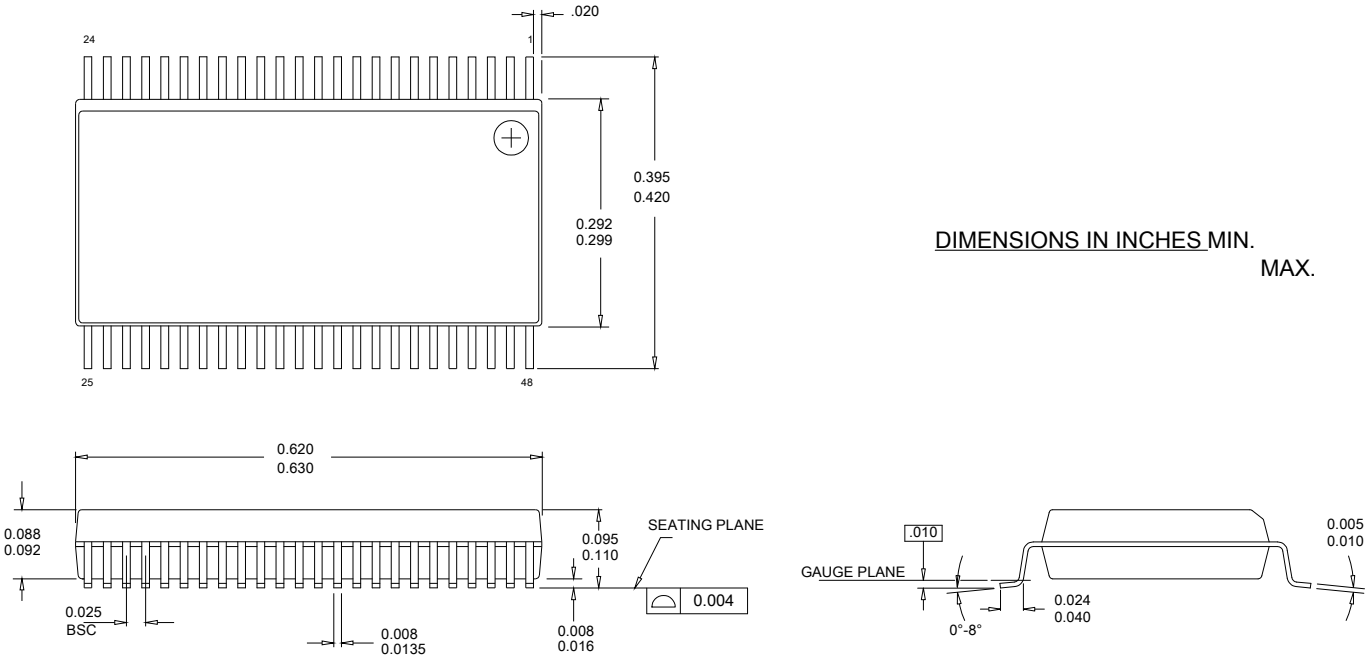
**Figure 14. Definition for Timing for Fast/Standard Mode on the $I^2C$ Bus**




**Note**

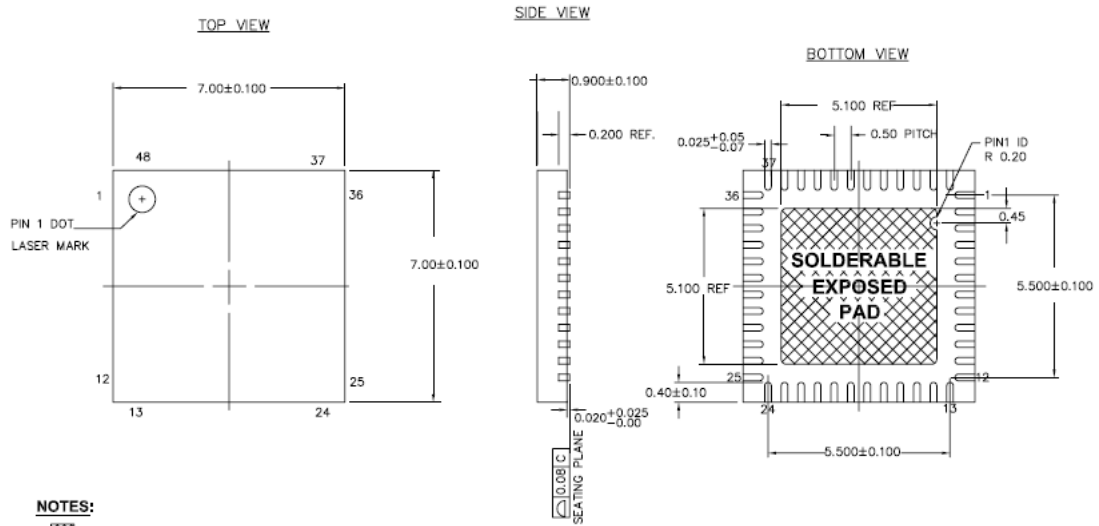
11. A Fast-Mode I2C-bus device can be used in a Standard Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

**Figure 18. 48-Pin (300 MIL) SSOP**




51-85061 *C

**Figure 19. 48-Pin (7x7 mm) QFN**




**NOTES:**
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *C

**Important Notes**

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.
- Pinned vias for thermal conduction are not required for the low power PSoC device.

## Device Programmers

All device programmers are purchased from the Cypress Online Store.

*CY3216 Modular Programmer*

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- Three Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

*CY3207ISSP In-System Serial Programmer (ISSP)*

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment.
Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

## Accessories (Emulation and Programming)

**Table 38. Emulation and Programming Accessories**

| Part Number | Pin Package | Flex-Pod Kit[15] | Foot Kit[16] | Adapter[17] |
|---|---|---|---|---|
| CY8C20236-24LKXI | 16 QFN | CY3250-20266QFN | CY3250-16QFN-RK | See note 15 |
| CY8C20246-24LKXI | 16 QFN | CY3250-20266QFN | CY3250-16QFN-FK | See note 17 |
| CY8C20336-24LQXI | 24 QFN | CY3250-20366QFN | CY3250-24QFN-FK | See note 15 |
| CY8C20346-24LQXI | 24 QFN | CY3250-20366QFN | CY3250-24QFN-FK | See note 17 |
| CY8C20396-24LQXI | 24 QFN | Not Available | | |
| CY8C20436-24LQXI | 32 QFN | CY3250-20466QFN | CY3250-32QFN-RK | See note 15 |
| CY8C20446-24LQXI | 32 QFN | CY3250-20466QFN | CY3250-32QFN-FK | See note 17 |
| CY8C20466-24LQXI | 32 QFN | CY3250-20466QFN | CY3250-32QFN-FK | See note 17 |
| CY8C20496-24LQXI | 32 QFN | Not Available | | |
| CY8C20536-24PVXI | 48 SSOP | CY3250-20X66 | CY3250-48SSOP-FK | See note 17 |
| CY8C20546-24PVXI | 48 SSOP | CY3250-20X66 | CY3250-48SSOP-FK | See note 17 |
| CY8C20566-24PVXI | 48 SSOP | CY3250-20X66 | CY3250-48SSOP-FK | See note 17 |
| CY8C20636-24LTXI | 48 QFN | CY3250-20666QFN | CY3250-48QFN-FK | See note 17 |
| CY8C20646-24LTXI | 48 QFN | CY3250-20666QFN | CY3250-48QFN-FK | See note 17 |
| CY8C20666-24LTXI | 48 QFN | CY3250-20666QFN | CY3250-48QFN-FK | See note 17 |

## Third-Party Tools

Several tools have been specially designed by the following third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at http://www.cypress.com under Documentation > Evaluation Boards.

## Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, refer Application Note “Debugging - Build a PSoC Emulator into Your Board - AN2323” at http://www.cypress.com/?rID2748.

**Notes**
15. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
16. Foot kit includes surface mount feet that can be soldered to the target PCB.
17. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

## Document History Page

| Document Title: CY8C20x36/46/66/96 CapSense® Applications<br>Document Number: 001-12696 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Origin of Change** | **Submission Date** | **Description of Change** |
| ** | 766857 | HMT | See ECN | New silicon and document (Revision **). |
| *A | 1242866 | HMT | See ECN | Add features. Update all applicable sections. Update specs. Fix 24-pin QFN pinout moving pins inside. Update package revisions. Update and add to Emulation and Programming Accessories table. |
| *B | 2174006 | AESA | See ECN | Added 48-Pin SSOP Part Pinout<br>Modified symbol $R_{VDD}$ to $R_{GND}$ in Table DC Analog Mux Bus Specification<br>Added footnote in Table DC Analog Mux Bus Specification<br>Added 16K FLASH Parts. Updated Notes, Package Diagrams and Ordering Information table. Updated Thermal Impedance and Solder Reflow tables |
| *C | 2587518 | TOF/JASM/MNU/ HMT | 10/13/08 | Converted from Preliminary to Final<br>Fixed broken links. Updated data sheet template.<br>Added operating voltage ranges with USB<br>ADC resolution changed from 10-bit to 8-bit<br>Included ADC specifications table<br>Included Comparator specification table<br>Included Voh7, Voh8, Voh9, Voh10 specs<br>Flash data retention – condition added to Note<br>Input leakage spec changed to 1 µA max<br>GPIO rise time for ports 0,1 and ports 2,3 made common<br>AC Programming specifications updated<br>Included AC Programming cycle timing diagram<br>AC SPI specification updated<br>The VIH for 3.0<Vdd<2.4 changed to 1.6 from 2.0<br>Added USB specification<br>Added SPI CLK to P1[0]<br>Updated package diagrams<br>Updated thermal impedances for QFN packages<br>Updated $F_{GPIO}$ parameter in Table 23<br>Updated voltage ranges for $F_{SPIM}$ and $F_{SPIS}$ in Table 30<br>Update Development Tools, add Designing with PSoC Designer. Edit, fix links, notes and table format. Update $R_{IN}$ formula, fix TRise parameter names in GPIO figure, fix Switch Rate note. Update maximum data in Table 20. DC POR and LVD Specifications. |
| *D | 2649637 | SNV/AESA | 03/17/2009 | Changed title to “CY8C20x36/46/66, CY8C20396 CapSense™ Applications”. Updated data sheet Features, pin information, and ordering information sections. Updated package diagram 001-42168 to *C. |
| *E | 2700196 | SNV/PYRS | 04/30/2009 | Added part numbers CY8C20496, CY8C20536, CY8C20546, CY8C20636, CY8C20646<br>Updated Features on page 1<br>Added 48-Pin QFN without USB pin Diagram and Pin Definition table<br>Added 32-Pin QFN (with USB) package<br>Added SPI Master and Slave AC Specificatons<br>Updated Emulations and Programming Accessories Table on page 33<br>Updated Ordering Information on page 37<br>Removed reference to Hi-Tech C Compiler in Development Tool Selection on page 35 |

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

| Products | |
|---|---|
| PSoC | psoc.cypress.com |
| Clocks & Buffers | clocks.cypress.com |
| Wireless | wireless.cypress.com |
| Memories | memory.cypress.com |
| Image Sensors | image.cypress.com |

| PSoC Solutions | |
|---|---|
| General | psoc.cypress.com/solutions |
| Low Power/Low Voltage | psoc.cypress.com/low-power |
| Precision Analog | psoc.cypress.com/precision-analog |
| LCD Drive | psoc.cypress.com/lcd-drive |
| CAN 2.0b | psoc.cypress.com/can |
| USB | psoc.cypress.com/usb |