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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific

represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are <u>Embedded - Microcontrollers -</u> <u>Application Specific</u>?

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Details

Product Status	Obsolete
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (16kB)
Controller Series	CY8C20xx6
RAM Size	2K x 8
Interface	I ² C, SPI
Number of I/O	36
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Durahaaa UDI	https://www.a.yfl.com/product.dotail/infinaan.tachpalagiac/cy/0c20E46_24p.yvi
Purchase ORL	https://www.e-xh.com/product-detail/infineon-technologies/cy8c20546-24pvxi

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Logic Block Diagram







Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

- 1. Select Components
- 2. Configure Components
- 3. Organize and Connect
- 4. Generate, Verify, and Debug

Select Components

Both the system-level and chip-level views provide a library of pre-built, pre-tested hardware peripheral components. In the system-level view these components are called "drivers" and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces (I²C-bus, for example), and the logic to control how they interact with one another (called valuators).

In the chip-level view the components are called "user modules." User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and programmable system-on-chip varieties.

Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins, or connect system-level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view selecting a potentiometer driver to control a variable speed fan driver and setting up the valuators to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog-todigital converter (ADC) to convert the potentiometer's output to a digital signal, and a PWM to control the fan.

In the chip-level view, you perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the "Generate Configuration Files" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed. The system-level design also generates a C main() program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.



Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Table 1. Acronyms

Acronym	Description
AC	alternating current
API	application programming interface
CPU	central processing unit
DC	direct current
FSR	full scale range
GPIO	general purpose I/O
GUI	graphical user interface
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™
SLIMO	slow IMO
SRAM	static random access memory

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 11 on page 17 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, 01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimal.



24-Pin QFN with USB

Table 4. Pin Definitions - CY8C20396 PSoC Device [2, 3]

Din No	Тур	be	Namo	Description
FILLING.	Digital	Analog	Name	Description
1	I/O	Ι	P2[5]	
2	I/O	I	P2[3]	
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I2C SCL, SPI SS
5	IOHR	I	P1[5]	I2C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK, I2C SCL, SPI MOSI
8	Pov	ver	VSS	Ground
9	I/O	I	D+	USB D+
10	I/O	I	D-	USB D-
11	Pov	ver	VDD	Supply
12	IOHR	I	P1[0]	ISSP DATA, I2C SDA
13	IOHR	I	P1[2]	
14	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
15	IOHR	I	P1[6]	
16	RESET	INPUT	XRES	Active high external reset with internal pull down
17	IOH	I	P0[0]	
18	IOH	I	P0[2]	
19	IOH	I	P0[4]	
20	IOH	I	P0[6]	
21	IOH	I	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input
24	IOH	I	P0[1]	Integrating input
CP	Pov	ver	VSS	Thermal pad must be connected to Ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output





48-Pin QFN with USB

Table 9. Pin Definitions - CY8C20646, CY8C20666 PSoC Device $^{\left[2,\;3\right]}$

Pin No.	Digital	Analog	Name	Description	Figure 8. CY8C20646, CY8C20666 PSoC Device				8C20646, CY8C20666 PSoC Device 8C20646, CY8C20666 PSoC Device マロン マロン マロン マロン マロン マロン マロン マロン マロン マロン
1			NC	No connection					
2	I/O	Ι	P2[7]					NC 1	8 4 9 9 9 7 7 7 7 7 9 8 8 6 6 6 8 P2[6], AI
3	I/O	Ι	P2[5]	Crystal output (XOut)		^		, P2[7] = 2	35 P 2[4],AI
4	I/O	Ι	P2[3]	Crystal input (XIn)		~	Al, Xln	, P2[3] = 4	33 = P2[2],Al
5	I/O	Ι	P2[1]				AI	, P2[1] = 5	32 P 4[2],AI
6	I/O	I	P4[3]				AI	, P4[3] =6	
7	I/O	I	P4[1]				AI	, P4[1] P 7 , P3[7] P 8	(100 View) 30 P P3[0],Al 29 P P3[4], Al
8	I/O	I	P3[7]				AI	, P3[5] P 9	28 = P3[2],AI
9	I/O	I	P3[5]				AI	, P3[3] = 10	0 27 E P3[0], AI
10	I/O	I	P3[3]		AI, I	2C SCL,	SPI SS	, P1[7] =1;	20 7 10 0 ~ 0 0 0 - 0 0 725 P1[6], Al
11	I/O	Ι	P3[1]						
12	IOHR	- 1	P1[7]	I2C SCL, SPI SS					7[5] NC NC NC NC NC NC NC NC NC NC NC NC NC
13	IOHR	I	P1[5]	I2C SDA, SPI MISO					AI, F SSI, F LK, P LK, P
14			NC	No connection					
15			NC	No connection					SPI M SPI (SDA, AI, E
16	IOHR	I	P1[3]	SPI CLK					
17	IOHR	I	P1[1]	ISSP CLK ^[1] , I2C SCL, SPI MOSI					2C S TA1, K ⁶ , I2
18	Pow	ver	Vss	Ground connection	1				
19	I/O		D+	USB D+					4 4
20	I/O		D-	USB D-					
21	Pow	er	Vdd	Supply voltage					
22	IOHR	I	P1[0]	ISSP DATA ^[1] , I2C SDA, SPI CLK					
23	IOHR	Ι	P1[2]						
24	IOHR	Ι	P1[4]	Optional external clock input (EXTCLK)					
25	IOHR	I	P1[6]						
26	Inp	ut	XRES	Active high external reset with internal pull down					
27	I/O	- 1	P3[0]						
28	I/O	I	P3[2]			1		-	1
29	I/O	I	P3[4]		Pin No.	Digital	Analog	Name	Description
30	I/O	-	P3[6]		40	IOH	I	P0[6]	
31	I/O	-	P4[0]		41	Po	wer	Vdd	Supply voltage
32	I/O	Ι	P4[2]		42			NC	No connection
33	I/O	Ι	P2[0]		43			NC	No connection
34	I/O	I	P2[2]		44	IOH	Ι	P0[7]	
35	I/O	Ι	P2[4]		45	IOH	Ι	P0[5]	
36	I/O	Ι	P2[6]		46	IOH	Ι	P0[3]	Integrating input
37	IOH	Ι	P0[0]		47	Po	wer	Vss	Ground connection
38	IOH	Ι	P0[2]		48	IOH	Ι	P0[1]	
39	IOH	I	P0[4]		CP	Po	wer	Vss	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 12. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Тур	Max	Units
T _{STG}	Storage Temperature	Higher storage temperatures reduces data retention time. Recommended Storage Temperature is $+25^{\circ}C \pm 25^{\circ}C$. Extended duration storage temperatures above $85^{\circ}C$ degrades reliability.	-55	+25	+125	ů
Vdd	Supply Voltage Relative to Vss		-0.5	-	+6.0	V
V _{IO}	DC Input Voltage		Vss – 0.5	-	Vdd + 0.5	V
V _{IOZ}	DC Voltage Applied to Tri-state		Vss -0.5	-	Vdd + 0.5	V
I _{MIO}	Maximum Current into any Port Pin		-25	—	+50	mA
ESD	Electro Static Discharge Voltage	Human Body Model ESD	2000	—	-	V
LU	Latch up Current	In accordance with JESD78 standard	_	_	200	mA

Operating Temperature

Table 13. Operating Temperature

Symbol	Description	Conditions	Min	Тур	Мах	Units
T _A	Ambient Temperature		-40	-	+85	°C
TJ	Operational Die Temperature	The temperature rise from ambient to junction is package specific. Refer the table Thermal Impedances per Package on page 34. The user must limit the power consumption to comply with this requirement.	-40	-	+100	°C



DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 14. DC Chip-Level Specifications

Symbol	Description	Conditions	Min	Тур	Мах	Units
Vdd	Supply Voltage	Refer the table DC POR and LVD Specifications on page 24	1.71	-	5.5	V
I _{DD24}	Supply Current, IMO = 24 MHz	Conditions are Vdd = 3.0V, T _A = 25°C, CPU = 24 MHz. CapSense running at 12 MHz, no I/O sourcing current	-	2.88	4.0	mA
I _{DD12}	Supply Current, IMO = 12 MHz	Conditions are Vdd = 3.0V, T _A = 25°C, CPU = 12 MHz. CapSense running at 12 MHz, no I/O sourcing current	_	1.71	2.6	mA
I _{DD6}	Supply Current, IMO = 6 MHz	Conditions are Vdd = 3.0V, T _A = 25°C, CPU = 6 MHz. CapSense running at 6 MHz, no I/O sourcing current	-	1.16	1.8	mA
I _{SB0}	Deep Sleep Current	Vdd = 3.0V, T _A = 25°C, I/O regulator turned off	-	0.1	-	μA
I _{SB1}	Standby Current with POR, LVD and Sleep Timer	Vdd = 3.0V, T _A = 25°C, I/O regulator turned off	_	1.07	1.5	μA

DC General Purpose IO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 5.5V and $-40^{\circ}C \le T_A \le 85^{\circ}C$, 2.4V to 3.0V and $-40^{\circ}C \le T_A \le 85^{\circ}C$, or 1.71V to 2.4V and $-40^{\circ}C \le T_A \le 85^{\circ}C$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 15. 3.0V to 5.5V DC GPIO Specifications

Symbol	Description	Conditions	Min	Тур	Max	Units
R _{PU}	Pull up Resistor		4	5.6	8	kΩ
V _{OH1}	High Output Voltage Port 2 or 3 Pins	IOH \leq 10 μ A, maximum of 10 mA source current in all IOs	Vdd - 0.2	_	_	V
V _{OH2}	High Output Voltage Port 2 or 3 Pins	IOH = 1 mA, maximum of 20 mA source current in all IOs	Vdd - 0.9	_	-	V
V _{OH3}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	IOH < 10 μ A, maximum of 10 mA source current in all IOs	Vdd - 0.2	_	-	V
V _{OH4}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	IOH = 5 mA, maximum of 20 mA source current in all IOs	Vdd - 0.9	_	-	V
V _{OH5}	High Output Voltage Port 1 Pins with LDO Regulator Enabled for 3V Out	IOH < 10 μ A, Vdd > 3.1V, maximum of 4 IOs all sourcing 5 mA	2.85	3.00	3.3	V
V _{OH6}	High Output Voltage Port 1 Pins with LDO Regulator Enabled for 3V Out	IOH = 5 mA, Vdd > 3.1V, maximum of 20 mA source current in all IOs	2.20	_	_	V
V _{OH7}	High Output Voltage Port 1 Pins with LDO Enabled for 2.5V Out	IOH < 10 μA, Vdd > 2.7V, maximum of 20 mA source current in all IOs	2.35	2.50	2.75	V
V _{OH8}	High Output Voltage Port 1 Pins with LDO Enabled for 2.5V Out	IOH = 2 mA, Vdd > 2.7V, maximum of 20 mA source current in all IOs	1.90	_	-	V
V _{OH9}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	IOH < 10 μ A, Vdd > 2.7V, maximum of 20 mA source current in all IOs	1.60	1.80	2.1	V



Table 17. 1.71V to 2.4V DC GPIO Specifications (continued)

Symbol	Description	Conditions	Min	Тур	Max	Units
V _H	Input Hysteresis Voltage		-	80	-	mV
IIL	Input Leakage (Absolute Value)		-	0.001	1	μA
C _{PIN}	Capacitive Load on Pins	Package and pin dependent Temp = 25 ^o C	0.5	1.7	5	pF

Table 18.DC Characteristics – USB Interface

Symbol	Description	Conditions	Min	Тур	Max	Units
Rusbi	USB D+ Pull Up Resistance	With idle bus	0.900	-	1.575	kΩ
Rusba	USB D+ Pull Up Resistance	While receiving traffic	1.425	-	3.090	kΩ
Vohusb	Static Output High		2.8	-	3.6	V
Volusb	Static Output Low			-	0.3	V
Vdi	Differential Input Sensitivity		0.2	-		V
Vcm	Differential Input Common Mode Range		0.8	-	2.5	V
Vse	Single Ended Receiver Threshold		0.8	-	2.0	V
Cin	Transceiver Capacitance			-	50	pF
lio	Hi-Z State Data Line Leakage	On D+ or D- line	-10	-	+10	μA
Rps2	PS/2 Pull Up Resistance		3	5	7	kΩ
Rext	External USB Series Resistor	In series with each USB pin	21.78	22.0	22.22	Ω

DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. DC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Тур	Мах	Units
R _{SW}	Switch Resistance to Common Analog Bus		-	-	800	Ω
R _{GND}	Resistance of Initialization Switch to Vss		_	-	800	Ω

The maximum pin voltage for measuring $\rm R_{SW}$ and $\rm R_{GND}$ is 1.8V

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 20. DC Comparator Specifications

Symbol	Description	Conditions	Min	Тур	Мах	Units
V _{LPC}	Low Power Comparator (LPC) common mode	Maximum voltage limited to Vdd	0.0	-	1.8	V
I _{LPC}	LPC supply current		-	10	40	μΑ
V _{OSLPC}	LPC voltage offset		-	2.5	30	mV



DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 23. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Тур	Max	Units
V _{PPOR0} V _{PPOR1} V _{PPOR2} V _{PPOR3}	Vdd Value for PPOR Trip PORLEV[1:0] = 00b, HPOR = 0 PORLEV[1:0] = 00b, HPOR = 1 PORLEV[1:0] = 01b, HPOR = 1 PORLEV[1:0] = 10b, HPOR = 1	Vdd must be greater than or equal to 1.71V during startup, reset from the XRES pin, or reset from watchdog.	1.61 _	1.66 2.36 2.60 2.82	1.71 2.41 2.66 2.95	> > >
V _{LVD0} V _{LVD1} V _{LVD2} V _{LVD3} V _{LVD4} V _{LVD5} V _{LVD6} V _{LVD7}	Vdd Value for LVD Trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b		2.40 ^[6] 2.64 ^[7] 2.85 ^[8] 2.95 3.06 1.84 1.75 ^[9] 4.62	2.45 2.71 2.92 3.02 3.13 1.90 1.80 4.73	2.51 2.78 2.99 3.09 3.20 2.32 1.84 4.83	>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 24. DC Programming Specifications

Symbol	Description	Conditions	Min	Тур	Max	Units
Vdd _{IWRITE}	Supply Voltage for Flash Write Operations		1.71	-	5.25	V
I _{DDP}	Supply Current During Programming or Verify		_	5	25	mA
V _{ILP}	Input Low Voltage During Programming or Verify	See the appropriate DC General Purpose IO Specifications on page 19	_	_	V _{IL}	V
V _{IHP}	Input High Voltage During Programming or Verify	See appropriate DC General Purpose IO Specifications on page 19 table on pages 15 or 16	V _{IH}	_	_	V
I _{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	Driving internal pull down resistor	-	_	0.2	mA
I _{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	Driving internal pull down resistor	-	-	1.5	mA
V _{OLP}	Output Low Voltage During Programming or Verify		_	-	Vss + 0.75	V
V _{OHP}	Output High Voltage During Programming or Verify	See appropriate DC General Purpose IO Specifications on page 19 table on page 16. For Vdd > 3V use V _{OH4} in Table 13 on page 18.	V _{OH}	-	Vdd	V
Flash _{ENPB}	Flash Write Endurance	Erase/write cycles per block	50,000	-	-	-
Flash _{DR}	Flash Data Retention	Following maximum Flash write cycles; ambient temperature of 55°C	10	20	_	Years

Notes

- 6. Always greater than 50 mV above V_{PPOR1} voltage for falling supply. 7. Always greater than 50 mV above V_{PPOR2} voltage for falling supply. 8. Always greater than 50 mV above V_{PPOR3} voltage for falling supply. 9. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.



AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 25. AC Chip-Level Specifications

Symbol	Description	Conditions	Min	Тур	Мах	Units
F _{CPU}	CPU Frequency		5.7	-	25.2	MHz
F _{32K1}	Internal Low Speed Oscillator Frequency		19	32	50	kHz
F _{IMO24}	Internal Main Oscillator Frequency at 24 MHz Setting		22.8	24	25.2	MHz
F _{IMO12}	Internal Main Oscillator Frequency at 12 MHz Setting		11.4	12	12.6	MHz
F _{IMO6}	Internal Main Oscillator Frequency at 6 MHz Setting		5.7	6.0	6.3	MHz
DC _{IMO}	Duty Cycle of IMO		40	50	60	%
T _{RAMP}	Supply Ramp Time		20	-	-	μS
T _{XRST}	External Reset Pulse Width at Power Up	After supply voltage is valid	1			ms
T _{XRST2}	External Reset Pulse Width after Power Up ^[10]	Applies after part has booted	10			μS



AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges. **Table 26.** AC GPIO Specifications

Symbol	Description	Conditions	Min	Тур	Max	Units
F _{GPIO}	GPIO Operating Frequency	Normal Strong Mode Port 0, 1	0	-	6 MHz for 1.71V <vdd<2.4v< td=""><td>MHz</td></vdd<2.4v<>	MHz
			0	-	12 MHz for 2.4V <vdd<5.5v< td=""><td></td></vdd<5.5v<>	
TRise23	Rise Time, Strong Mode, Cload = 50 pF Ports 2 or 3	Vdd = 3.0 to 3.6V, 10% – 90%	15	-	80	ns
TRise23L	Rise Time, Strong Mode Low Supply, Cload = 50 pF, Ports 2 or 3	Vdd = 1.71 to 3.0V, 10% – 90%	15	-	80	ns
TRise01	Rise Time, Strong Mode, Cload = 50 pF Ports 0 or 1	Vdd = 3.0 to 3.6V, 10% – 90% LDO enabled or disabled	10	-	50	ns
TRise01L	Rise Time, Strong Mode Low Supply, Cload = 50 pF, Ports 0 or 1	Vdd = 1.71 to 3.0V, 10% – 90% LDO enabled or disabled	10	-	80	ns
TFall	Fall Time, Strong Mode, Cload = 50 pF All Ports	Vdd = 3.0 to 3.6V, 10% – 90%	10	-	50	ns
TFallL	Fall Time, Strong Mode Low Supply, Cload = 50 pF, All Ports	Vdd = 1.71 to 3.0V, 10% – 90%	10	-	70	ns

Figure 12. GPIO Timing Diagram





AC I2C Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 33. AC Characteristics of the I2C SDA and SCL Pins

Symbol	Description		Standard Mode		Fast Mode	
		Min	Max	Min	Max	
F _{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz
T _{HDSTAI2C}	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	-	0.6	-	μS
T _{LOWI2C}	LOW Period of the SCL Clock	4.7	-	1.3	-	μS
T _{HIGHI2C}	HIGH Period of the SCL Clock	4.0	-	0.6	-	μS
T _{SUSTAI2C}	Setup Time for a Repeated START Condition	4.7	-	0.6	-	μS
T _{HDDATI2C}	Data Hold Time	0	-	0		μS
T _{SUDATI2C}	Data Setup Time	250	1	100 ^[11]	1	ns
T _{SUSTOI2C}	Setup Time for STOP Condition	4.0	-	0.6	-	μS
T _{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	_	1.3	-	μS
T _{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	-	-	0	50	ns



Note

11. A Fast-Mode I2C-bus device can be used in a Standard Mode I2C-bus system, but the requirement t_{SU:DAT} ≥ 250 ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + t_{SU:DAT} = 1000 + 250 = 1250 ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.



Table 34. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Тур	Max	Units
F _{SCLK}	SCLK clock frequency	$\begin{array}{l} V_{DD} \geq 2.4V \\ V_{DD} < 2.4V \end{array}$			6 3	MHz
DC	SCLK duty cycle			50		%
T _{SETUP}	MISO to SCLK setup time	$\begin{array}{l} V_{DD} \geq 2.4V \\ V_{DD} < 2.4V \end{array}$	60 100			ns
T _{HOLD}	SCLK to MISO hold time		40			ns
T _{OUT_VAL}	SCLK to MOSI valid time				40	ns
T _{OUT_HIGH}	MOSI high time		40			ns

Table 35. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Тур	Max	Units
F _{SCLK}	SCLK clock frequency	$V_{DD} \ge 2.4V \\ V_{DD} < 2.4V$			12 6	MHz
T _{LOW}	SCLK low time		41.67			ns
T _{HIGH}	SCLK high time		41.67			ns
T _{SETUP}	MOSI to SCLK setup time		30			ns
T _{HOLD}	SCLK to MOSI hold time		50			ns
T _{SS_MISO}	SS high to MISO valid				153	ns
T _{SCLK_MISO}	SCLK to MISO valid				125	ns
T _{SS_HIGH}	SS high time				50	ns
T _{SS_CLK}	Time from SS low to first SCLK		2/SCLK			ns
T _{CLK_SS}	Time from last SCLK to SS high		2/SCLK			ns



Packaging Information

This section illustrates the packaging specifications for the CY8C20x36/46/66/96 PSoC device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled PSoC Emulator Pod Dimensions at http://www.cypress.com/design/MR10161.



Figure 15. 16-pin QFN No E-pad 3x3mm Package Outline (Sawn)

001-09116 *D





Figure 16. 24-Pin (4x4 x 0.6 mm) QFN











Figure 19. 48-Pin (7x7 mm) QFN



Important Notes

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.
- Pinned vias for thermal conduction are not required for the low power PSoC device.



Development Tool Selection

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at

http://www.cypress.com/psocdesigner and includes a free C compiler.

PSoC Programmer

PSoC Programmer is flexible enough and is used on the bench in development and is also suitable for factory programming. PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of cost at

http://www.cypress.com/psocprogrammer.

Development Kits

All development kits are sold at the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack



Device Programmers

All device programmers are purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- Three Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 38. Emulation and Programming Accessories

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment. Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Part Number	Pin Package	Flex-Pod Kit ^[15]	Foot Kit ^[16]	Adapter ^[17]
CY8C20236-24LKXI	16 QFN	CY3250-20266QFN	CY3250-16QFN-RK	See note 15
CY8C20246-24LKXI	16 QFN	CY3250-20266QFN	CY3250-16QFN-FK	See note 17
CY8C20336-24LQXI	24 QFN	CY3250-20366QFN	CY3250-24QFN-FK	See note 15
CY8C20346-24LQXI	24 QFN	CY3250-20366QFN	CY3250-24QFN-FK	See note 17
CY8C20396-24LQXI	24 QFN		Not Available	·
CY8C20436-24LQXI	32 QFN	CY3250-20466QFN	CY3250-32QFN-RK	See note 15
CY8C20446-24LQXI	32 QFN	CY3250-20466QFN	CY3250-32QFN-FK	See note 17
CY8C20466-24LQXI	32 QFN	CY3250-20466QFN	CY3250-32QFN-FK	See note 17
CY8C20496-24LQXI	32 QFN		Not Available	·
CY8C20536-24PVXI	48 SSOP	CY3250-20X66	CY3250-48SSOP-FK	See note 17
CY8C20546-24PVXI	48 SSOP	CY3250-20X66	CY3250-48SSOP-FK	See note 17
CY8C20566-24PVXI	48 SSOP	CY3250-20X66	CY3250-48SSOP-FK	See note 17
CY8C20636-24LTXI	48 QFN	CY3250-20666QFN	CY3250-48QFN-FK	See note 17
CY8C20646-24LTXI	48 QFN	CY3250-20666QFN	CY3250-48QFN-FK	See note 17
CY8C20666-24LTXI	48 QFN	CY3250-20666QFN	CY3250-48QFN-FK	See note 17

Third-Party Tools

Several tools have been specially designed by the following third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at http://www.cypress.com under Documentation > Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, refer Application Note "Debugging - Build a PSoC Emulator into Your Board - AN2323" at http://www.cypress.com/?rID2748.

Notes

16. Foot kit includes surface mount feet that can be soldered to the target PCB.

^{15.} Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.

^{17.} Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.



Ordering Information

The following table lists the CY8C20x36/46/66/96 PSoC devices' key package features and ordering codes.

Table 39. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	CapSense Blocks	Digital I/O Pins	Analog Inputs ^[18]	XRES Pin	USB
16-Pin (3x3x0.6mm) QFN	CY8C20236-24LKXI	8K	1K	1	13	13	Yes	No
16-Pin (3x3x0.6mm) QFN (Tape and Reel)	CY8C20236-24LKXIT	8K	1K	1	13	13	Yes	No
16 Pin (3x3 x 0.6 mm) QFN	CY8C20246-24LKXI	16K	2K	1	13	13	Yes	No
16 Pin (3x3 x 0.6 mm) QFN (Tape and Reel)	CY8C20246-24LKXIT	16K	2K	1	13	13	Yes	No
24-Pin (4x4x0.6mm) QFN	CY8C20336-24LQXI	8K	1K	1	20	20	Yes	No
24-Pin (4x4x0.6mm) QFN (Tape and Reel)	CY8C20336-24LQXIT	8K	1K	1	20	20	Yes	No
24 Pin (4x4 x 0.6 mm) QFN	CY8C20346-24LQXI	16K	2K	1	20	20	Yes	No
24 Pin (4x4 x 0.6 mm) QFN (Tape and Reel)	CY8C20346-24LQXIT	16K	2K	1	20	20	Yes	No
24-Pin (4x4x0.6mm) QFN	CY8C20396-24LQXI	16K	2K	1	19	19	Yes	Yes
24-Pin (4x4x0.6mm) QFN (Tape and Reel)	CY8C20396-24LQXIT	16K	2K	1	19	19	Yes	Yes
32-Pin (5x5x0.6mm) QFN	CY8C20436-24LQXI	8K	1K	1	28	28	Yes	No
32-Pin (5x5x0.6mm) QFN (Tape and Reel)	CY8C20436-24LQXIT	8K	1K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20446-24LQXI	16K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20446-24LQXIT	16K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20466-24LQXI	32K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20466-24LQXIT	32K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20496-24LQXI	16K	2K	1	25	25	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20496-24LQXIT	16K	2K	1	25	25	Yes	No
48-Pin SSOP	CY8C20536-24PVXI	8K	1K	1	36	36	Yes	No
48-Pin SSOP (Tape and Reel)	CY8C20536-24PVXIT	8K	1K	1	36	36	Yes	No
48-Pin SSOP	CY8C20546-24PVXI	16K	2K	1	36	36	Yes	No
48-Pin SSOP (Tape and Reel)	CY8C20546-24PVXIT	16K	2K	1	36	36	Yes	No
48-Pin SSOP	CY8C20566-24PVXI	32K	2K	1	36	36	Yes	No
48-Pin SSOP (Tape and Reel)	CY8C20566-24PVXIT	32K	2K	1	36	36	Yes	No
48 Pin (7x7 mm) QFN	CY8C20636-24LTXI	8K	1K	1	36	36	Yes	No
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20636-24LTXIT	8K	1K	1	36	36	Yes	No
48 Pin (7x7 mm) QFN	CY8C20646-24LTXI	16K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20646-24LTXIT	16K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN	CY8C20666-24LTXI	32K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20666-24LTXIT	32K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN (OCD) ^[4]	CY8C20066-24LTXI	32K	2K	1	36	36	Yes	Yes

Notes

18. Dual-function Digital I/O Pins also connect to the common analog mux.



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Document Number: 001-12696 Rev. *E

Revised April 24, 2009

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