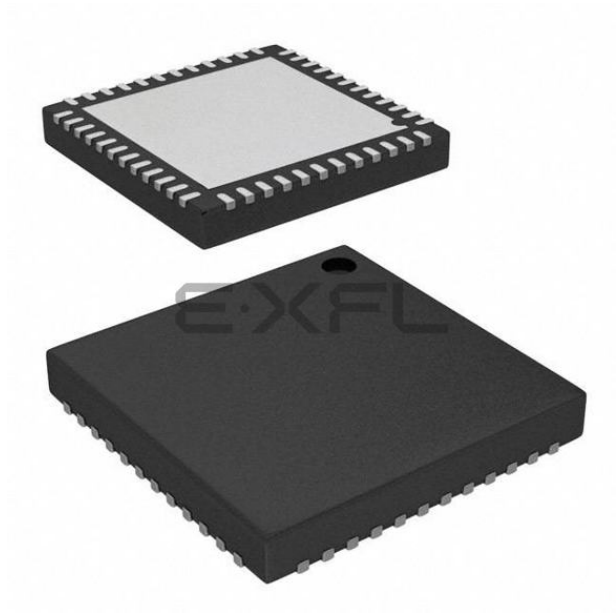

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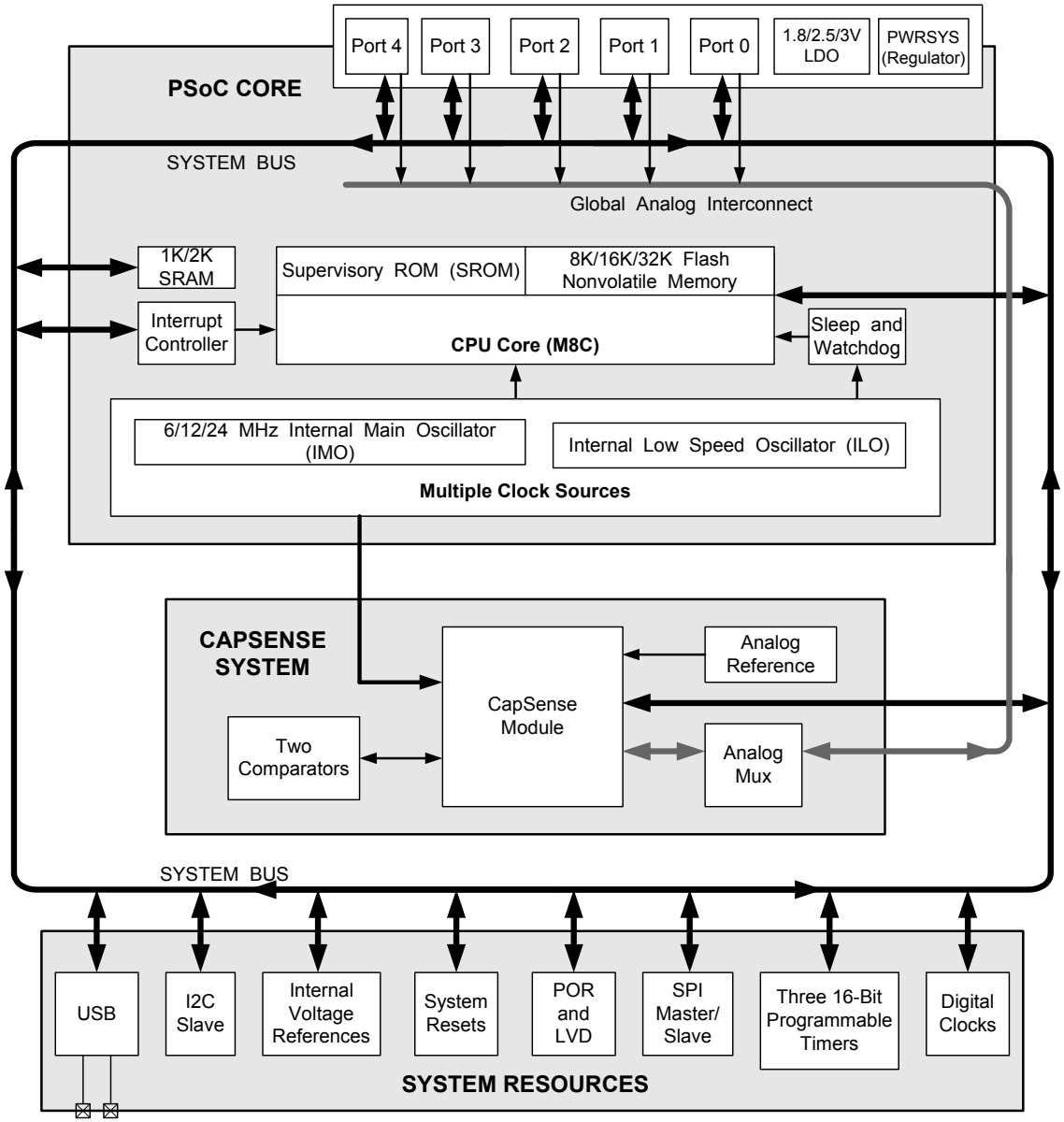
Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (32kB)
Controller Series	CY8C20xx6
RAM Size	2K x 8
Interface	I²C, SPI, USB
Number of I/O	36
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20666-24ltxit

Logic Block Diagram



Additional System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The merits of each system resource are listed here:

- The I2C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I2C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power-On-Reset) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO.
- Standard Cypress PSoC IDE tools are available for debugging the CY8C20x36/46/66/96 family of parts. However, the additional trace length and a minimal ground plane in the Flex-Pod can create noise problems that make it difficult to debug the design. A custom bonded On-Chip Debug (OCD) device is available in an 48-pin QFN package. The OCD device is recommended for debugging designs that have high current and/or high analog accuracy requirements. The QFN package is compact and is connected to the ICE through a high density connector.

Getting Started

The quickest way to understand PSoC silicon is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the PSoC® Programmable System-on-Chip™ Technical Reference Manual for CY8C20x36/46/66/96 PSoC Devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at www.cypress.com/psoc.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located here: www.cypress.com/psoc. Select Application Notes under the Documentation tab.

Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

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Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Table 1. Acronyms

Acronym	Description
AC	alternating current
API	application programming interface
CPU	central processing unit
DC	direct current
FSR	full scale range
GPIO	general purpose I/O
GUI	graphical user interface
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™
SLIMO	slow IMO
SRAM	static random access memory

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 11 on page 17 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimal.

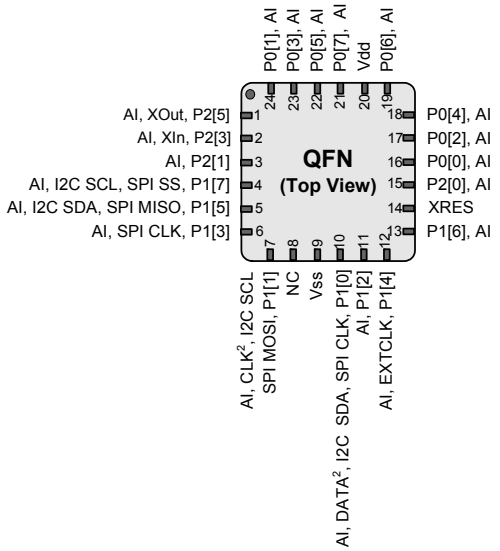
24-Pin QFN

Table 3. Pin Definitions - CY8C20336, CY8C20346 [2, 3]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I2C SCL, SPI SS
5	IOHR	I	P1[5]	I2C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK[1], I2C SCL, SPI MOSI
8			NC	No connection
9	Power		Vss	Ground connection
10	IOHR	I	P1[0]	ISSP DATA[1], I2C SDA, SPI CLK
11	IOHR	I	P1[2]	
12	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
13	IOHR	I	P1[6]	
14	Input		XRES	Active high external reset with internal pull down
15	I/O	I	P2[0]	
16	IOH	I	P0[0]	
17	IOH	I	P0[2]	
18	IOH	I	P0[4]	
19	IOH	I	P0[6]	
20	Power		Vdd	Supply voltage
21	IOH	I	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input
24	IOH	I	P0[1]	Integrating input
CP	Power		Vss	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 3. CY8C20336, CY8C20346 PSoC Device



Note
3. The center pad (CP) on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.

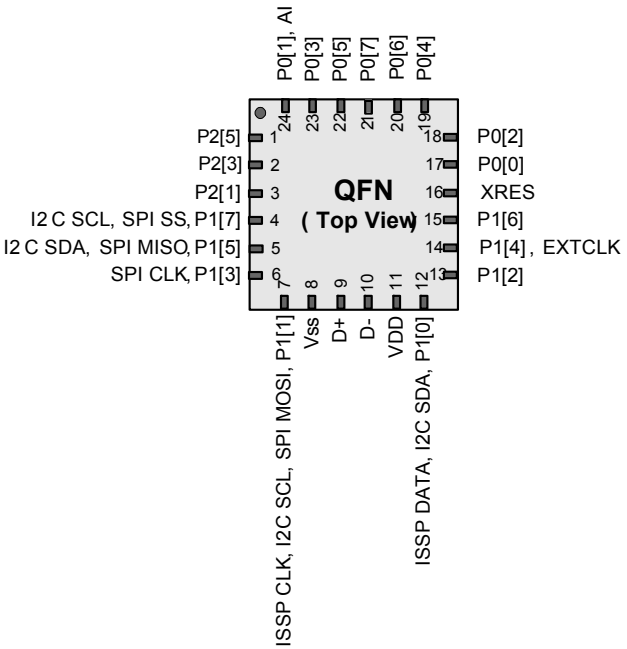
24-Pin QFN with USB

Table 4. Pin Definitions - CY8C20396 PSoC Device [2, 3]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	
2	I/O	I	P2[3]	
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I2C SCL, SPI SS
5	IOHR	I	P1[5]	I2C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK, I2C SCL, SPI MOSI
8	Power		VSS	Ground
9	I/O	I	D+	USB D+
10	I/O	I	D-	USB D-
11	Power		VDD	Supply
12	IOHR	I	P1[0]	ISSP DATA, I2C SDA
13	IOHR	I	P1[2]	
14	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
15	IOHR	I	P1[6]	
16	RESET INPUT		XRES	Active high external reset with internal pull down
17	IOH	I	P0[0]	
18	IOH	I	P0[2]	
19	IOH	I	P0[4]	
20	IOH	I	P0[6]	
21	IOH	I	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input
24	IOH	I	P0[1]	Integrating input
CP	Power		VSS	Thermal pad must be connected to Ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Figure 4. CY8C20396 PSoC Device

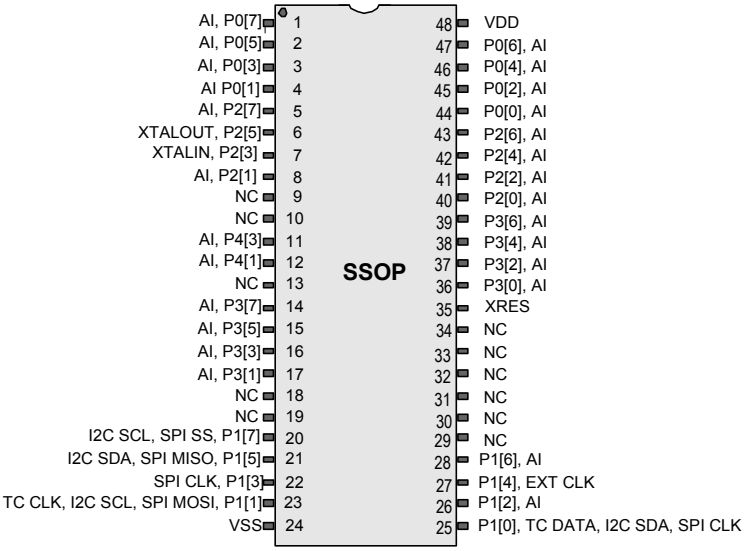


48-Pin SSOP

Table 7. Pin Definitions - CY8C20536, CY8C20546, and CY8C20566 PSoC Device[2]

Pin No.	Digital	Analog	Name	Description
1	IOH	I	P0[7]	
2	IOH	I	P0[5]	
3	IOH	I	P0[3]	
4	IOH	I	P0[1]	
5	I/O	I	P2[7]	
6	I/O	I	P2[5]	XTAL Out
7	I/O	I	P2[3]	XTAL In
8	I/O	I	P2[1]	
9			NC	No connection
10			NC	No connection
11	I/O	I	P4[3]	
12	I/O	I	P4[1]	
13			NC	No connection
14	I/O	I	P3[7]	
15	I/O	I	P3[5]	
16	I/O	I	P3[3]	
17	I/O	I	P3[1]	
18			NC	No connection
19			NC	No connection
20	IOHR	I	P1[7]	I2C SCL, SPI SS
21	IOHR	I	P1[5]	I2C SDA, SPI MISO
22	IOHR	I	P1[3]	SPI CLK
23	IOHR	I	P1[1]	TC CLK[1], I2C SCL, SPI MOSI
24			VSS	Ground Pin
25	IOHR	I	P1[0]	TC DATA[1], I2C SDA, SPI CLK
26	IOHR	I	P1[2]	
27	IOHR	I	P1[4]	EXT CLK
28	IOHR	I	P1[6]	
29			NC	No connection
30			NC	No connection
31			NC	No connection
32			NC	No connection
33			NC	No connection
34			NC	No connection
35			XRES	Active high external reset with internal pull down
36	I/O	I	P3[0]	
37	I/O	I	P3[2]	
38	I/O	I	P3[4]	
39	I/O	I	P3[6]	
40	I/O	I	P2[0]	
41	I/O	I	P2[2]	
42	I/O	I	P2[4]	
43	I/O	I	P2[6]	
44	IOH	I	P0[0]	
45	IOH	I	P0[2]	
46	IOH	I	P0[4]	
47	IOH	I	P0[6]	
48	Power		Vdd	Power Pin

Figure 6. CY8C20536, CY8C20546, and CY8C20566 PSoC Device



LEGEND A = Analog, I = Input, O = Output, NC = No Connection, H = 5 mA High Output Drive, R = Regulated Output Option.

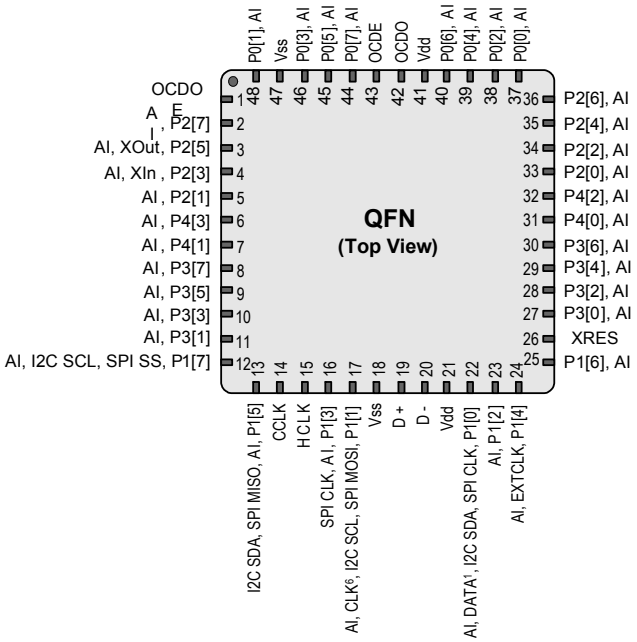
48-Pin QFN OCD

The 48-pin QFN part is for the CY8C20066 On-Chip Debug (OCD) PSoC device. Note that this part is only used for in-circuit debugging.[4]

Table 10. Pin Definitions - CY8C20066 PSoC Device [2, 3]

Pin No.	Digital	Analog	Name	Description
1			OCDOE	OCD mode direction pin
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I2C SCL, SPI SS
13	IOHR	I	P1[5]	I2C SDA, SPI MISO
14			CCLK	OCD CPU clock output
15			HCLK	OCD high speed clock output
16	IOHR	I	P1[3]	SPI CLK.
17	IOHR	I	P1[1]	ISSP CLK[1], I2C SCL, SPI MOSI
18	Power		Vss	Ground connection
19	I/O		D+	USB D+
20	I/O		D-	USB D-
21	Power		Vdd	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA(1), I2C SDA, SPI CLK
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	

Figure 9. CY8C20066 PSoC Device



Pin No.	Digital	Analog	Name	Description
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		Vdd	Supply voltage
42			OCDO	OCD even data I/O
43			OCDE	OCD odd data output
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		Vss	Ground connection
48	IOH	I	P0[1]	
CP	Power		Vss	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

Note
4. This part is available in limited quantities for In-Circuit Debugging during prototype development. It is not available in production volumes.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 12. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage Temperature	Higher storage temperatures reduces data retention time. Recommended Storage Temperature is +25°C ± 25°C. Extended duration storage temperatures above 85°C degrades reliability.	–55	+25	+125	°C
Vdd	Supply Voltage Relative to Vss		–0.5	–	+6.0	V
V_{IO}	DC Input Voltage		Vss – 0.5	–	Vdd + 0.5	V
V_{IOZ}	DC Voltage Applied to Tri-state		Vss –0.5	–	Vdd + 0.5	V
I_{MIO}	Maximum Current into any Port Pin		–25	–	+50	mA
ESD	Electro Static Discharge Voltage	Human Body Model ESD	2000	–	–	V
LU	Latch up Current	In accordance with JESD78 standard	–	–	200	mA

Operating Temperature

Table 13. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_A	Ambient Temperature		–40	–	+85	°C
T_J	Operational Die Temperature	The temperature rise from ambient to junction is package specific. Refer the table Thermal Impedances per Package on page 34. The user must limit the power consumption to comply with this requirement.	–40	–	+100	°C

Table 15. 3.0V to 5.5V DC GPIO Specifications *(continued)*

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OH10}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	IOH = 1 mA, Vdd > 2.7V, maximum of 20 mA source current in all IOs	1.20	–	–	V
V_{OL}	Low Output Voltage	IOL = 25 mA, Vdd > 3.3V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input Low Voltage		–	–	0.80	V
V_{IH}	Input High Voltage		2.00	–		V
V_H	Input Hysteresis Voltage		–	80	–	mV
I_{IL}	Input Leakage (Absolute Value)		–	0.001	1	µA
C_{PIN}	Pin Capacitance	Package and pin dependent Temp = 25°C	0.5	1.7	5	pF

Table 17. 1.71V to 2.4V DC GPIO Specifications *(continued)*

Symbol	Description	Conditions	Min	Typ	Max	Units
V_H	Input Hysteresis Voltage		–	80	–	mV
I_{IL}	Input Leakage (Absolute Value)		–	0.001	1	µA
C_{PIN}	Capacitive Load on Pins	Package and pin dependent Temp = 25°C	0.5	1.7	5	pF

Table 18.DC Characteristics – USB Interface

Symbol	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ Pull Up Resistance	With idle bus	0.900	-	1.575	kΩ
Rusba	USB D+ Pull Up Resistance	While receiving traffic	1.425	-	3.090	kΩ
Vohusb	Static Output High		2.8	-	3.6	V
Volusb	Static Output Low			-	0.3	V
Vdi	Differential Input Sensitivity		0.2	-		V
Vcm	Differential Input Common Mode Range		0.8	-	2.5	V
Vse	Single Ended Receiver Threshold		0.8	-	2.0	V
Cin	Transceiver Capacitance			-	50	pF
Iio	Hi-Z State Data Line Leakage	On D+ or D- line	-10	-	+10	µA
Rps2	PS/2 Pull Up Resistance		3	5	7	kΩ
Rext	External USB Series Resistor	In series with each USB pin	21.78	22.0	22.22	Ω

DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. DC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{SW}	Switch Resistance to Common Analog Bus		–	–	800	Ω
R_{GND}	Resistance of Initialization Switch to Vss		–	–	800	Ω

The maximum pin voltage for measuring R_{SW} and R_{GND} is 1.8V

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 20. DC Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{LPC}	Low Power Comparator (LPC) common mode	Maximum voltage limited to Vdd	0.0	–	1.8	V
I_{LPC}	LPC supply current		–	10	40	µA
V_{OSLPC}	LPC voltage offset		–	2.5	30	mV

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

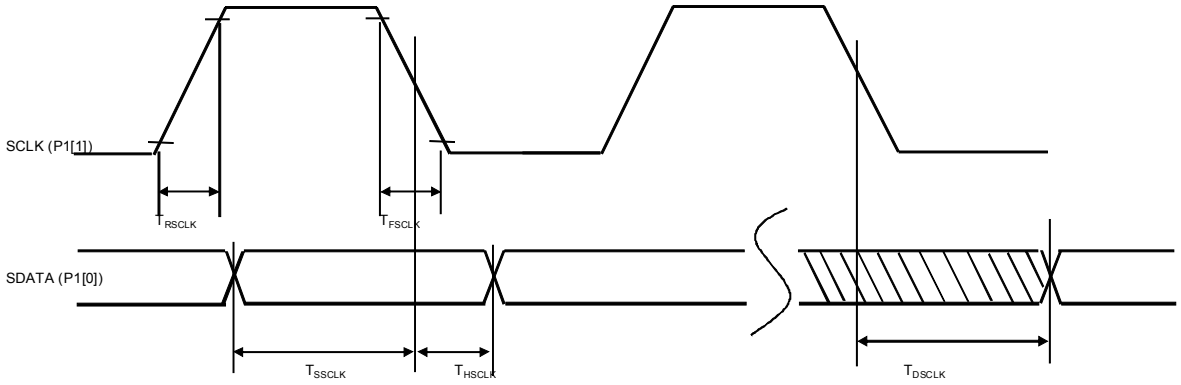
Table 25. AC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{CPU}	CPU Frequency		5.7	–	25.2	MHz
F_{32K1}	Internal Low Speed Oscillator Frequency		19	32	50	kHz
F_{IMO24}	Internal Main Oscillator Frequency at 24 MHz Setting		22.8	24	25.2	MHz
F_{IMO12}	Internal Main Oscillator Frequency at 12 MHz Setting		11.4	12	12.6	MHz
F_{IMO6}	Internal Main Oscillator Frequency at 6 MHz Setting		5.7	6.0	6.3	MHz
DC_{IMO}	Duty Cycle of IMO		40	50	60	%
T_{RAMP}	Supply Ramp Time		20	–	–	µs
T_{XRST}	External Reset Pulse Width at Power Up	After supply voltage is valid	1			ms
T_{XRST2}	External Reset Pulse Width after Power Up[10]	Applies after part has booted	10			µs

Note
10. The minimum required XRES pulse length is longer when programming the device (see Table 32 on page 28).

AC Programming Specifications

Figure 13. AC Waveform



The following table lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 32. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{RSCLK}	Rise Time of SCLK		1	–	20	ns
T_{FSCLK}	Fall Time of SCLK		1	–	20	ns
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK		40	–	–	ns
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK		40	–	–	ns
F_{SCLK}	Frequency of SCLK		0	–	8	MHz
T_{ERASEB}	Flash Erase Time (Block)		–	–	18	ms
T_{WRITE}	Flash Block Write Time		–	–	25	ms
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	3.6 < Vdd	–	–	60	ns
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	3.0 ≤ Vdd ≤ 3.6	–	–	85	ns
T_{DSCLK2}	Data Out Delay from Falling Edge of SCLK	1.71 ≤ Vdd ≤ 3.0	–	–	130	ns
T_{XRST3}	External Reset Pulse Width after Power Up	Required to enter programming mode when coming out of sleep	263	–	–	µs

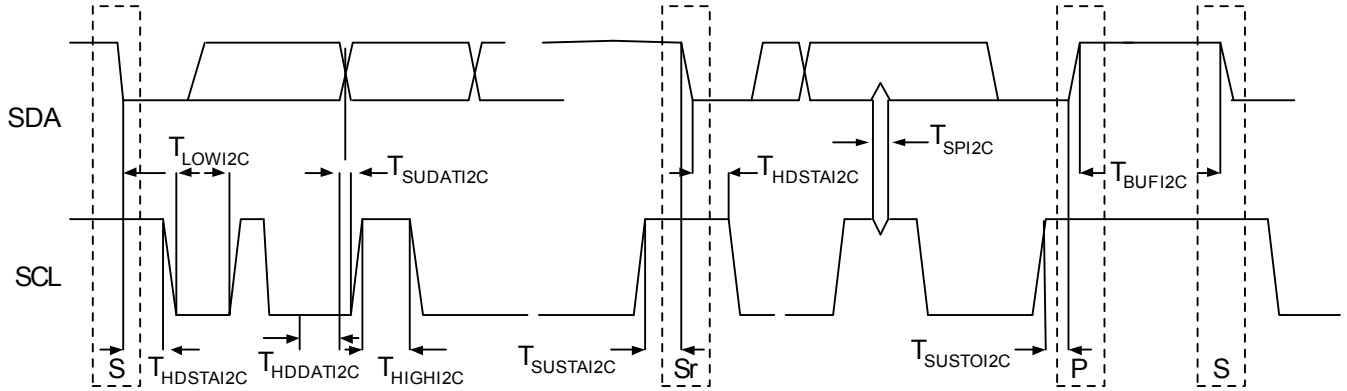
AC I2C Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 33. AC Characteristics of the I2C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs
$T_{SUDATI2C}$	Data Setup Time	250	–	100[11]	–	ns
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns

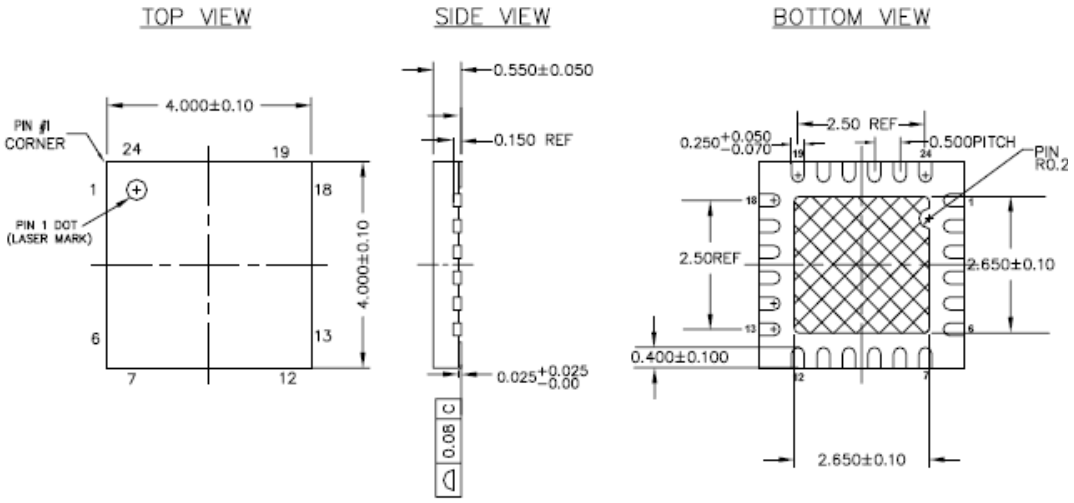
Figure 14. Definition for Timing for Fast/Standard Mode on the I^2C Bus



Note

11. A Fast-Mode I2C-bus device can be used in a Standard Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Figure 16. 24-Pin (4x4 x 0.6 mm) QFN

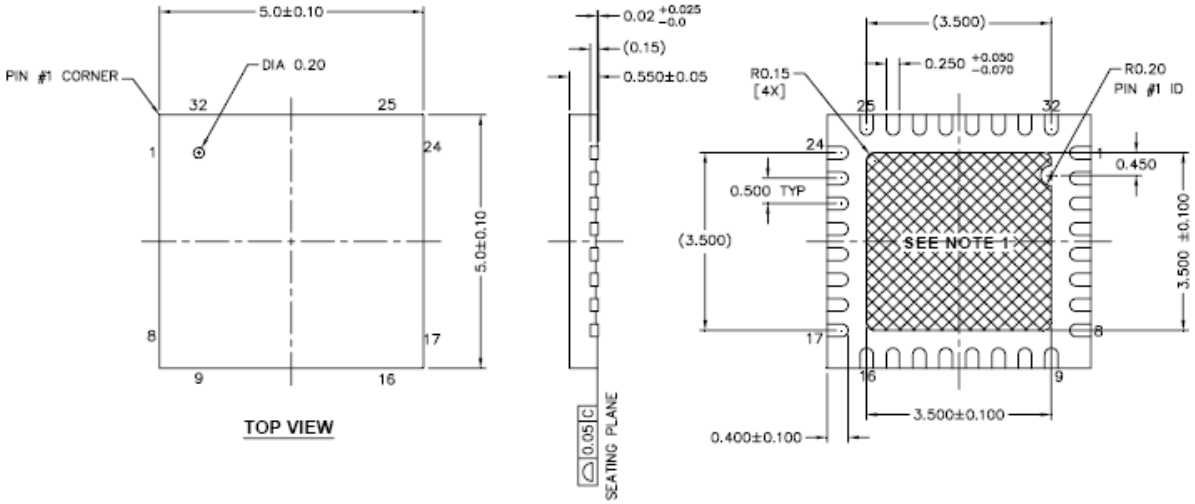


NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. UNIT PACKAGE WEIGHT : 0.024 grams
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *B

Figure 17. 32-Pin (5x5 x 0.6 mm) QFN



TOP VIEW

SIDE VIEW

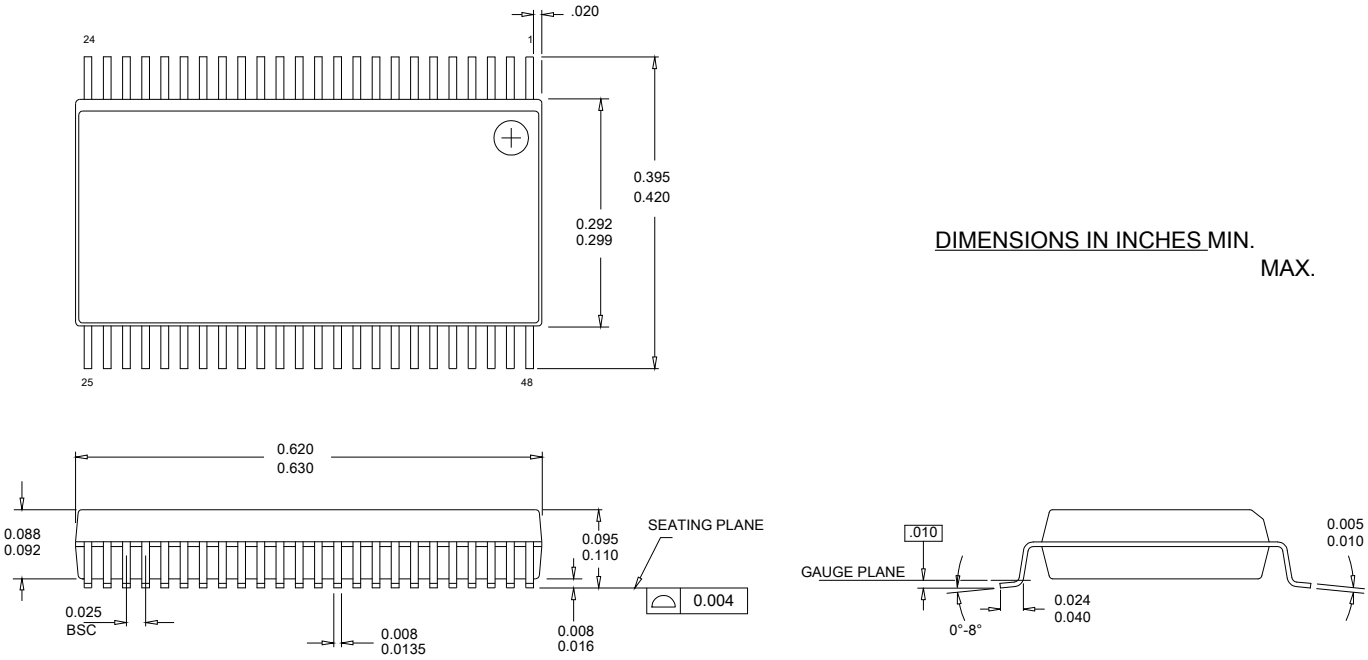
BOTTOM VIEW

NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

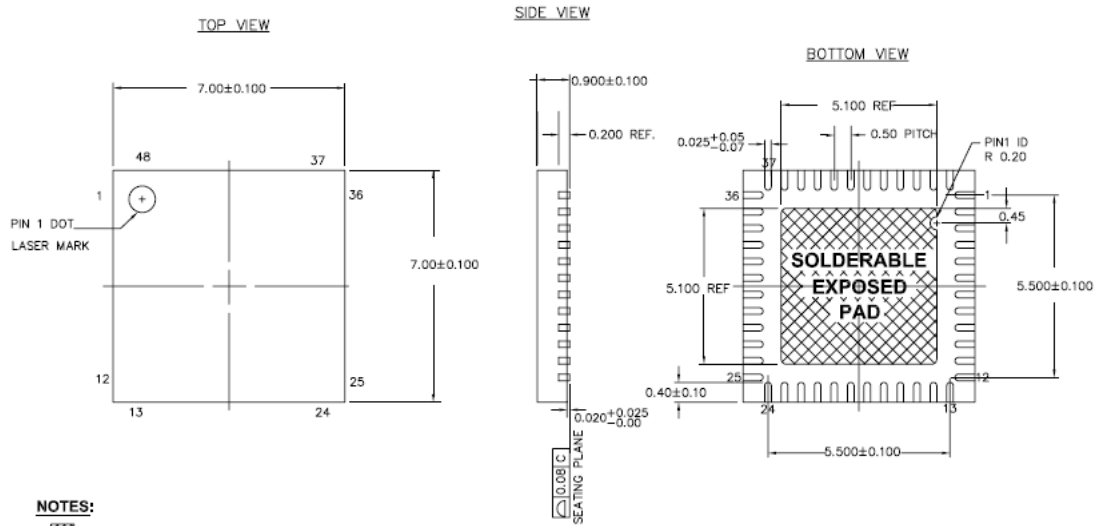
001-42168 *C

Figure 18. 48-Pin (300 MIL) SSOP



51-85061 *C

Figure 19. 48-Pin (7x7 mm) QFN



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *C

Important Notes

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.
- Pinned vias for thermal conduction are not required for the low power PSoC device.

Thermal Impedances

Table 36. Thermal Impedances per Package

Package	Typical θ_{JA} [12]
16 QFN	32.69°C/W
24 QFN[13]	20.90°C/W
32 QFN[13]	19.51°C/W
48 SSOP	69°C/W
48 QFN[13]	17.68°C/W

Solder Reflow Peak Temperature

This table lists the minimum solder reflow peak temperature to achieve good solderability.

Table 37. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature[14]	Maximum Peak Temperature
16 QFN	240°C	260°C
24 QFN	240°C	260°C
32 QFN	240°C	260°C
48 SSOP	220°C	260°C
48 QFN	240°C	260°C

Notes
12. $T_J = T_A + \text{Power} \times \theta_{JA}$.
13. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.
14. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Development Tool Selection

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com/psocdesigner and includes a free C compiler.

PSoC Programmer

PSoC Programmer is flexible enough and is used on the bench in development and is also suitable for factory programming. PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of cost at http://www.cypress.com/psocprogrammer.

Development Kits

All development kits are sold at the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack

Device Programmers

All device programmers are purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- Three Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment.
Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 38. Emulation and Programming Accessories

Part Number	Pin Package	Flex-Pod Kit[15]	Foot Kit[16]	Adapter[17]
CY8C20236-24LKXI	16 QFN	CY3250-20266QFN	CY3250-16QFN-RK	See note 15
CY8C20246-24LKXI	16 QFN	CY3250-20266QFN	CY3250-16QFN-FK	See note 17
CY8C20336-24LQXI	24 QFN	CY3250-20366QFN	CY3250-24QFN-FK	See note 15
CY8C20346-24LQXI	24 QFN	CY3250-20366QFN	CY3250-24QFN-FK	See note 17
CY8C20396-24LQXI	24 QFN	Not Available		
CY8C20436-24LQXI	32 QFN	CY3250-20466QFN	CY3250-32QFN-RK	See note 15
CY8C20446-24LQXI	32 QFN	CY3250-20466QFN	CY3250-32QFN-FK	See note 17
CY8C20466-24LQXI	32 QFN	CY3250-20466QFN	CY3250-32QFN-FK	See note 17
CY8C20496-24LQXI	32 QFN	Not Available		
CY8C20536-24PVXI	48 SSOP	CY3250-20X66	CY3250-48SSOP-FK	See note 17
CY8C20546-24PVXI	48 SSOP	CY3250-20X66	CY3250-48SSOP-FK	See note 17
CY8C20566-24PVXI	48 SSOP	CY3250-20X66	CY3250-48SSOP-FK	See note 17
CY8C20636-24LTXI	48 QFN	CY3250-20666QFN	CY3250-48QFN-FK	See note 17
CY8C20646-24LTXI	48 QFN	CY3250-20666QFN	CY3250-48QFN-FK	See note 17
CY8C20666-24LTXI	48 QFN	CY3250-20666QFN	CY3250-48QFN-FK	See note 17

Third-Party Tools

Several tools have been specially designed by the following third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at http://www.cypress.com under Documentation > Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, refer Application Note “Debugging - Build a PSoC Emulator into Your Board - AN2323” at http://www.cypress.com/?rID2748.

Notes
15. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
16. Foot kit includes surface mount feet that can be soldered to the target PCB.
17. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

Ordering Information

The following table lists the CY8C20x36/46/66/96 PSoC devices' key package features and ordering codes.

Table 39. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	CapSense Blocks	Digital I/O Pins	Analog Inputs[18]	XRES Pin	USB
16-Pin (3x3x0.6mm) QFN	CY8C20236-24LKXI	8K	1K	1	13	13	Yes	No
16-Pin (3x3x0.6mm) QFN (Tape and Reel)	CY8C20236-24LKXIT	8K	1K	1	13	13	Yes	No
16 Pin (3x3 x 0.6 mm) QFN	CY8C20246-24LKXI	16K	2K	1	13	13	Yes	No
16 Pin (3x3 x 0.6 mm) QFN (Tape and Reel)	CY8C20246-24LKXIT	16K	2K	1	13	13	Yes	No
24-Pin (4x4x0.6mm) QFN	CY8C20336-24LQXI	8K	1K	1	20	20	Yes	No
24-Pin (4x4x0.6mm) QFN (Tape and Reel)	CY8C20336-24LQXIT	8K	1K	1	20	20	Yes	No
24 Pin (4x4 x 0.6 mm) QFN	CY8C20346-24LQXI	16K	2K	1	20	20	Yes	No
24 Pin (4x4 x 0.6 mm) QFN (Tape and Reel)	CY8C20346-24LQXIT	16K	2K	1	20	20	Yes	No
24-Pin (4x4x0.6mm) QFN	CY8C20396-24LQXI	16K	2K	1	19	19	Yes	Yes
24-Pin (4x4x0.6mm) QFN (Tape and Reel)	CY8C20396-24LQXIT	16K	2K	1	19	19	Yes	Yes
32-Pin (5x5x0.6mm) QFN	CY8C20436-24LQXI	8K	1K	1	28	28	Yes	No
32-Pin (5x5x0.6mm) QFN (Tape and Reel)	CY8C20436-24LQXIT	8K	1K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20446-24LQXI	16K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20446-24LQXIT	16K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20466-24LQXI	32K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20466-24LQXIT	32K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20496-24LQXI	16K	2K	1	25	25	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20496-24LQXIT	16K	2K	1	25	25	Yes	No
48-Pin SSOP	CY8C20536-24PVXI	8K	1K	1	36	36	Yes	No
48-Pin SSOP (Tape and Reel)	CY8C20536-24PVXIT	8K	1K	1	36	36	Yes	No
48-Pin SSOP	CY8C20546-24PVXI	16K	2K	1	36	36	Yes	No
48-Pin SSOP (Tape and Reel)	CY8C20546-24PVXIT	16K	2K	1	36	36	Yes	No
48-Pin SSOP	CY8C20566-24PVXI	32K	2K	1	36	36	Yes	No
48-Pin SSOP (Tape and Reel)	CY8C20566-24PVXIT	32K	2K	1	36	36	Yes	No
48 Pin (7x7 mm) QFN	CY8C20636-24LTXI	8K	1K	1	36	36	Yes	No
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20636-24LTXIT	8K	1K	1	36	36	Yes	No
48 Pin (7x7 mm) QFN	CY8C20646-24LTXI	16K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20646-24LTXIT	16K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN	CY8C20666-24LTXI	32K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20666-24LTXIT	32K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN (OCD)[4]	CY8C20066-24LTXI	32K	2K	1	36	36	Yes	Yes

Notes
18. Dual-function Digital I/O Pins also connect to the common analog mux.

Document History Page

Document Title: CY8C20x36/46/66/96 CapSense® Applications Document Number: 001-12696				
Revision	**ECN**	**Origin of Change**	**Submission Date**	**Description of Change**
**	766857	HMT	See ECN	New silicon and document (Revision **).
*A	1242866	HMT	See ECN	Add features. Update all applicable sections. Update specs. Fix 24-pin QFN pinout moving pins inside. Update package revisions. Update and add to Emulation and Programming Accessories table.
*B	2174006	AESA	See ECN	Added 48-Pin SSOP Part Pinout Modified symbol R_{VDD} to R_{GND} in Table DC Analog Mux Bus Specification Added footnote in Table DC Analog Mux Bus Specification Added 16K FLASH Parts. Updated Notes, Package Diagrams and Ordering Information table. Updated Thermal Impedance and Solder Reflow tables
*C	2587518	TOF/JASM/MNU/ HMT	10/13/08	Converted from Preliminary to Final Fixed broken links. Updated data sheet template. Added operating voltage ranges with USB ADC resolution changed from 10-bit to 8-bit Included ADC specifications table Included Comparator specification table Included Voh7, Voh8, Voh9, Voh10 specs Flash data retention – condition added to Note Input leakage spec changed to 1 µA max GPIO rise time for ports 0,1 and ports 2,3 made common AC Programming specifications updated Included AC Programming cycle timing diagram AC SPI specification updated The VIH for 3.0<Vdd<2.4 changed to 1.6 from 2.0 Added USB specification Added SPI CLK to P1[0] Updated package diagrams Updated thermal impedances for QFN packages Updated F_{GPIO} parameter in Table 23 Updated voltage ranges for F_{SPIM} and F_{SPIS} in Table 30 Update Development Tools, add Designing with PSoC Designer. Edit, fix links, notes and table format. Update R_{IN} formula, fix TRise parameter names in GPIO figure, fix Switch Rate note. Update maximum data in Table 20. DC POR and LVD Specifications.
*D	2649637	SNV/AESA	03/17/2009	Changed title to “CY8C20x36/46/66, CY8C20396 CapSense™ Applications”. Updated data sheet Features, pin information, and ordering information sections. Updated package diagram 001-42168 to *C.
*E	2700196	SNV/PYRS	04/30/2009	Added part numbers CY8C20496, CY8C20536, CY8C20546, CY8C20636, CY8C20646 Updated Features on page 1 Added 48-Pin QFN without USB pin Diagram and Pin Definition table Added 32-Pin QFN (with USB) package Added SPI Master and Slave AC Specificatons Updated Emulations and Programming Accessories Table on page 33 Updated Ordering Information on page 37 Removed reference to Hi-Tech C Compiler in Development Tool Selection on page 35