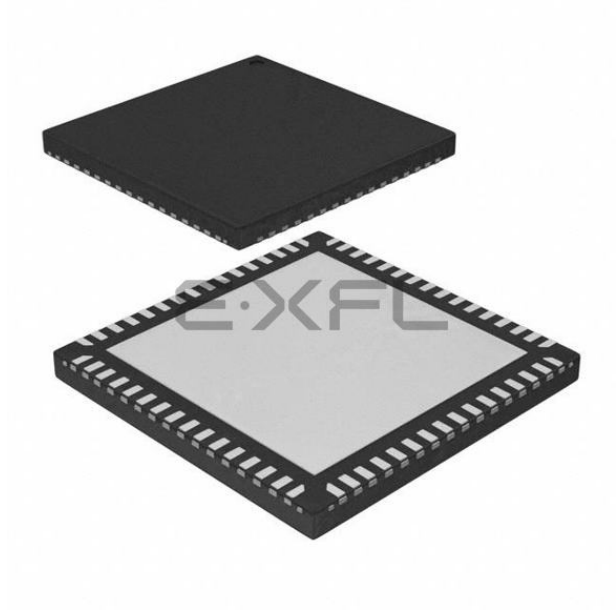

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega128d3-mh

6.4 ALU - Arithmetic Logic Unit

The arithmetic logic unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed. The ALU operates in direct connection with all 32 general purpose registers. In a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed and the result is stored in the register file. After an arithmetic or logic operation, the status register is updated to reflect information about the result of the operation.

ALU operations are divided into three main categories – arithmetic, logical, and bit functions. Both 8- and 16-bit arithmetic is supported, and the instruction set allows for efficient implementation of 32-bit aritmetic. The hardware multiplier supports signed and unsigned multiplication and fractional format.

6.4.1 Hardware Multiplier

The multiplier is capable of multiplying two 8-bit numbers into a 16-bit result. The hardware multiplier supports different variations of signed and unsigned integer and fractional numbers:

- Multiplication of unsigned integers
- Multiplication of signed integers
- Multiplication of a signed integer with an unsigned integer
- Multiplication of unsigned fractional numbers
- Multiplication of signed fractional numbers
- Multiplication of a signed fractional number with an unsigned one

A multiplication takes two CPU clock cycles.

6.5 Program Flow

After reset, the CPU starts to execute instructions from the lowest address in the flash programmemory ‘0.’ The program counter (PC) addresses the next instruction to be fetched.

Program flow is provided by conditional and unconditional jump and call instructions capable of addressing the whole address space directly. Most AVR instructions use a 16-bit word format, while a limited number use a 32-bit format.

During interrupts and subroutine calls, the return address PC is stored on the stack. The stack is allocated in the general data SRAM, and consequently the stack size is only limited by the total SRAM size and the usage of the SRAM. After reset, the stack pointer (SP) points to the highest address in the internal SRAM. The SP is read/write accessible in the I/O memory space, enabling easy implementation of multiple stacks or stack areas. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR CPU.

6.6 Status Register

The status register (SREG) contains information about the result of the most recently executed arithmetic or logic instruction. This information can be used for altering program flow in order to perform conditional operations. Note that the status register is updated after all ALU operations, as specified in the instruction set reference. This will in many cases remove the need for using the dedicated compare instructions, resulting in faster and more compact code.

The status register is not automatically stored when entering an interrupt routine nor restored when returning from an interrupt. This must be handled by software.

The status register is accessible in the I/O memory space.

6.7 Stack and Stack Pointer

The stack is used for storing return addresses after interrupts and subroutine calls. It can also be used for storing temporary data. The Stack Pointer (SP) register always points to the top of the stack. It is implemented as two 8-bit registers that are accessible in the I/O memory space. Data are pushed and popped from the stack using the PUSH and POP instructions. The stack grows from a higher memory location to a lower memory location. This implies that pushing data onto the stack decreases the SP, and popping data off the stack increases the SP. The SP is automatically loaded

13. Interrupts and Programmable Multilevel Interrupt Controller

13.1 Features

- Short and predictable interrupt response time
- Separate interrupt configuration and vector address for each interrupt
- Programmable multilevel interrupt controller
  - Interrupt prioritizing according to level and vector address
  - Three selectable interrupt levels for all interrupts: low, medium, and high
  - Selectable, round-robin priority scheme within low-level interrupts
  - Non-maskable interrupts for critical functions
- Interrupt vectors optionally placed in the application section or the boot loader section

13.2 Overview

Interrupts signal a change of state in peripherals, and this can be used to alter program execution. Peripherals can have one or more interrupts, and all are individually enabled and configured. When an interrupt is enabled and configured, it will generate an interrupt request when the interrupt condition is present. The programmable multilevel interrupt controller (PMIC) controls the handling and prioritizing of interrupt requests. When an interrupt request is acknowledged by the PMIC, the program counter is set to point to the interrupt vector, and the interrupt handler can be executed.

All peripherals can select between three different priority levels for their interrupts: low, medium, and high. Interrupts are prioritized according to their level and their interrupt vector address. Medium-level interrupts will interrupt low-level interrupt handlers. High-level interrupts will interrupt both medium- and low-level interrupt handlers. Within each level, the interrupt priority is decided from the interrupt vector address, where the lowest interrupt vector address has the highest interrupt priority. Low-level interrupts have an optional round-robin scheduling scheme to ensure that all interrupts are serviced within a certain amount of time.

Non-maskable interrupts (NMI) are also supported, and can be used for system critical functions.

13.3 Interrupt Vectors

The interrupt vector is the sum of the peripheral's base interrupt address and the offset address for specific interrupts in each peripheral. The base addresses for the Atmel AVR XMEGA D3 devices are shown in Table 13-1 on page 29. Offset addresses for each interrupt available in the peripheral are described for each peripheral in the XMEGA D manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in Table 13-1 on page 29. The program address is the word address.

14. I/O Ports

14.1 Features

- 50 general purpose input and output pins with individual configuration
- Output driver with configurable driver and pull settings:
  - Totem-pole
  - Wired-AND
  - Wired-OR
  - Bus-keeper
  - Inverted I/O
- Input with synchronous and/or asynchronous sensing with interrupts and events
  - Sense both edges
  - Sense rising edges
  - Sense falling edges
  - Sense low level
- Optional pull-up and pull-down resistor on input and Wired-OR/AND configuration
- Asynchronous pin change sensing that can wake the device from all sleep modes
- Two port interrupts with pin masking per I/O port
- Efficient and safe access to port pins
  - Hardware read-modify-write through dedicated toggle/clear/set registers
  - Configuration of multiple pins in a single operation
  - Mapping of port registers into bit-accessible I/O memory space
- Peripheral clocks output on port pin
- Real-time counter clock output to port pin
- Event channels can be output on port pin
- Remapping of digital peripheral pin functions
  - Selectable USART, SPI, and timer/counter input/output pin locations

14.2 Overview

One port consists of up to eight port pins: pin 0 to 7. Each port pin can be configured as input or output with configurable driver and pull settings. They also implement synchronous and asynchronous input sensing with interrupts and events for selectable pin change conditions. Asynchronous pin-change sensing means that a pin change can wake the device from all sleep modes, included the modes where no clocks are running.

All functions are individual and configurable per pin, but several pins can be configured in a single operation. The pins have hardware read-modify-write (RMW) functionality for safe and correct change of drive value and/or pull resistor configuration. The direction of one port pin can be changed without unintentionally changing the direction of any other pin.

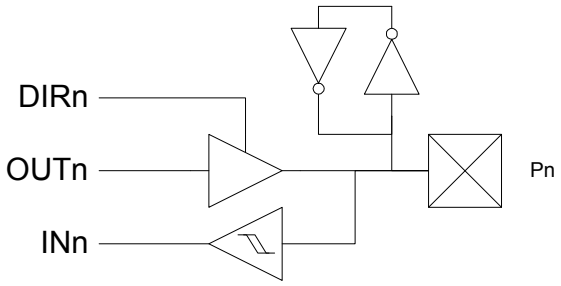
The port pin configuration also controls input and output selection of other device functions. It is possible to have both the peripheral clock and the real-time clock output to a port pin, and available for external use. The same applies to events from the event system that can be used to synchronize and control external functions. Other digital peripherals, such as USART, SPI, and timer/counters, can be remapped to selectable pin locations in order to optimize pin-out versus application needs.

The notation of the ports are PORTA, PORTB, PORTC, PORTD, PORTE, PORTF, and PORTR.

14.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

Figure 14-4. I/O Configuration - Totem-pole with Bus-keeper



14.3.5 Others

Figure 14-5. Output Configuration - Wired-OR with Optional Pull-down

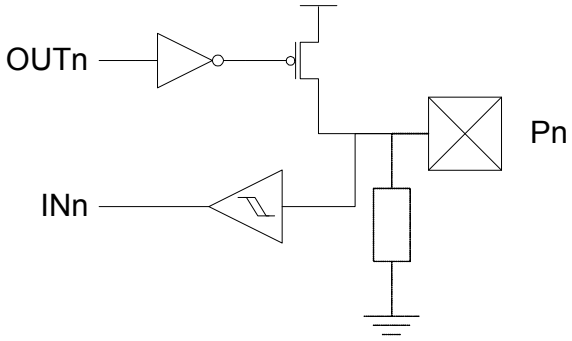


Figure 14-6. I/O Configuration - Wired-AND with Optional Pull-up

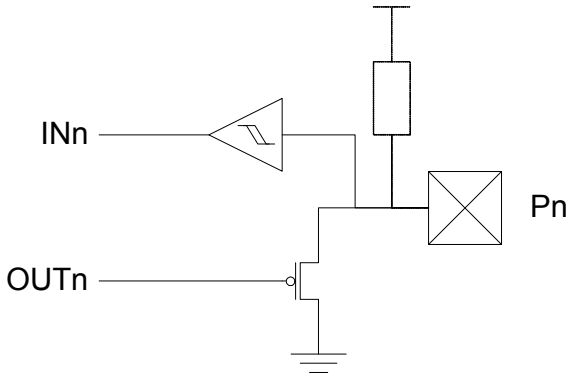


Table 32-5. Current Consumption for Modules and Peripherals

Symbol	Parameter	Condition [1]			Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator					0.9		µA
	32.768kHz int. oscillator					29		
	2MHz int. oscillator					82		
		DFLL enabled with 32.768kHz int. osc. as reference				114		
	32MHz int. oscillator					250		
		DFLL enabled with 32.768kHz int. osc. as reference				400		
	PLL	20× multiplication factor, 32MHz int. osc. DIV4 as reference				300		
	Watchdog timer					1.0		
	BOD	Continuous mode				140		
		Sampled mode, includes ULP oscillator				1.4		
	Internal 1.0V reference					180		
	Temperature sensor					175		
	ADC	16ksps V_{REF} = Ext. ref.				1.23		mA
			CURRLIMIT = LOW			1.1		
			CURRLIMIT = MEDIUM			0.98		
			CURRLIMIT = HIGH			0.87		
		75ksps V_{REF} = Ext. ref.	CURRLIMIT = LOW			1.7		
		300ksps V_{REF} = Ext. ref.				3.1		
	USART	Rx and Tx enabled, 9600 BAUD				9.7		µA
	Flash memory and EEPROM programming					5		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

32.2 Atmel ATxmega64D3

32.2.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 32-30 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 32-30. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC} + 0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	

32.2.2 General Operating Ratings

The device must operate within the ratings listed in Table 32-31 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 32-31. General Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	

Table 32-32. Operating Voltage and Frequency

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 32-8 on page 83 the frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

32.2.4 Wake-up Time from Sleep Modes

Table 32-35. Device Wake-up Time from Sleep Modes with Various System Clock Sources

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from idle, standby, and extended standby mode	External 2MHz clock		2.0		µs
		32.768kHz internal oscillator		125		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from power-save and power-down mode	External 2MHz clock		4.6		
		32.768kHz internal oscillator		330		
		2MHz internal oscillator		9.5		
		32MHz internal oscillator		5.6		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 32-9. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 32-9. Wake-up Time Definition

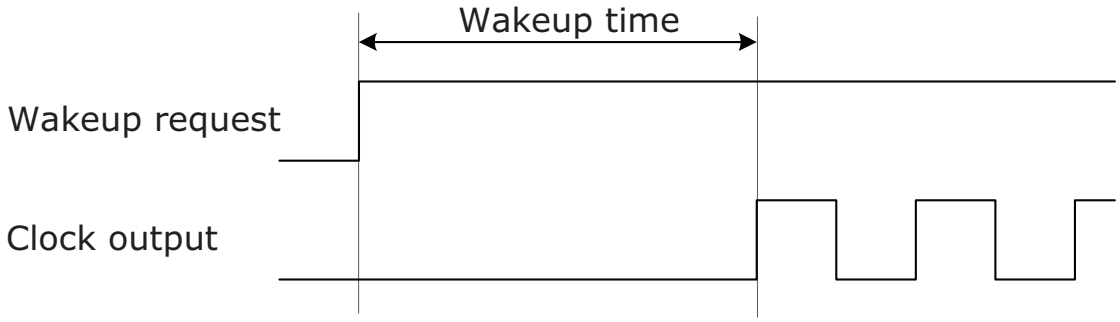


Table 32-68. Accuracy Characteristics

Symbol	Parameter	Condition [2]		Min.	Typ.	Max.	Units
RES	Resolution	12-bit resolution	Differential	8	12	12	Bits
			Single ended signed	7	11	11	
			Single ended unsigned	8	12	12	
INL [1]	Integral non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.5	1	lsb
			16ksps, all V_{REF}		0.8	2	
			300ksps, V_{REF} = 3V		0.6	1	
			300ksps, all V_{REF}		1.0	2	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.5	1	
			16ksps, all V_{REF}		1.3	2	
DNL [1]	Differential non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.3	1	lsb
			16ksps, all V_{REF}		0.5	1	
			300ksps, V_{REF} = 3V		0.3	1	
			300ksps, all V_{REF}		0.5	1	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.6	1	
			16ksps, all V_{REF}		0.6	1	
	Offset error	Differential mode	300ksps, V_{REF} = 3V		-7		mV
			Temperature drift, V_{REF} = 3V		0.01		mV/K
			Operating voltage drift		0.16		mV/V
	Gain error	Differential mode	External reference		-5		mV
			AV_{CC}/1.6		-5		
			AV_{CC}/2.0		-6		
			Bandgap		±10		
			Temperature drift		0.02		mV/K
			Operating voltage drift		2		mV/V
	Gain error	Single ended unsigned mode	External reference		-8		mV
			AV_{CC}/1.6		-8		
			AV_{CC}/2.0		-8		
			Bandgap		±10		
			Temperature drift		0.03		mV/K
			Operating voltage drift		2		mV/V

Notes:
1. Maximum numbers are based on characterization and not tested in production and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external V_{REF} is used.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
C_{XTAL1}	Parasitic capacitance XTAL1 pin				5.9		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin				8.3		
C_{LOAD}	Parasitic capacitance load				3.5		

Notes: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

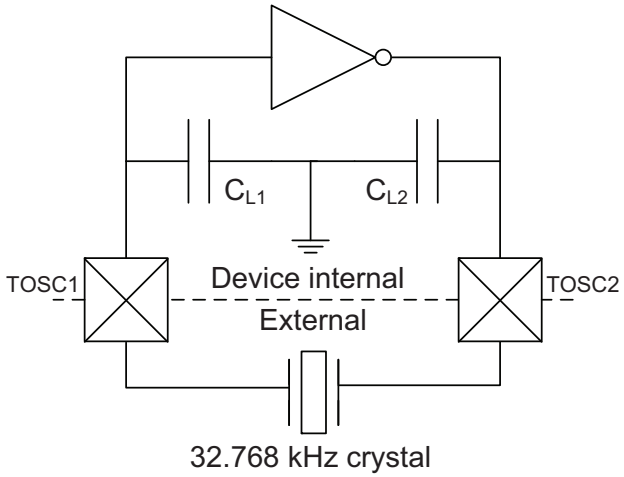
32.5.13.8 External 32.768kHz Crystal Oscillator and TOSC Characteristics

Table 32-143. External 32.768kHz Crystal Oscillator and TOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
		Crystal load capacitance 12pF			28	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			3.5		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			3.5		
	Recommended safety factor	Capacitance load matched to crystal specification	3			

Note: See Figure 32-32 for definition.

Figure 32-32. TOSC Input Capacitance



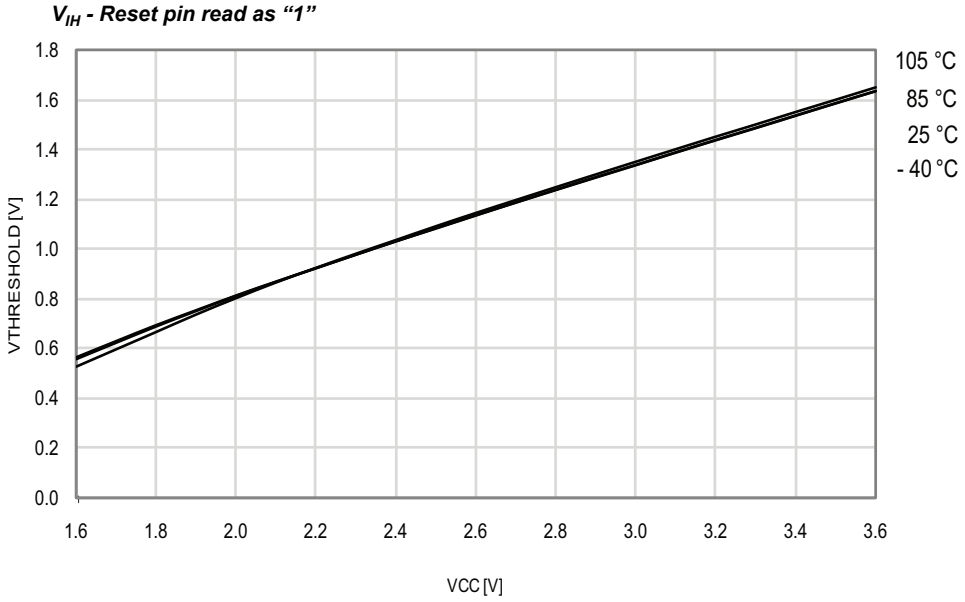
The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

Table 32-155. Accuracy Characteristics

Symbol	Parameter	Condition [1]		Min.	Typ.	Max.	Units
RES	Resolution	12-bit resolution	Differential	8	12	12	Bits
			Single ended signed	7	11	11	
			Single ended unsigned	8	12	12	
INL [2]	Integral non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.5	1	lsb
			16ksps, all V_{REF}		0.8	2	
			300ksps, V_{REF} = 3V		0.6	1	
			300ksps, all V_{REF}		1	2	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.5	1	
			16ksps, all V_{REF}		1.3	2	
DNL [2]	Differential non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.3	1	
			16ksps, all V_{REF}		0.5	1	
			300ksps, V_{REF} = 3V		0.35	1	
			300ksps, all V_{REF}		0.5	1	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.6	1	
			16ksps, all V_{REF}		0.6	1	
	Offset error	Differential mode	300ksps, V_{REF} = 3V		-7		mV
			Temperature drift, V_{REF} = 3V		0.01		mV/K
			Operating voltage drift		0.16		mV/V
	Gain error	Differential mode	External reference		-5		mV
			AV_{CC}/1.6		-5		
			AV_{CC}/2.0		-6		
			Bandgap		±10		
			Temperature drift		0.02		mV/K
			Operating voltage drift		2		mV/V
	Gain error	Single ended unsigned mode	External reference		-8		mV
			AV_{CC}/1.6		-8		
			AV_{CC}/2.0		-8		
			Bandgap		±10		
			Temperature drift		0.03		mV/K
			Operating voltage drift		2		mV/V

Notes:
1. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external V_{REF} is used.
2. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

Figure 33-53. Reset Pin Input Threshold Voltage vs. V_{CC}



33.1.8 Oscillator Characteristics

33.1.8.1 Ultra Low-power Internal Oscillator

Figure 33-54. Ultra Low-power Internal Oscillator Frequency vs. Temperature

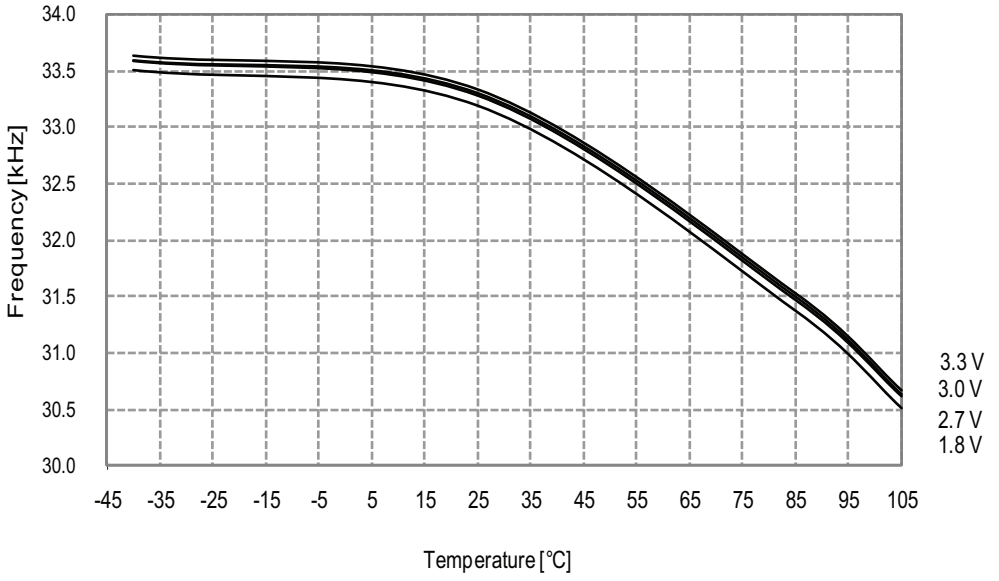


Figure 33-100. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IL} I/O pin read as "0"

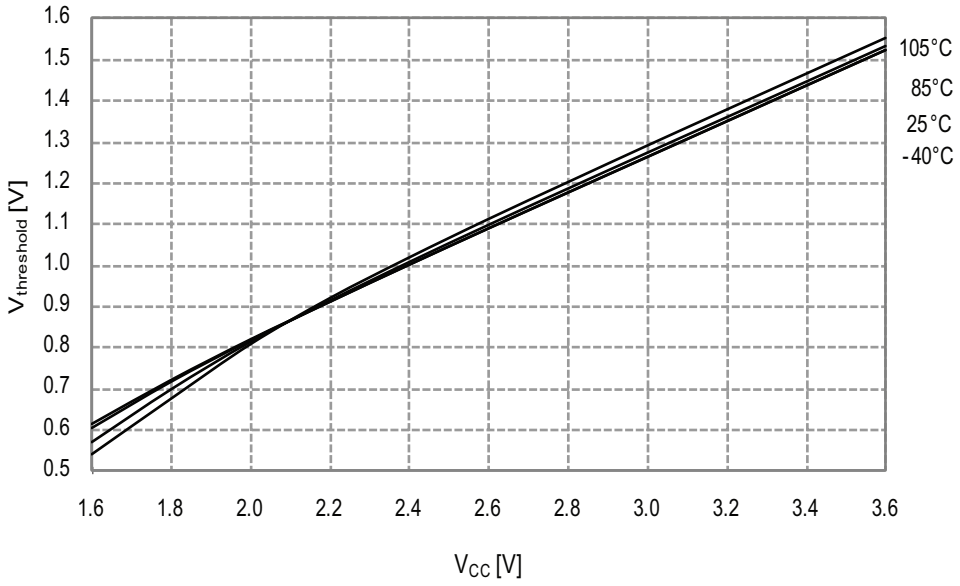
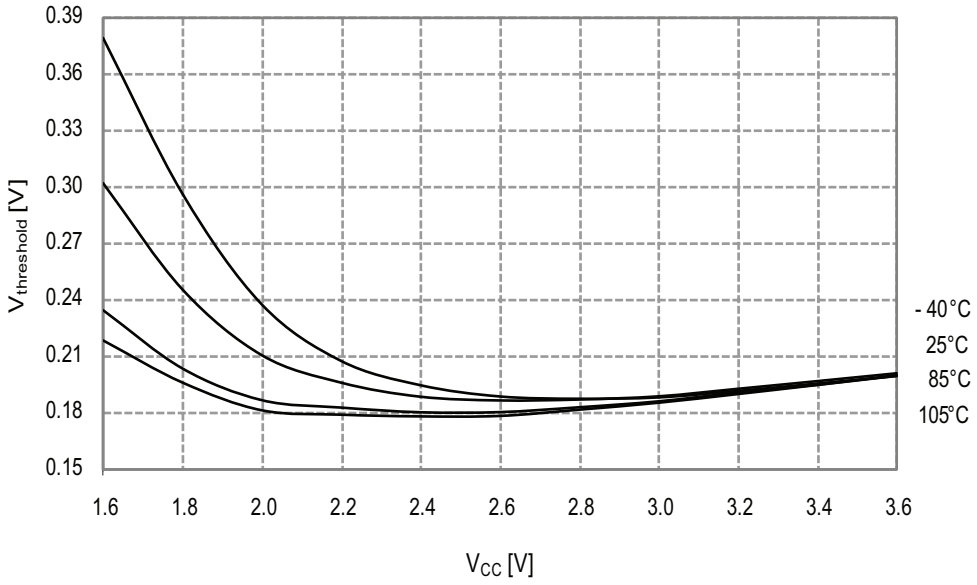


Figure 33-101. I/O Pin Input Hysteresis vs. V_{CC}



33.2.9 Two-Wire Interface Characteristics

Figure 33-140. SDA Hold Time vs. Temperature

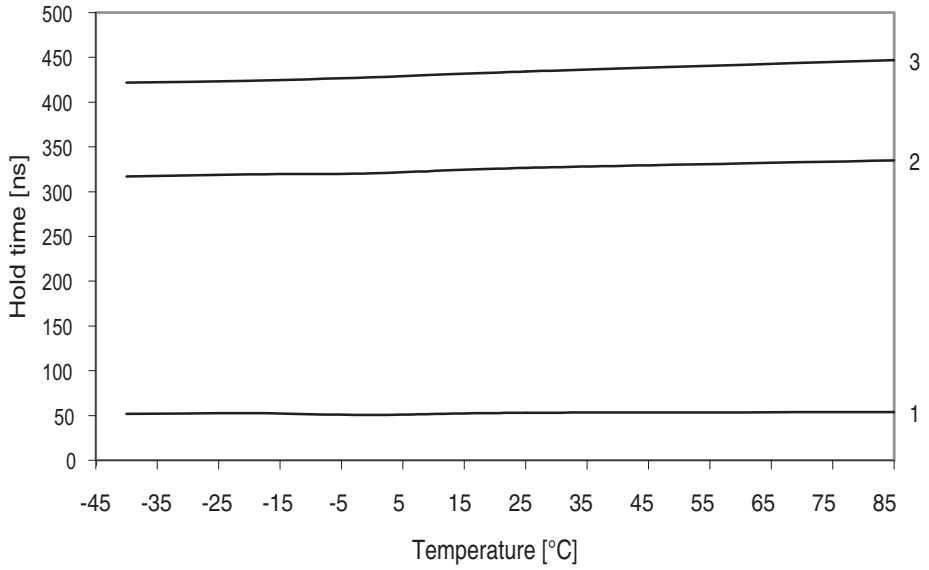


Figure 33-141. SDA Hold Time vs. Supply Voltage

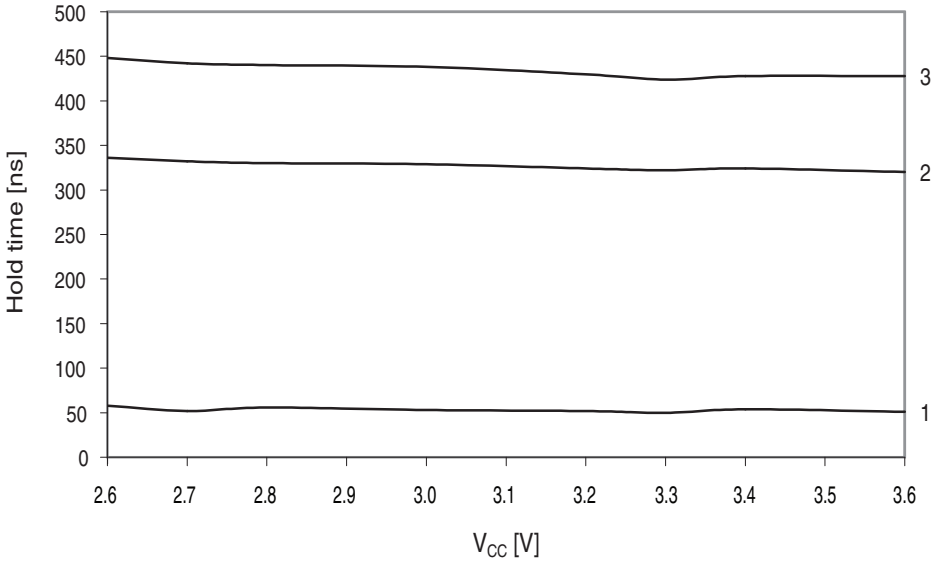


Figure 33-237.I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.0V

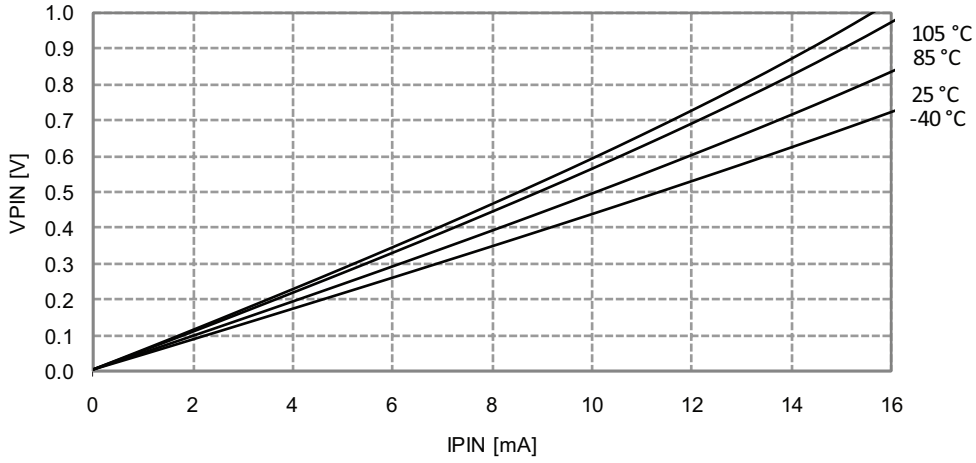


Figure 33-238.I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.3V

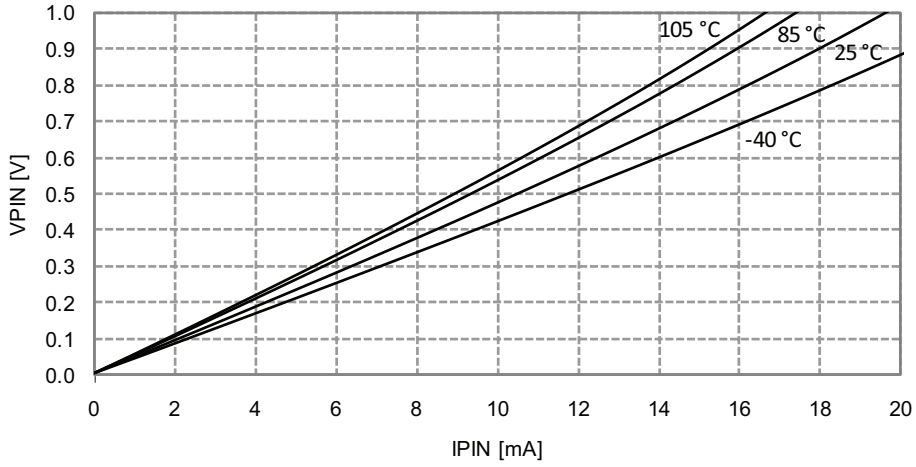


Figure 33-291.Idle Mode Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C

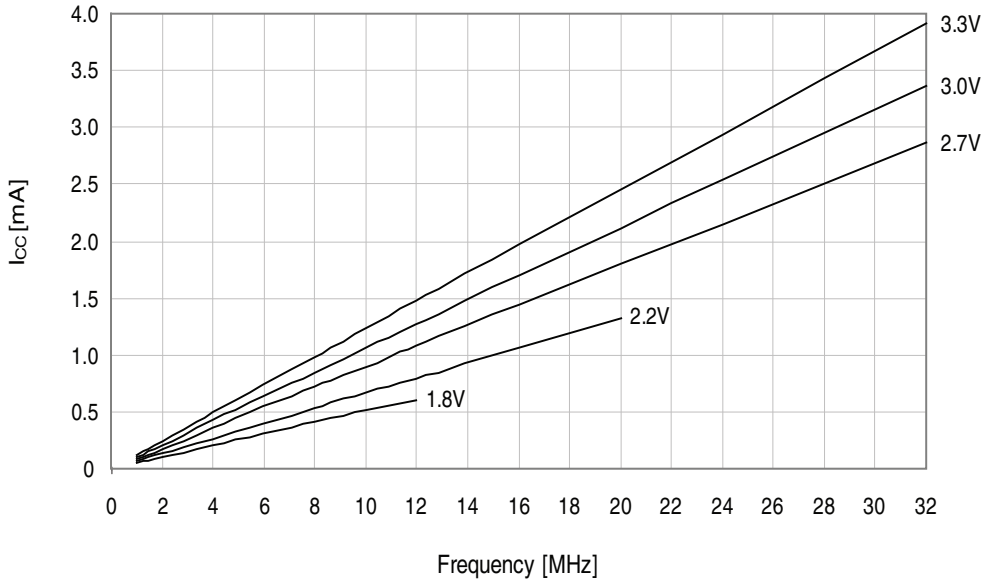
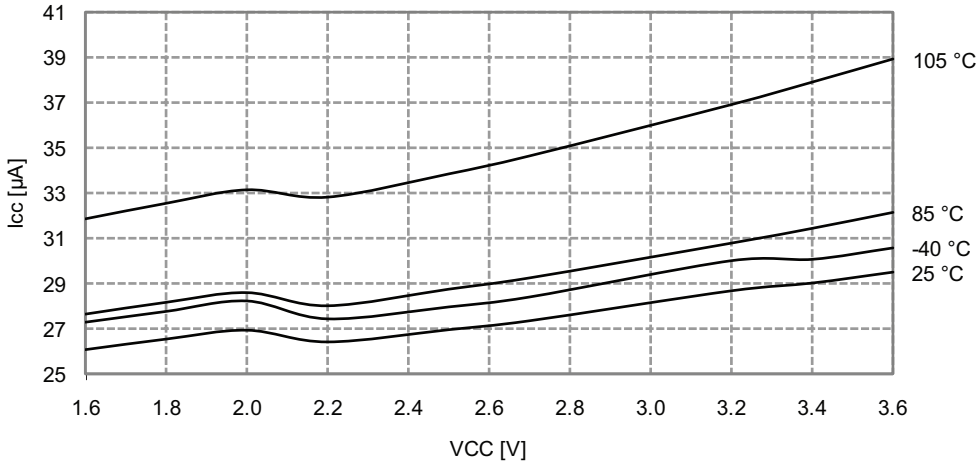


Figure 33-292.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator



33.5.1.3 Power-down Mode Supply Current

Figure 33-297.Power-down Mode Supply Current vs. V_{CC}

All functions disabled

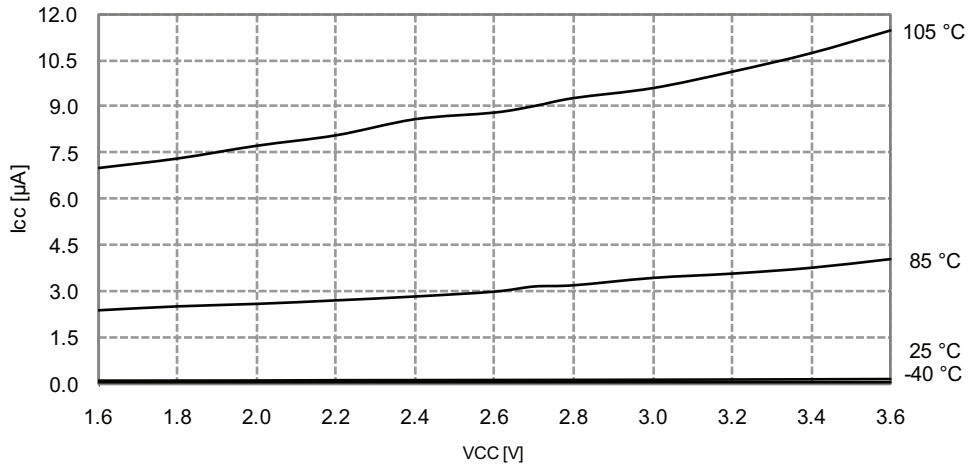


Figure 33-298.Power-down Mode Supply Current vs. V_{CC}

Watchdog and sampled BOD enabled

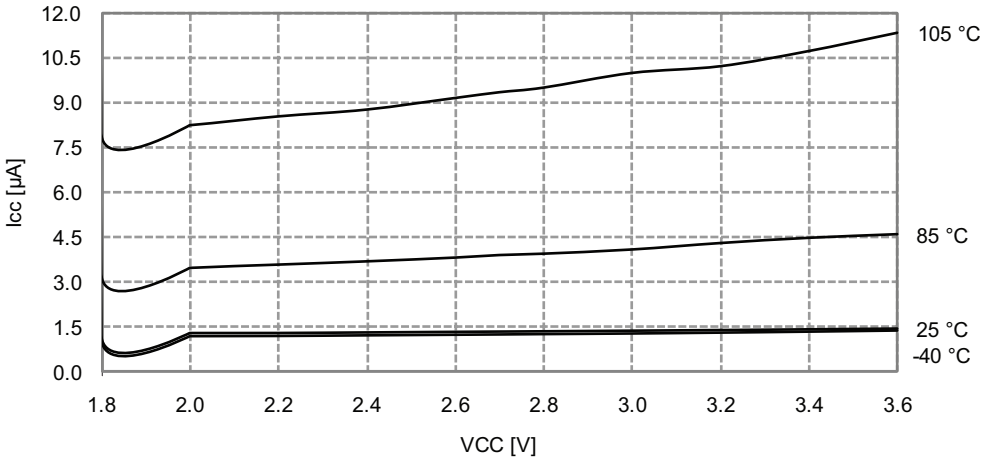


Figure 33-301.I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = 3.0V

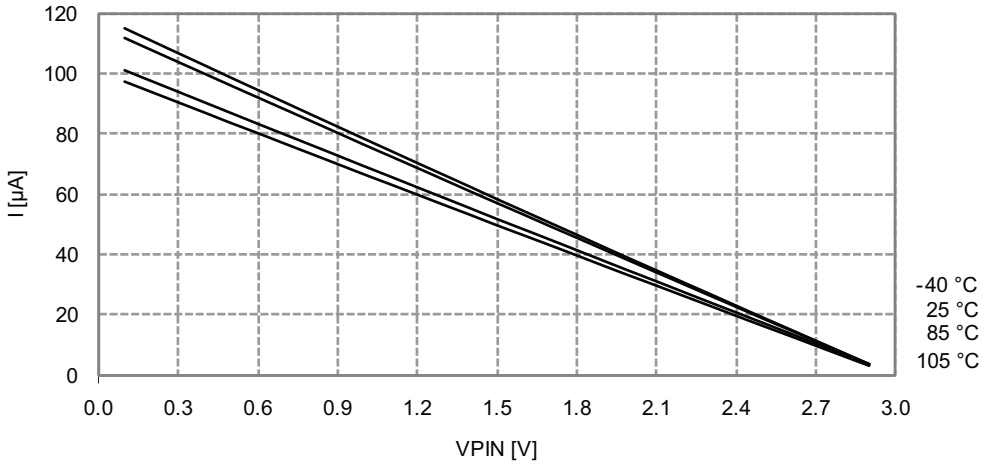
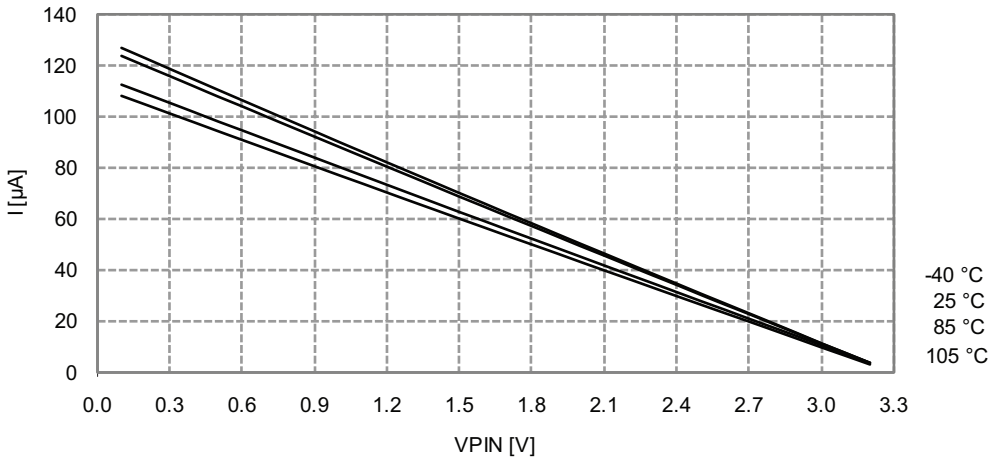


Figure 33-302.I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = 3.3V



34.2 Atmel ATxmega64D3

34.2.1 Rev. I

- AC system status flags are only valid if AC-system is enabled
- Sampled BOD in Active mode will cause noise when bandgap is used as reference
- Temperature sensor not calibrated

1. AC system status flags are only valid if AC-system is enabled

The status flags for the ac-output are updated even though the AC is not enabled which is invalid. Also, it is not possible to clear the AC interrupt flags without enabling either of the Analog comparators.

Problem fix/workaround

Software should clear the AC system flags once, after enabling the AC system before using the AC system status flags.

2. Sampled BOD in Active mode will cause noise when bandgap is used as reference

Using the BOD in sampled mode when the device is running in Active or Idle mode will add noise on the bandgap reference for ADC, DAC, and Analog Comparator.

Problem fix/workaround

If the bandgap is used as reference for either the ADC, DAC and Analog Comparator, the BOD must not be set in sampled mode.

3. Temperature sensor not calibrated

Temperature sensor factory calibration not implemented.

Problem fix/workaround

None.

34.2.2 Rev. H

Not sampled.

34.2.3 Rev. G

Not sampled.

34.2.4 Rev. F

Not sampled.

Problem fix/workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
       ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc)) &&
         /* SCL not held by slave: */
         !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

22. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

Problem fix/workaround

None.

23. TWI Data Interrupt Flag erroneously read as set

When issuing the TWI slave response command CMD=0b11, it takes one Peripheral Clock cycle to clear the data interrupt flag (DIF). A read of DIF directly after issuing the command will show the DIF still set.

Problem fix/workaround

Add one NOP instruction before checking DIF.

24. WDR instruction inside closed window will not issue reset

When a WDR instruction is execute within one ULP clock cycle after updating the window control register, the counter can be cleared without giving a system reset.

Problem fix/workaround

Wait at least one ULP clock cycle before executing a WDR instruction.

25. Non available functions and options

The below function and options are not available. Writing to any registers or fuse to try and enable or configure these functions or options will have no effect, and will be as writing to a reserved address location.

- TWIE, the TWI module on PORTE
- TWI SDAHOLD option in the TWI CTRL register is one bit

34.5.5 Rev. E

- Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously
- V_{CC} voltage scaler for AC is non-linear
- ADC gain stage cannot be used for single conversion
- ADC has increased INL error for some operating conditions
- ADC gain stage output range is limited to 2.4V
- ADC Event on compare match non-functional
- ADC propagation delay is not correct when 8× – 64× gain is used
- Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V
- Accuracy lost on first three samples after switching input to ADC gain stage
- Configuration of PGM and CWCM not as described in the XMEGA D Manual
- PWM is not restarted properly after a fault in cycle-by-cycle mode
- BOD will be enabled at any reset
- EEPROM page buffer always written when NVM DATA0 is written
- Pending full asynchronous pin change interrupts will not wake the device
- Pin configuration does not affect Analog Comparator Output
- NMI Flag for Crystal Oscillator Failure automatically cleared
- RTC Counter value not correctly read after sleep
- Pending asynchronous RTC-interrupts will not wake up device
- TWI Transmit collision flag not cleared on repeated start
- Clearing TWI Stop Interrupt Flag may lock the bus
- TWI START condition at bus timeout will cause transaction to be dropped
- TWI Data Interrupt Flag (DIF) erroneously read as set
- WDR instruction inside closed window will not issue reset
- Non available functions and options
- Sampled BOD in Active mode will cause noise when bandgap is used as reference
- Temperature sensor not calibrated
- Disabling the USART transmitter does not automatically set the TxD pin direction to input

1. Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously

If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1µs and could potentially give a wrong comparison result.

Problem fix/workaround

If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. V_{CC} voltage scaler for AC is non-linear

The 6-bit V_{CC} voltage scaler in the Analog Comparators is non-linear.