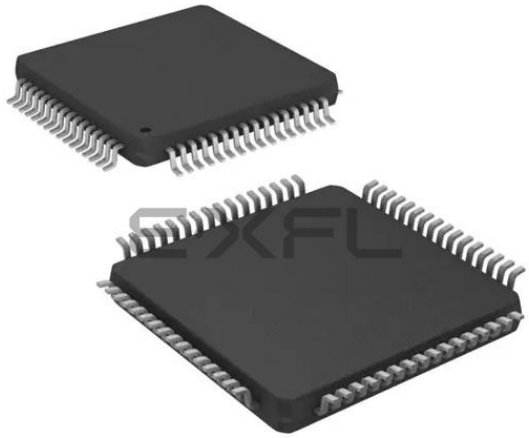

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	192KB (96K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega192d3-aur

Figure 7-2. Data Memory Map (hexadecimal address)

Byte address	ATxmega32D3
0	I/O registers (4K)
FFF	
1000	EEPROM (1K)
17FF	
	RESERVED
2000	Internal SRAM (4K)
2FFF	

Byte address	ATxmega64D3
0	I/O registers (4K)
FFF	
1000	EEPROM (2K)
17FF	
	RESERVED
2000	Internal SRAM (4K)
2FFF	

Byte address	ATxmega128D3
0	I/O registers (4K)
FFF	
1000	EEPROM (2K)
17FF	
	RESERVED
2000	Internal SRAM (8K)
3FFF	

Byte address	ATxmega192D3
0	I/O registers (4K)
FFF	
1000	EEPROM (2K)
17FF	
	RESERVED
2000	Internal SRAM (16K)
5FFF	

Byte address	ATxmega256D3
0	I/O registers (4K)
FFF	
1000	EEPROM (4K)
1FFF	
2000	Internal SRAM (16K)
5FFF	

Byte address	ATxmega384D3
0	I/O registers (4K)
FFF	
1000	EEPROM (4K)
1FFF	
2000	Internal SRAM (32K)
9FFF	

7.6 EEPROM

All devices have EEPROM for nonvolatile data storage. It is either addressable in a separate data space (default) or memory mapped and accessed in normal data space. The EEPROM supports both byte and page access. Memory mapped EEPROM allows highly efficient EEPROM reading and EEPROM buffer loading. When doing this, EEPROM is accessible using load and store instructions. Memory mapped EEPROM will always start at hexadecimal address 0x1000.

11. System Control and Reset

11.1 Features

- Reset the microcontroller and set it to initial state when a reset source goes active
- Multiple reset sources that cover different situations
  - Power-on reset
  - External reset
  - Watchdog reset
  - Brownout reset
  - PDI reset
  - Software reset
- Asynchronous operation
  - No running system clock in the device is required for reset
- Reset status register for reading the reset source from the application code

11.2 Overview

The reset system issues a microcontroller reset and sets the device to its initial state. This is for situations where operation should not start or continue, such as when the microcontroller operates below its power supply rating. If a reset source goes active, the device enters and is kept in reset until all reset sources have released their reset. The I/O pins are immediately tri-stated. The program counter is set to the reset vector location, and all I/O registers are set to their initial values. The SRAM content is kept. However, if the device accesses the SRAM when a reset occurs, the content of the accessed location can not be guaranteed.

After reset is released from all reset sources, the default oscillator is started and calibrated before the device starts running from the reset vector address. By default, this is the lowest program memory address, 0, but it is possible to move the reset vector to the lowest address in the boot section.

The reset functionality is asynchronous, and so no running system clock is required to reset the device. The software reset feature makes it possible to issue a controlled system reset from the user software.

The reset status register has individual status flags for each reset source. It is cleared at power-on reset, and shows which sources have issued a reset since the last power-on.

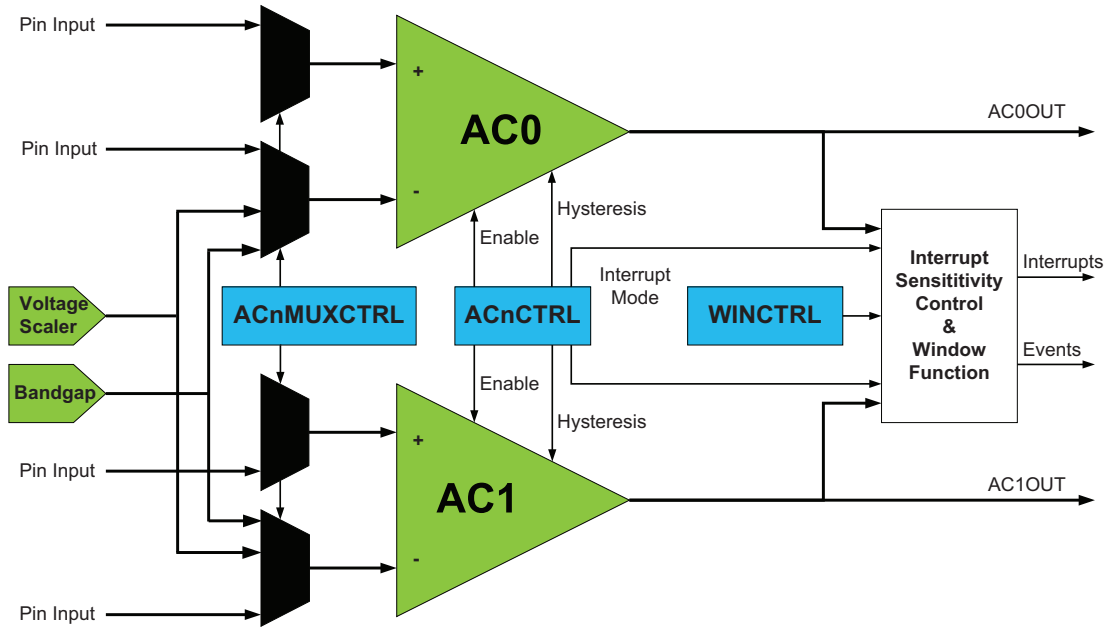
11.3 Reset Sequence

A reset request from any reset source will immediately reset the device and keep it in reset as long as the request is active. When all reset requests are released, the device will go through three stages before the device starts running again:

- Reset counter delay
- Oscillator startup
- Oscillator calibration

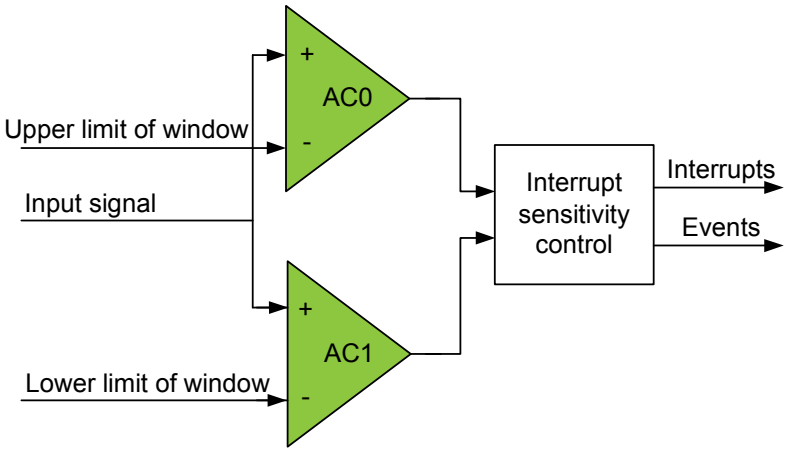
If another reset requests occurs during this process, the reset sequence will start over again.

Figure 26-1. Analog Comparator Overview



The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in Figure 26-2.

Figure 26-2. Analog Comparator Window Function



29. Peripheral Module Address Map

The address maps show the base address for each peripheral and module in Atmel AVR XMEGA D3. For complete register description and summary for each peripheral module, refer to the XMEGA D manual.

Table 29-1. Peripheral Module Address Map

Base address	Name	Description
0x0000	GPIO	General Purpose IO Registers
0x0010	VPORT0	Virtual Port 0
0x0014	VPORT1	Virtual Port 1
0x0018	VPORT2	Virtual Port 2
0x001C	VPORT3	Virtual Port 2
0x0030	CPU	CPU
0x0040	CLK	Clock Control
0x0048	SLEEP	Sleep Controller
0x0050	OSC	Oscillator Control
0x0060	DFLLRC32M	DFLL for the 32MHz Internal Oscillator
0x0068	DFLLRC2M	DFLL for the 2MHz Internal Oscillator
0x0070	PR	Power Reduction
0x0078	RST	Reset Controller
0x0080	WDT	Watchdog Timer
0x0090	MCU	MCU Control
0x00A0	PMIC	Programmable Multilevel Interrupt Controller
0x00B0	PORTCFG	Port Configuration
0x0180	EVSYS	Event System
0x00D0	CRC	CRC Module
0x01C0	NVM	Non Volatile Memory (NVM) Controller
0x0200	ADCA	Analog to Digital Converter on port A
0x0380	ACA	Analog Comparator pair on port A
0x0400	RTC	Real-Time Counter
0x0480	TWIC	Two-Wire Interface on port C
0x04A0	TWIE	Two-Wire Interface on port E
0x0600	PORTA	Port A
0x0620	PORTB	Port B
0x0640	PORTC	Port C

32.2.5 I/O Pin Characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

Table 32-36. I/O Pin Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} (1)/ I_{OL} (2)	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage	V_{CC} = 2.4 - 3.6V		0.7 * V_{CC}		V_{CC} + 0.5	V
		V_{CC} = 1.6 - 2.4V		0.8 * V_{CC}		V_{CC} + 0.5	
V_{IL}	Low level input voltage	V_{CC} = 2.4 - 3.6V		-0.5		0.3 * V_{CC}	
		V_{CC} = 1.6 - 2.4V		-0.5		0.2 * V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.6		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current I/O pin	T = 25°C			<0.01	1	µA
R_P	Pull/buss keeper resistor				25		kΩ

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
   The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
   The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.

Table 32-54. External Clock with Prescaler [1] for System Clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency [2]	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	4.5			
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes:
1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

32.2.13.7 External 16MHz Crystal Oscillator and XOSC Characteristics

Table 32-55. External 16MHz Crystal Oscillator and XOSC Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0		0		ns
			FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1			0		
	Long term jitter	XOSCPWR=0	FRQRANGE=0		0		
			FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1			0		
	Frequency error	XOSCPWR=0	FRQRANGE=0		0.03		%
			FRQRANGE=1		0.03		
			FRQRANGE=2 or 3		0.03		
		XOSCPWR=1			0.003		
	Duty cycle	XOSCPWR=0	FRQRANGE=0		50		
			FRQRANGE=1		50		
			FRQRANGE=2 or 3		50		
		XOSCPWR=1			50		

32.4.5 I/O Pin Characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

Table 32-94. I/O Pin Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} (1)/ I_{OL} (2)	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage	V_{CC} = 2.4 - 3.6V		0.7 * V_{CC}		V_{CC} + 0.5	V
		V_{CC} = 1.6 - 2.4V		0.8 * V_{CC}		V_{CC} + 0.5	
V_{IL}	Low level input voltage	V_{CC} = 2.4 - 3.6V		-0.5		0.3 * V_{CC}	
		V_{CC} = 1.6 - 2.4V		-0.5		0.2 * V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.6		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current I/O pin	T = 25°C			<0.01	1.0	µA
R_P	Pull/buss keeper resistor				25		kΩ

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
   The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
   The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.

32.4.11 Power-on Reset Characteristics

Table 32-103.Power-on Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} (1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.3		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled $V_{POT-} = V_{POT+}$.

32.4.12 Flash and EEPROM Memory Characteristics

Table 32-104.Endurance and Data Retention

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/Erase cycles	25°C	10K			Cycle
			85°C	10K			
			105°C	2K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			
	EEPROM	Write/Erase cycles	25°C	100K			Cycle
			85°C	100K			
			105°C	30K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			

Table 32-105. Programming Time

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
	Chip erase (2)	192KB flash, EEPROM		90		ms
	Application erase	Section erase		6		
	Flash	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		
	EEPROM	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

Figure 33-35. DNL Error vs. Sample Rate

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external

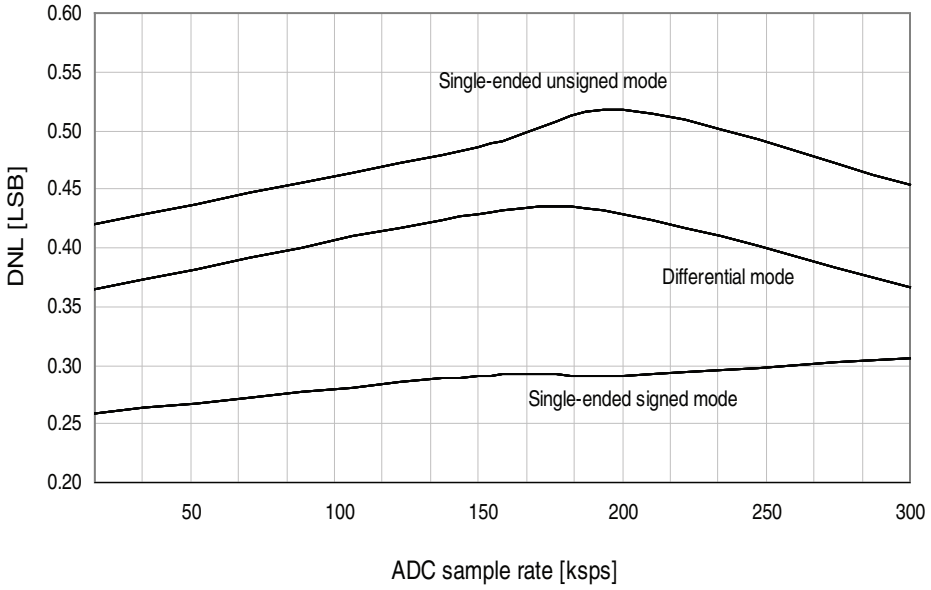


Figure 33-36. DNL Error vs. Input Code

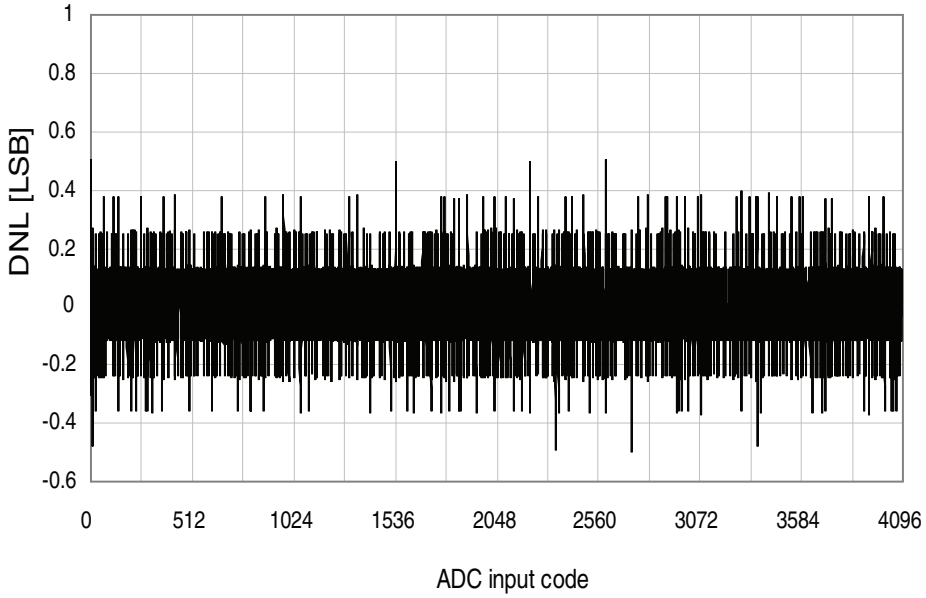


Figure 33-80.Idle Mode Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C

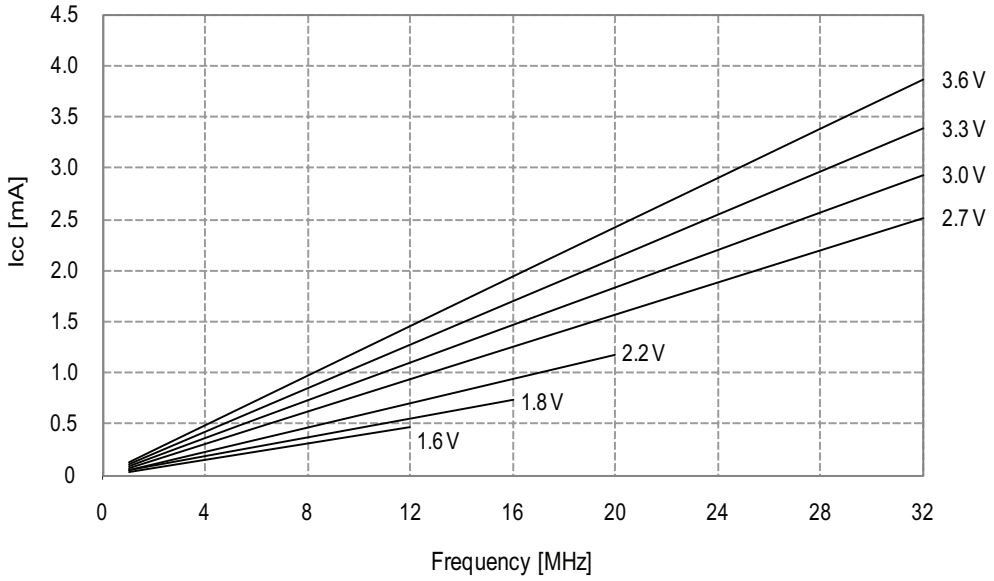
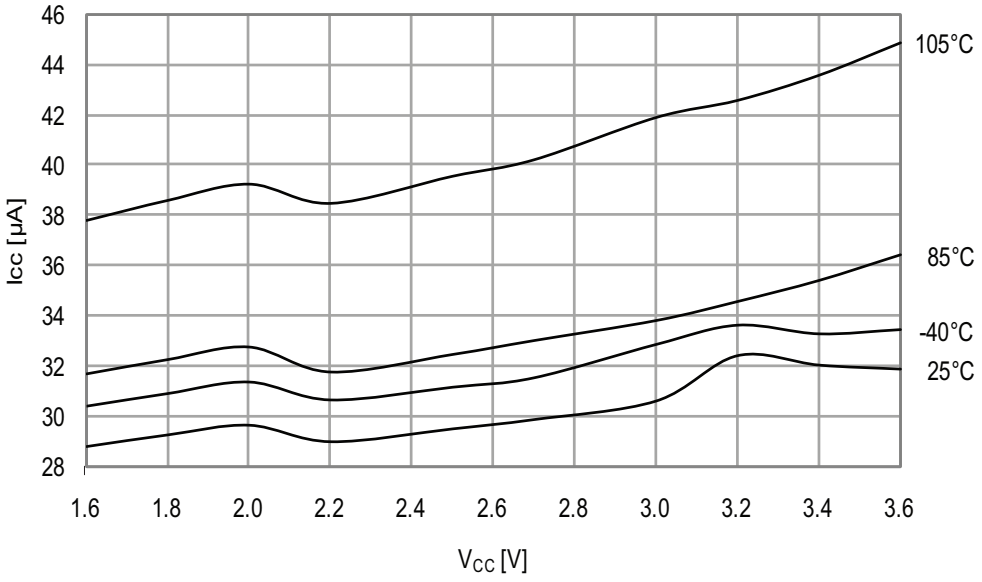


Figure 33-81. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator



33.3.2.3 Thresholds and Hysteresis

Figure 33-169. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IH} I/O pin read as "1"

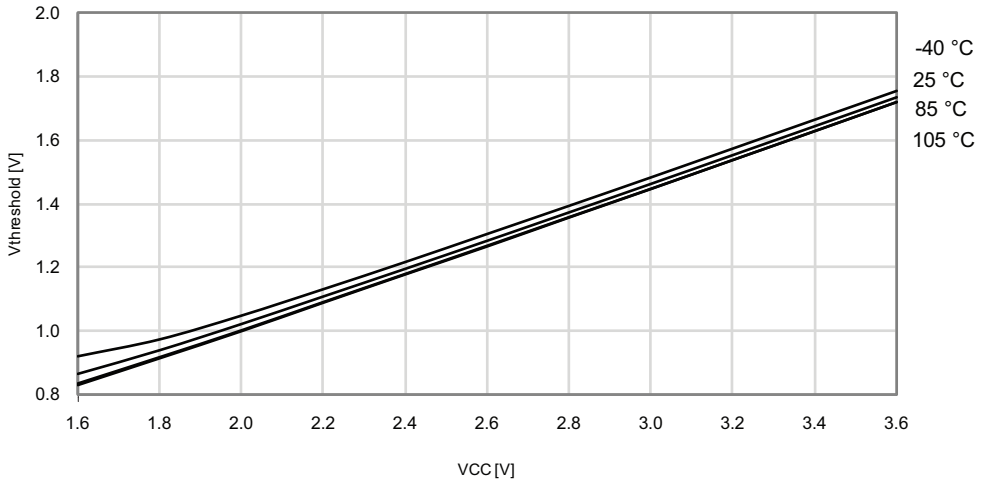


Figure 33-170. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IL} I/O pin read as "0"

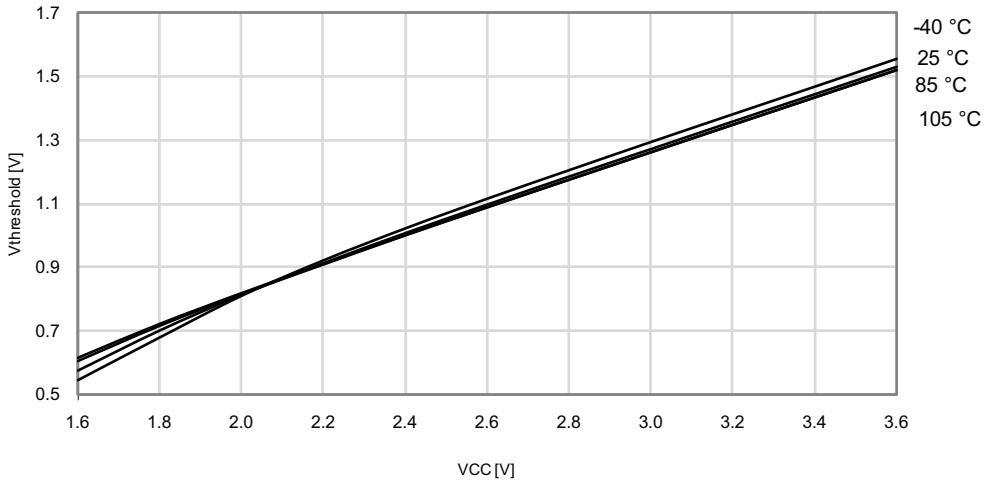
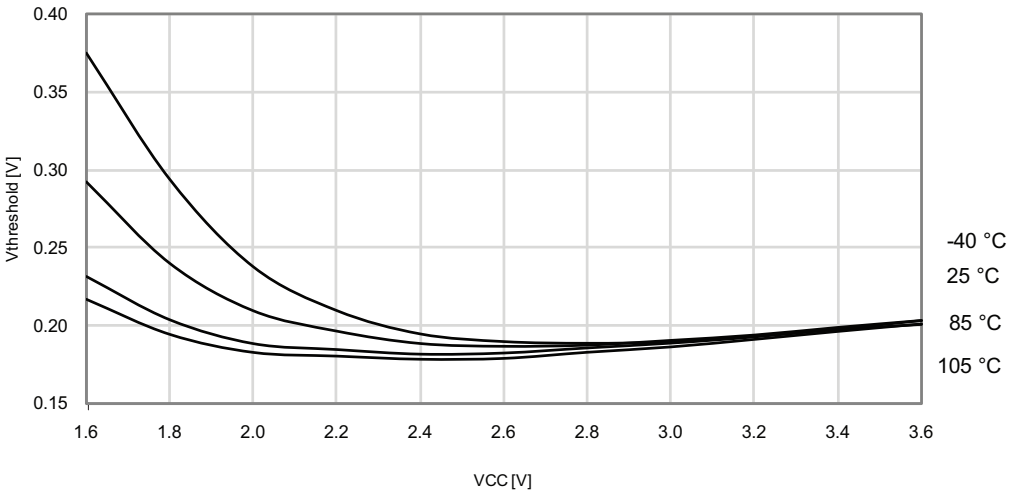


Figure 33-171. I/O Pin Input Hysteresis vs. V_{CC}



33.3.3 ADC Characteristics

Figure 33-172. INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

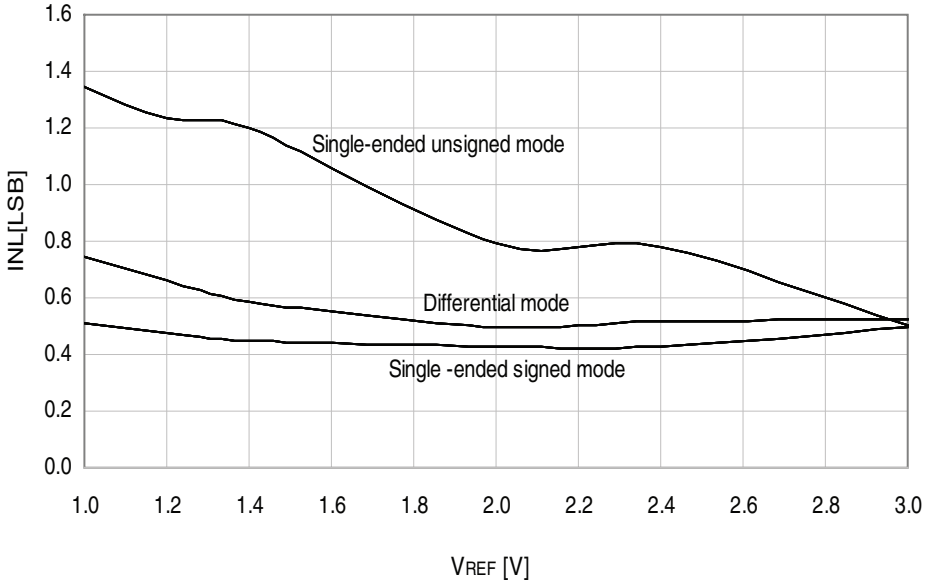


Figure 33-199. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator

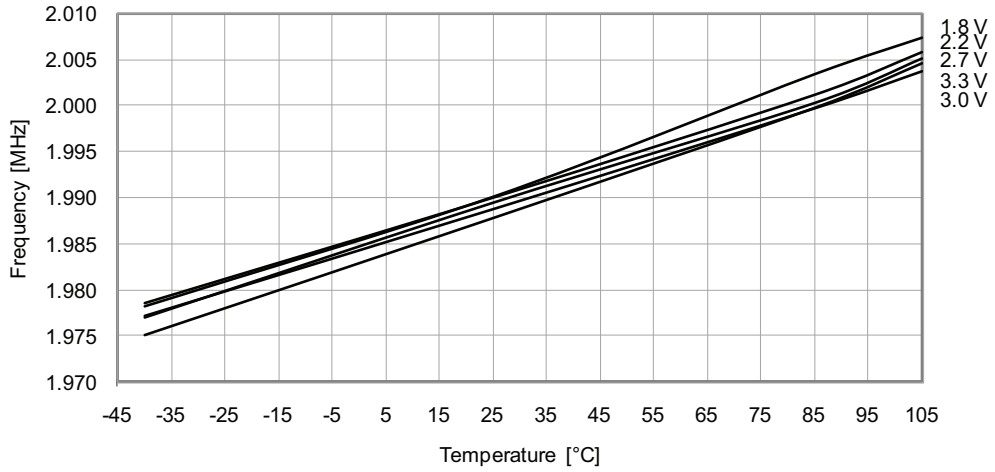


Figure 33-200. 2MHz Internal Oscillator Frequency vs. CALA Calibration Value

V_{CC} = 3V

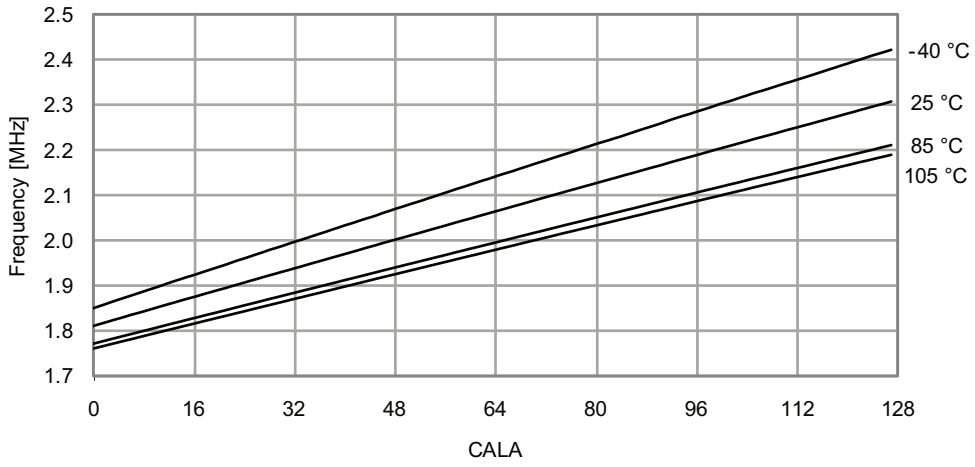


Figure 33-237.I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.0V

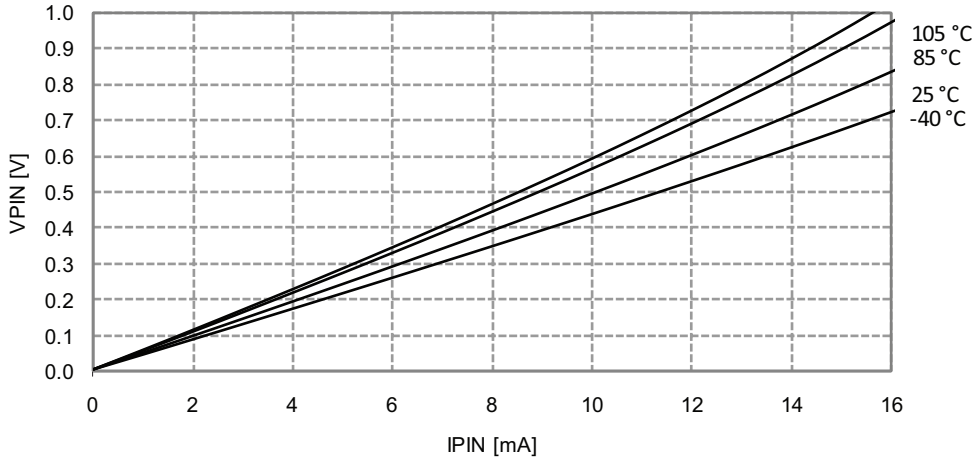


Figure 33-238.I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.3V

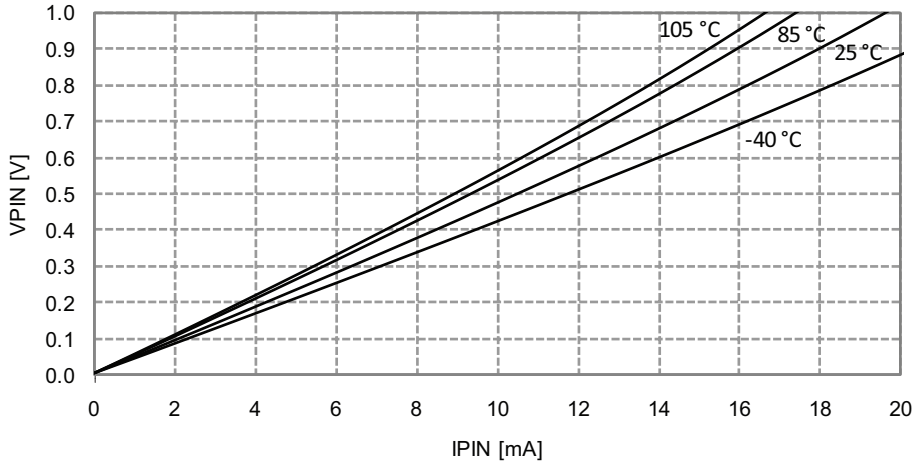


Figure 33-285.Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator

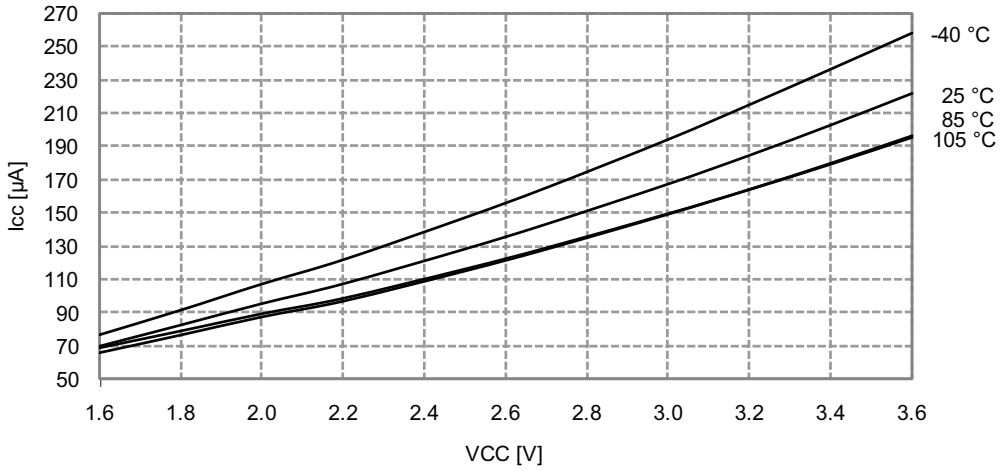


Figure 33-286.Active Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

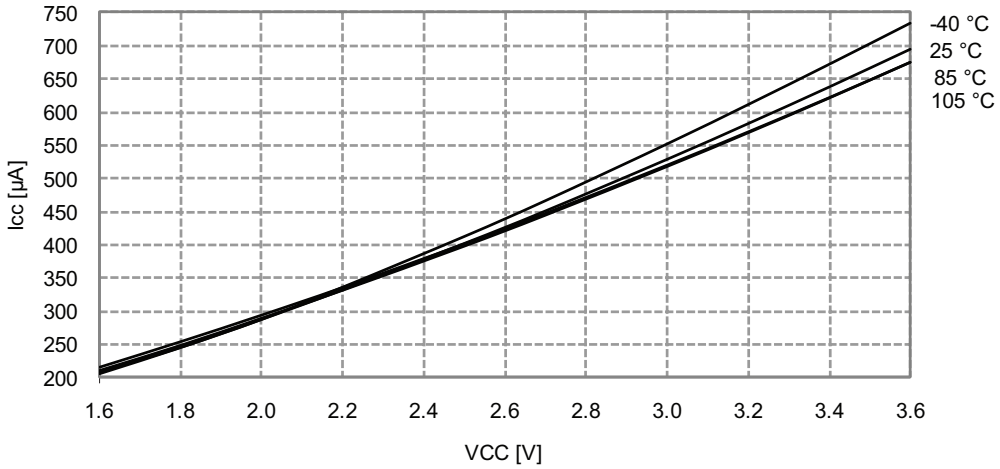
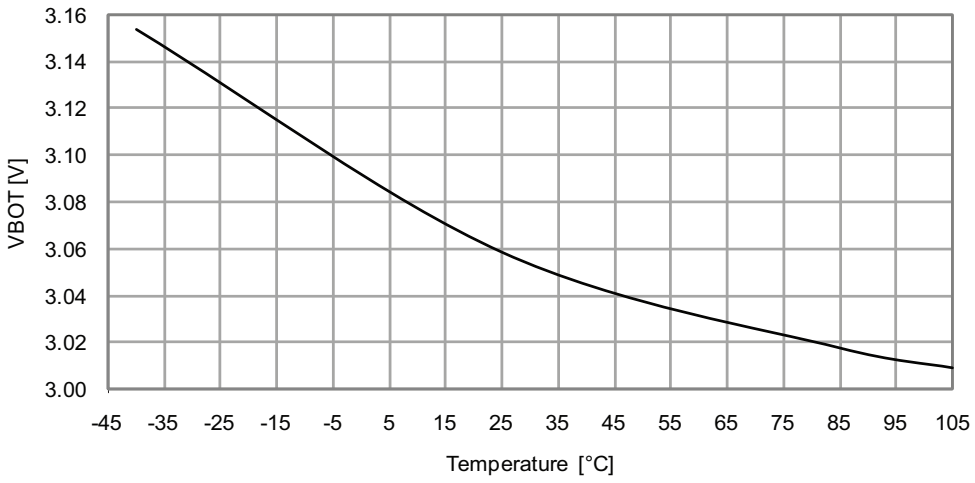


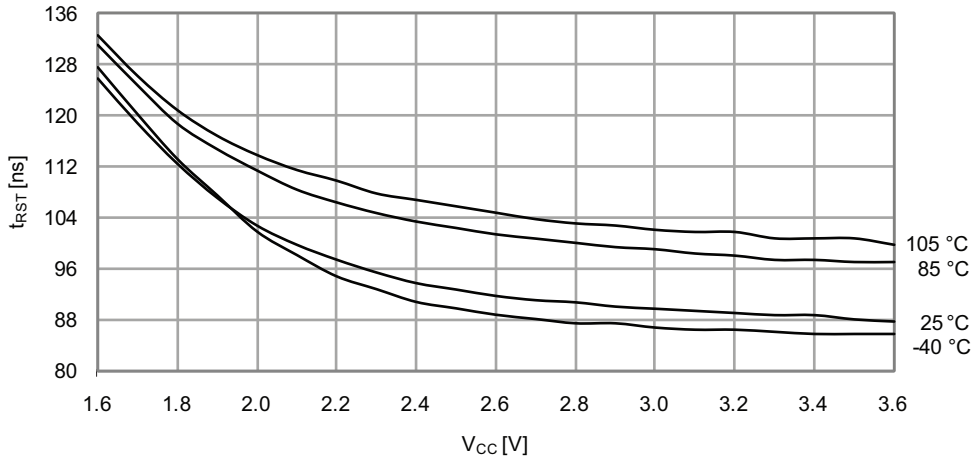
Figure 33-329. BOD Thresholds vs. Temperature

BOD level = 3.0V



33.5.7 External Reset Characteristics

Figure 33-330. Minimum Reset Pin Pulse Width vs. V_{CC}



33.6.2.2 Output Voltage vs. Sink/Source Current

Figure 33-373.I/O Pin Output Voltage vs. Source Current

V_{CC} = *1.8V*

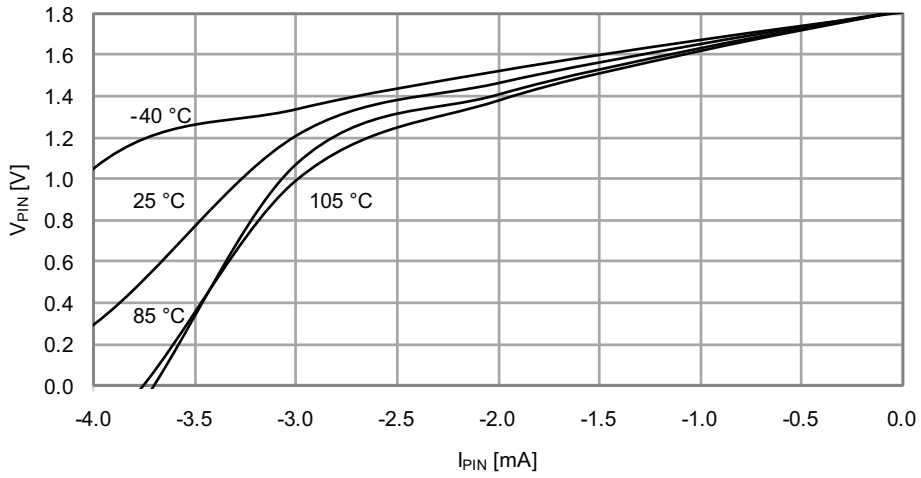
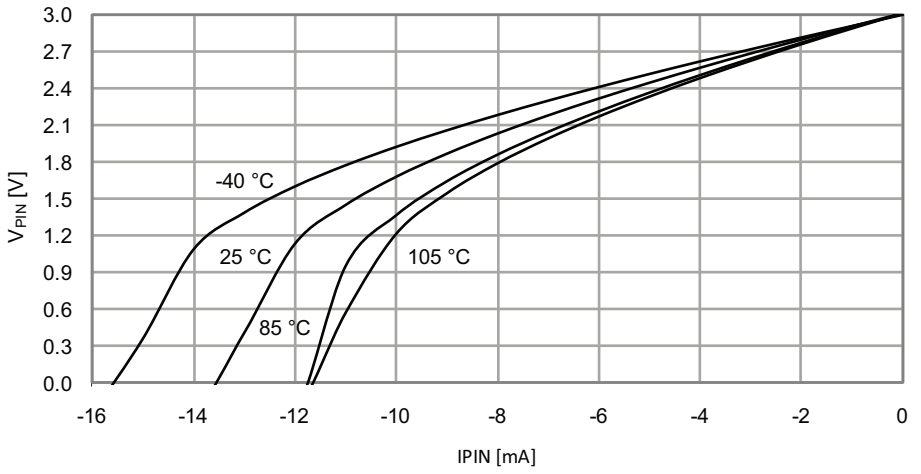


Figure 33-374.I/O Pin Output Voltage vs. Source Current

V_{CC} = *3.0V*



- 1× gain: 2.4 V
- 2× gain: 1.2 V
- 4× gain: 0.6 V
- 8× gain: 300 mV
- 16× gain: 150 mV
- 32× gain: 75 mV
- 64× gain: 38 mV

Problem fix/workaround

Keep the amplified voltage output from the ADC gain stage below 2.4V in order to get a correct result, or keep ADC voltage reference below 2.4V.

6. ADC Event on compare match non-functional

ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

Problem fix/workaround

Enable and use interrupt on compare match when using the compare function.

7. ADC propagation delay is not correct when 8× – 64× gain is used

The propagation delay will increase by only one ADC clock cycle for all gain settings.

Problem fix/workaround

None.

8. Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V

The ADC can not be used to do bandgap measurements when V_{CC} is below 2.7V.

Problem fix/workaround

None.

9. Accuracy lost on first three samples after switching input to ADC gain stage

Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

Problem fix/workaround

Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

10. Configuration of PGM and CWCM not as described in XMEGA D Manual

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

34.3.6 Rev. E

- Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously
- V_{CC} voltage scaler for AC is non-linear
- ADC gain stage cannot be used for single conversion
- ADC has increased INL error for some operating conditions
- ADC gain stage output range is limited to 2.4V
- ADC Event on compare match non-functional
- ADC propagation delay is not correct when 8× – 64× gain is used
- Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V
- Accuracy lost on first three samples after switching input to ADC gain stage
- Configuration of PGM and CWCM not as described in the XMEGA D Manual
- PWM is not restarted properly after a fault in cycle-by-cycle mode
- BOD will be enabled at any reset
- EEPROM page buffer always written when NVM DATA0 is written
- Pending full asynchronous pin change interrupts will not wake the device
- Pin configuration does not affect Analog Comparator Output
- NMI Flag for Crystal Oscillator Failure automatically cleared
- RTC Counter value not correctly read after sleep
- Pending asynchronous RTC-interrupts will not wake up device
- TWI Transmit collision flag not cleared on repeated start
- Clearing TWI Stop Interrupt Flag may lock the bus
- TWI START condition at bus timeout will cause transaction to be dropped
- TWI Data Interrupt Flag (DIF) erroneously read as set
- WDR instruction inside closed window will not issue reset
- Non available functions and options
- Sampled BOD in Active mode will cause noise when bandgap is used as reference
- Temperature sensor not calibrated
- Disabling the USART transmitter does not automatically set the TxD pin direction to input.

1. Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously

If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1µs and could potentially give a wrong comparison result.

Problem fix/workaround

If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. VCC voltage scaler for AC is non-linear

The 6-bit V_{CC} voltage scaler in the Analog Comparators is non-linear.

16. NMI Flag for Crystal Oscillator Failure automatically cleared

NMI flag for Crystal Oscillator Failure (XOSCFDIF) will be automatically cleared when executing the NMI interrupt handler.

Problem fix/workaround

This device revision has only one NMI interrupt source, so checking the interrupt source in software is not required.

17. Writing EEPROM or Flash while reading any of them will not work

The EEPROM and Flash cannot be written while reading EEPROM or Flash, or while executing code in Active mode.

Problem fix/workaround

Enter IDLE sleep mode within 2.5µs (five 2MHz clock cycles and 80 32MHz clock cycles) after starting an EEPROM or flash write operation. Wake-up source must either be EEPROM ready or NVM ready interrupt. Alternatively set up a Timer/Counter to give an overflow interrupt 7ms after the erase or write operation has started, or 13ms after atomic erase-and-write operation has started, and then enter IDLE sleep mode.

18. RTC Counter value not correctly read after sleep

If the RTC is set to wake up the device on RTC Overflow and bit 0 of RTC CNT is identical to bit 0 of RTC PER as the device is entering sleep, the value in the RTC count register can not be read correctly within the first prescaled RTC clock cycle after wake-up. The value read will be the same as the value in the register when entering sleep.

The same applies if RTC Compare Match is used as wake-up source.

Problem fix/workaround

Wait at least one prescaled RTC clock cycle before reading the RTC CNT value.

19. Pending asynchronous RTC-interrupts will not wake up device

Asynchronous Interrupts from the Real-Time-Counter that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again.

Problem fix/workaround

None.

20. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/workaround

Clear the flag in software after address interrupt.

21. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.