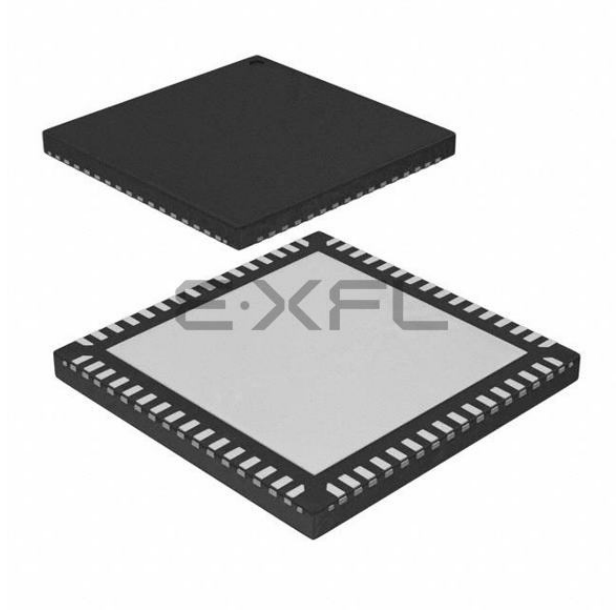

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	192KB (96K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega192d3-mhr

Table 28-1. Port A - Alternate Functions

PORT A	PIN #	INTERRUPT	ADCA POS/ GAINPOS	ADCA NEG	ADCA GAINNEG	ACA POS	ACA NEG	ACA OUT	REFA
GND	60								
AVCC	61								
PA0	62	SYNC	ADC0	ADC0		AC0	AC0		AREFA
PA1	63	SYNC	ADC1	ADC1		AC1	AC1		
PA2	64	SYNC/ASYNC	ADC2	ADC2		AC2			
PA3	1	SYNC	ADC3	ADC3		AC3	AC3		
PA4	2	SYNC	ADC4		ADC4	AC4			
PA5	3	SYNC	ADC5		ADC5	AC5	AC5		
PA6	4	SYNC	ADC6		ADC6	AC6		AC1OUT	
PA7	5	SYNC	ADC7		ADC7		AC7	AC0OUT	

Table 28-2. Port B - Alternate Functions

PORT B	PIN #	INTERRUPT	ADCA POS	REFB
PB0	6	SYNC	ADC8	AREFB
PB1	7	SYNC	ADC91	
PB2	8	SYNC/ASYNC	ADC10	
PB3	9	SYNC	ADC11	
PB4	10	SYNC	ADC12	
PB5	11	SYNC	ADC13	
PB6	12	SYNC	ADC14	
PB7	13	SYNC	ADC15	
GND	14			
VCC	15			

Table 28-3. Port C - Alternate Functions

PORT C	PIN #	INTERRUPT	TCC0 (1)(2)	AWEXC	TCC1	USARTC0 (3)	SPIC (4)	TWIC	CLOCKOUT (5)	EVENTOUT (6)
PC0	16	SYNC	OC0A	$\overline{\text{OC0ALS}}$				SDA		
PC1	17	SYNC	OC0B	OC0AHS		XCK0		SCL		
PC2	18	SYNC/ASYNC	OC0C	$\overline{\text{OC0BLS}}$		RXD0				
PC3	19	SYNC	OC0D	OC0BHS		TXD0				
PC4	20	SYNC		$\overline{\text{OC0CLS}}$	OC1A		$\overline{\text{SS}}$			
PC5	21	SYNC		OC0CHS	OC1B		MOSI			

Table 32-29. Two-wire Interface Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7V_{CC}$		V_{CC} + 0.5	V
V_{IL}	Input low voltage		-0.5		$0.3V_{CC}$	
V_{hys}	Hysteresis of Schmitt trigger inputs		$0.05V_{CC}$ (1)			
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		$20 + 0.1C_b$ (1)(2)		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ (2)	$20 + 0.1C_b$ (1)(2)		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER} (3) > max(10f_{SCL}, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold time (repeated) START condition	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{LOW}	Low period of SCL clock	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			
t_{HIGH}	High period of SCL clock	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	0.6			
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq 100kHz$	0		3.45	
		$f_{SCL} > 100kHz$	0		0.9	
$t_{SU;DAT}$	Data setup time	$f_{SCL} \leq 100kHz$	250			
		$f_{SCL} > 100kHz$	100			
$t_{SU;STO}$	Setup time for STOP condition	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
t_{BUF}	Bus free time between a STOP and START condition	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			

Notes:
1. Required only for $f_{SCL} > 100kHz$.
2. C_b = Capacitance of one bus line in pF.
3. f_{PER} = Peripheral clock frequency.

Table 32-69. Gain Stage Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode		4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode		4.4		pF
	Signal range	Gain stage output	0		AV_{CC} - 0.6	V
	Propagation delay	ADC conversion rate	1/2	1	3	Clk_{ADC} cycles
	Clock frequency	Same as ADC	100		1800	kHz
	Gain error	0.5x gain, normal mode		-1		%
		1x gain, normal mode		-1		
		8x gain, normal mode		-1		
		64x gain, normal mode		5		
	Offset error, input referred	0.5x gain, normal mode		10		mV
		1x gain, normal mode		5		
		8x gain, normal mode		-20		
		64x gain, normal mode		-126		

32.3.7 Analog Comparator Characteristics

Table 32-70. Analog Comparator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage			10		mV
I_{lk}	Input leakage current			<10	50	nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			50		µs
V_{hys1}	Hysteresis, none	V_{CC} = 1.6V - 3.6V		0		mV
V_{hys2}	Hysteresis, small	V_{CC} = 1.6V - 3.6V		15		
V_{hys3}	Hysteresis, large	V_{CC} = 1.6V - 3.6V		30		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T = 85°C		20	90	ns
		V_{CC} = 3.0V		17		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb
	Current source accuracy after calibration			5		%
	Current source calibration range	Single mode	4		6	µA

32.4.3 Current Consumption

Table 32-91. Current Consumption for Active Mode and Sleep Modes

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		60		µA
			V_{CC} = 3.0V		140		
		1MHz, Ext. Clk	V_{CC} = 1.8V		245		
			V_{CC} = 3.0V		550		
		2MHz, Ext. Clk	V_{CC} = 1.8V		440	700	
			V_{CC} = 3.0V		0.9	1.5	mA
		32MHz, Ext. Clk			9.0	15	
	Idle power consumption (2)	32kHz, Ext. Clk	V_{CC} = 1.8V		3.0		µA
			V_{CC} = 3.0V		3.5		
		1MHz, Ext. Clk	V_{CC} = 1.8V		55		
			V_{CC} = 3.0V		110		
		2MHz, Ext. Clk	V_{CC} = 1.8V		105	350	
			V_{CC} = 3.0V		215	650	
		32MHz, Ext. Clk			3.4	8.0	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			3.5	6.0	
		T = 105°C			10	15	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.5	2.0	
		WDT and sampled BOD enabled, T = 85°C			5.8	10	
		WDT and sampled BOD enabled, T= 105°C			12	20	
	Power-save power consumption (3)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.3		
			V_{CC} = 3.0V		1.4		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.7	2.0	
			V_{CC} = 3.0V		0.8	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.9	3.0	
			V_{CC} = 3.0V		1.1	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		170		

Notes:
1. All power reduction registers set including FPRM and EPRM.
2. All power reduction registers set without FPRM and EPRM.
3. Maximum limits are based on characterization, and not tested in production.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C_{XTAL1}	Parasitic capacitance XTAL1 pin			5.9		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin			8.3		
C_{LOAD}	Parasitic capacitance load			3.5		

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

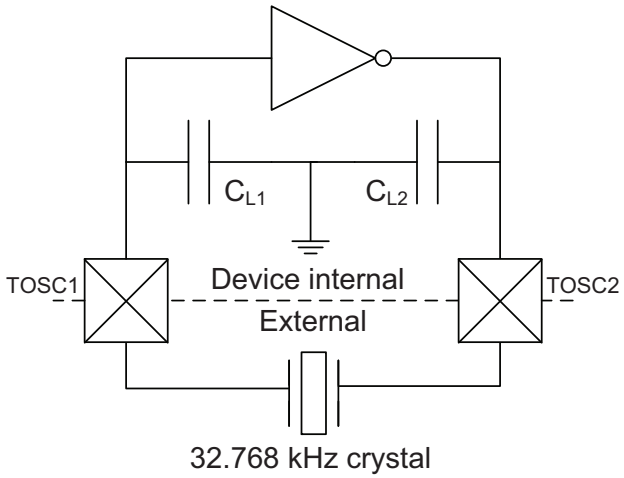
32.6.13.8 External 32.768kHz Crystal Oscillator and TOSC Characteristics

Table 32-172. External 32.768kHz Crystal Oscillator and TOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
		Crystal load capacitance 12pF			28	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			3.5		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			3.5		
	Recommended safety factor	Capacitance load matched to crystal specification	3			

Note: See Figure 32-39 on page 173 for definition.

Figure 32-39. TOSC Input Capacitance



The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

Figure 33-37. Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

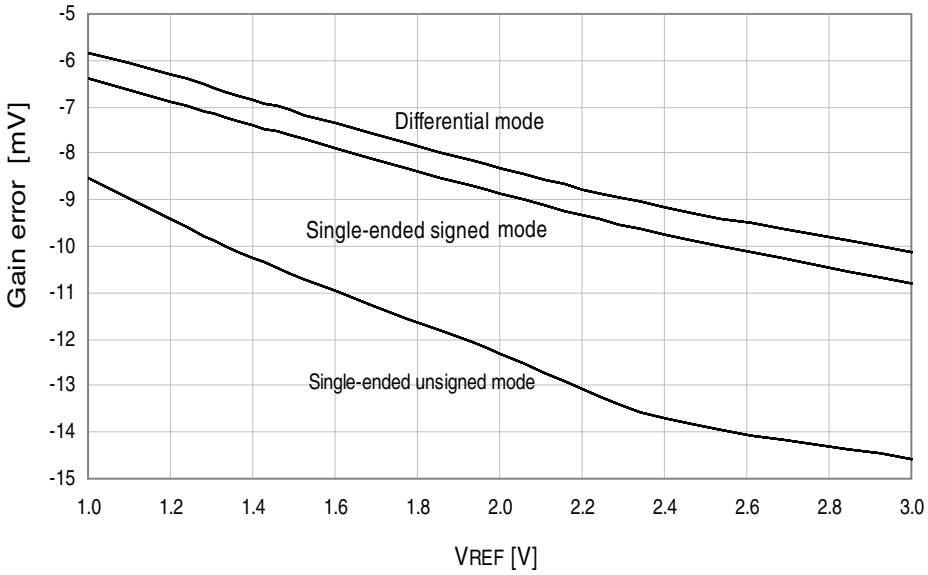
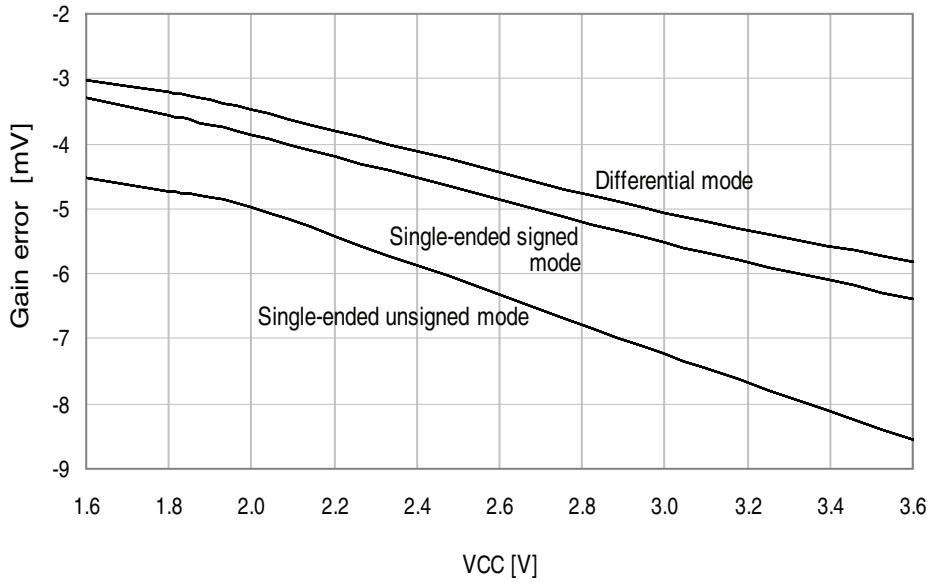


Figure 33-38. Gain Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps



33.1.7 External Reset Characteristics

Figure 33-49. Minimum Reset Pin Pulse Width vs. V_{CC}

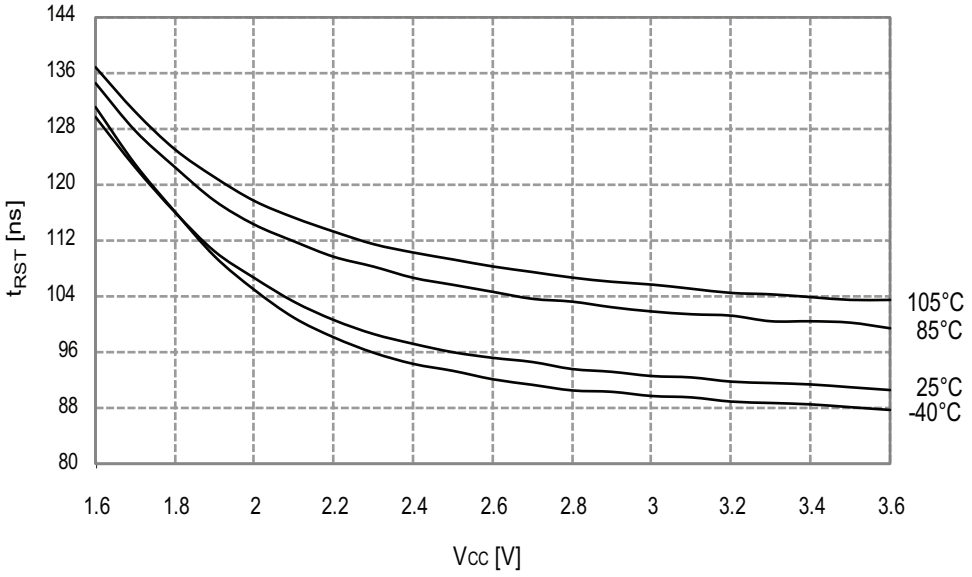
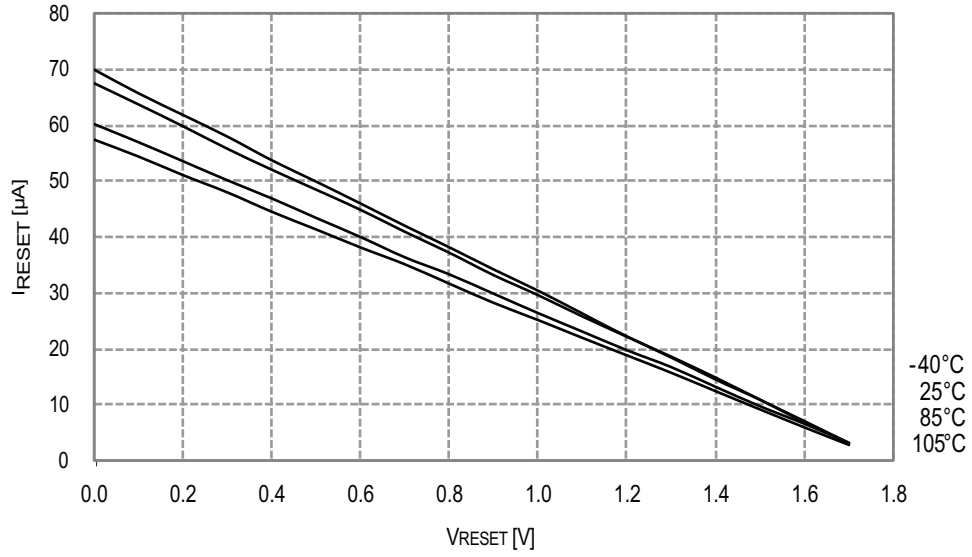


Figure 33-50. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 1.8V



33.1.8.3 2MHz Internal Oscillator

Figure 33-57. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled

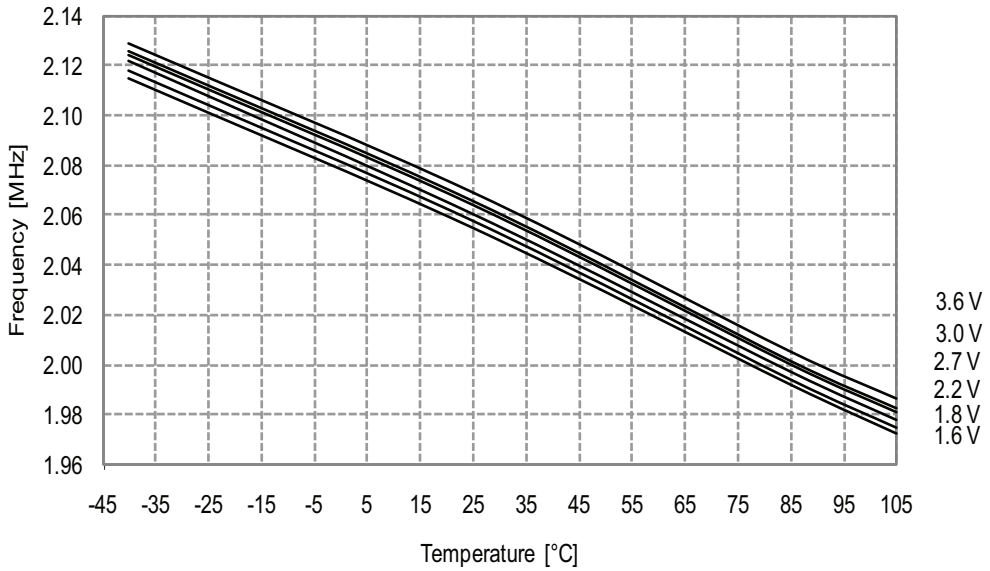


Figure 33-58. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator

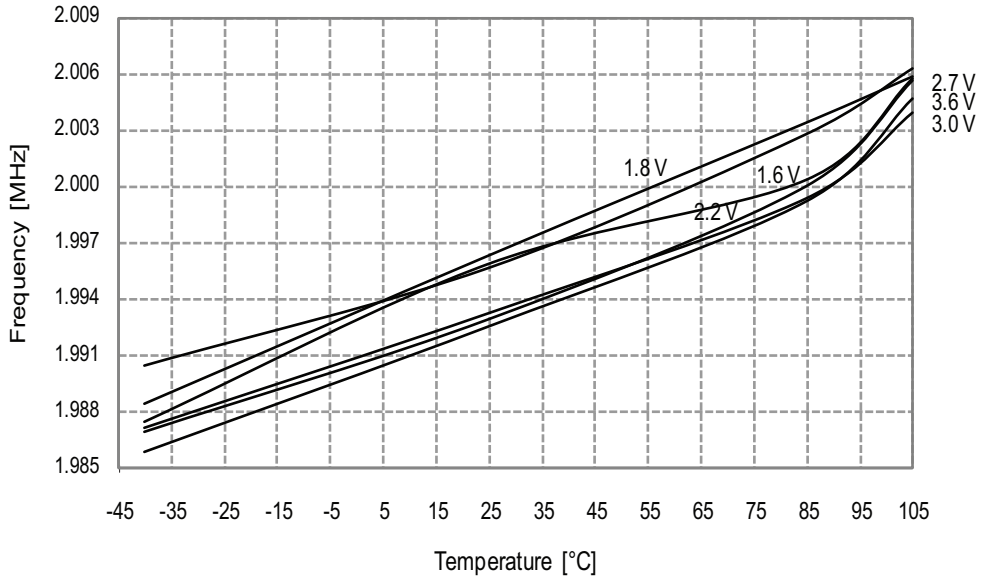


Figure 33-100. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IL} I/O pin read as "0"

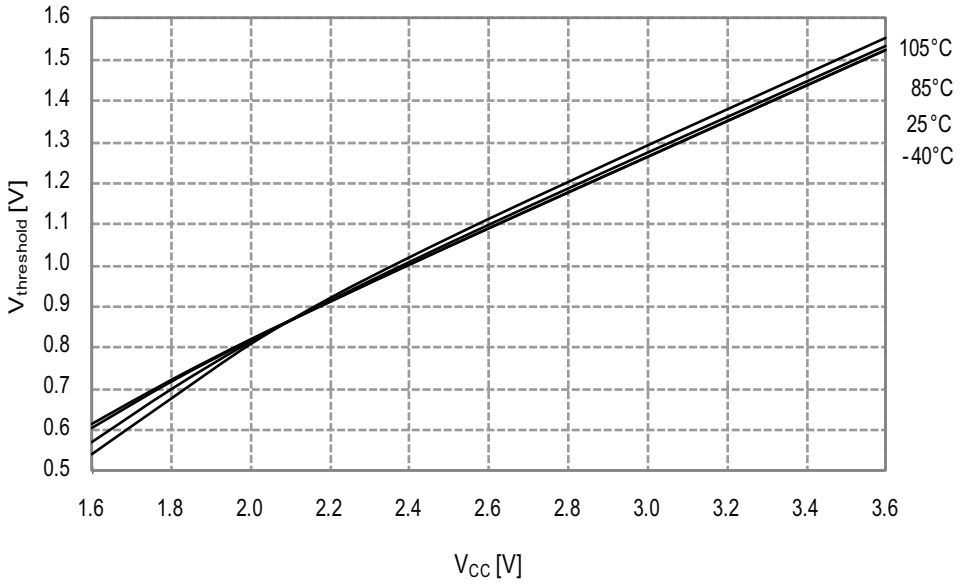


Figure 33-101. I/O Pin Input Hysteresis vs. V_{CC}

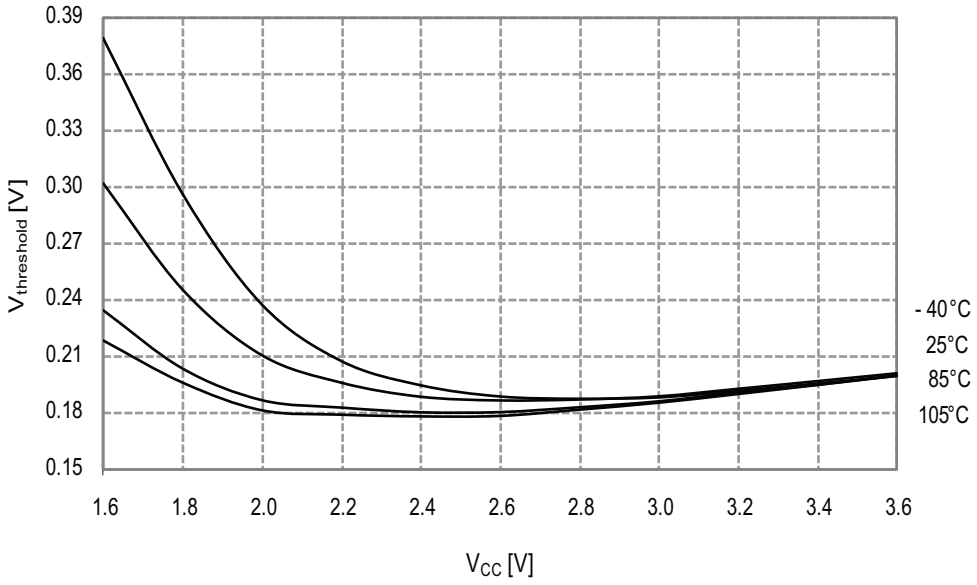


Figure 33-110. Offset Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

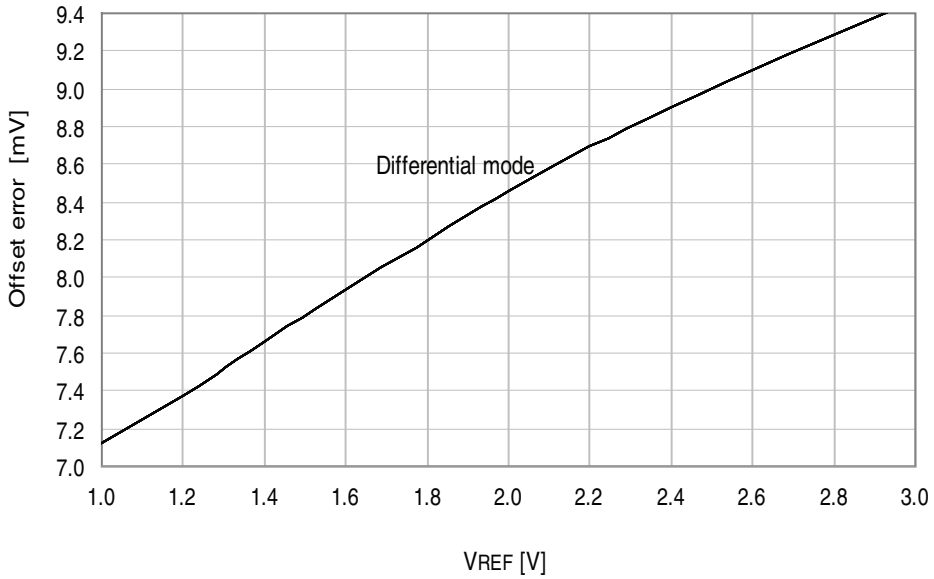


Figure 33-111. Gain Error vs. Temperature

V_{CC} = 3.0V, V_{REF} = external 2.0V

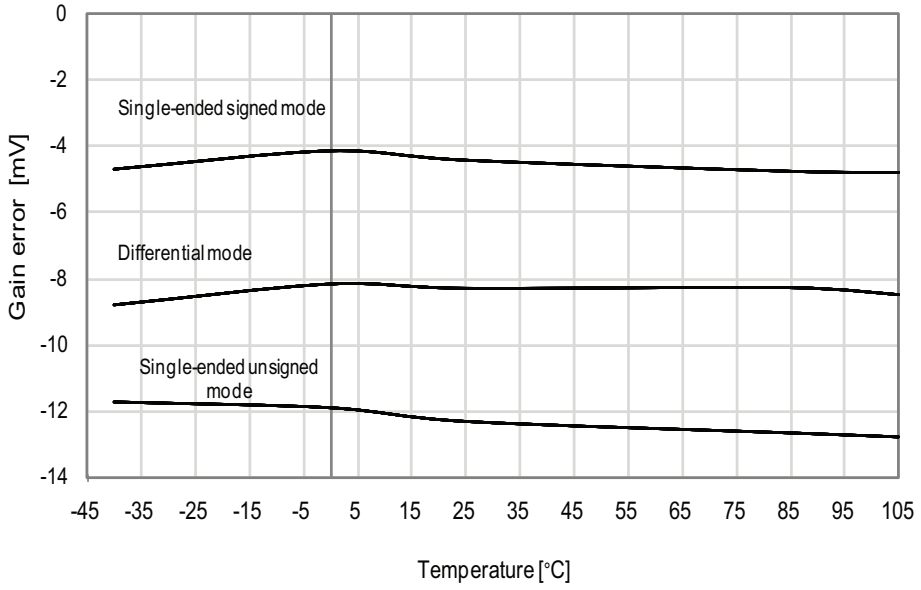
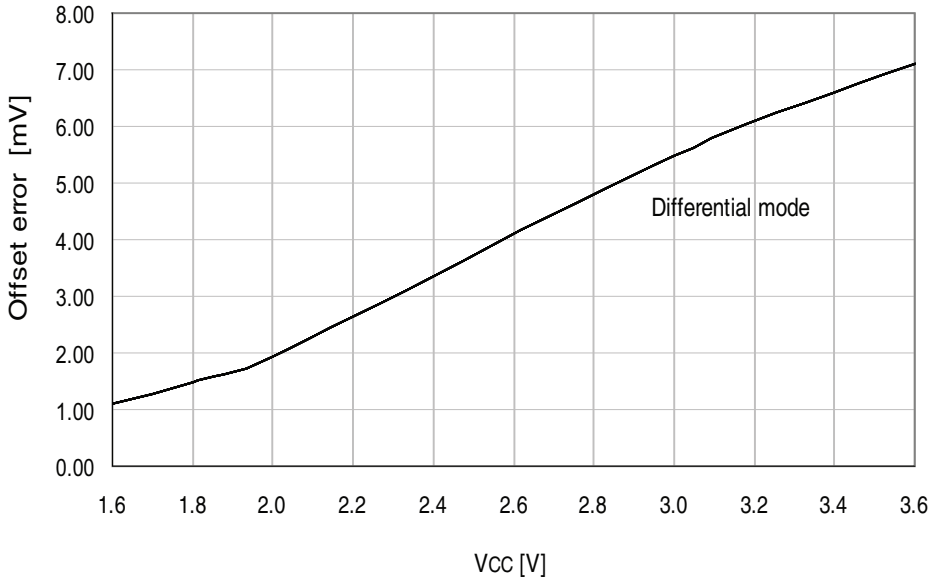


Figure 33-112. Offset Error vs. V_{CC}

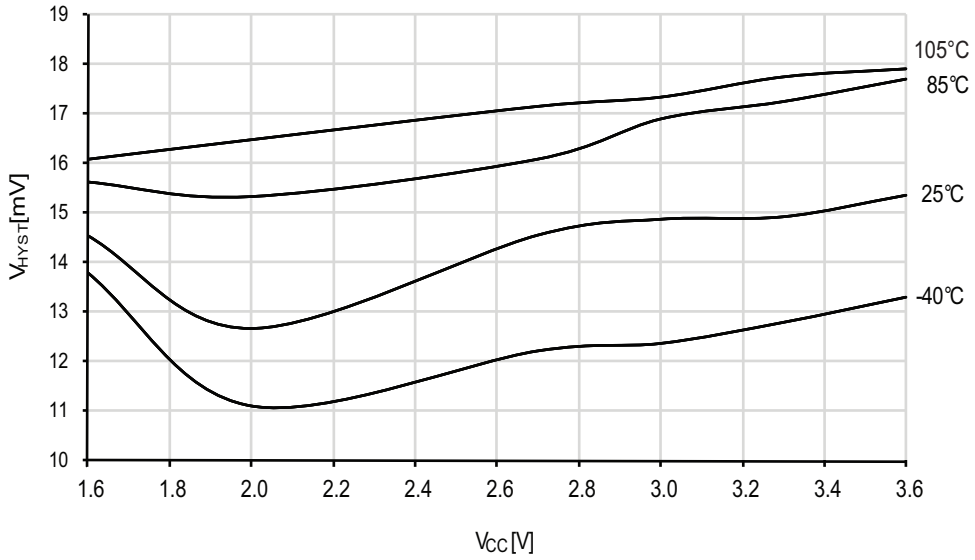
T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps



33.2.4 Analog Comparator Characteristics

Figure 33-113. Analog Comparator Hysteresis vs. V_{CC}

Small hysteresis



33.2.9 Two-Wire Interface Characteristics

Figure 33-140. SDA Hold Time vs. Temperature

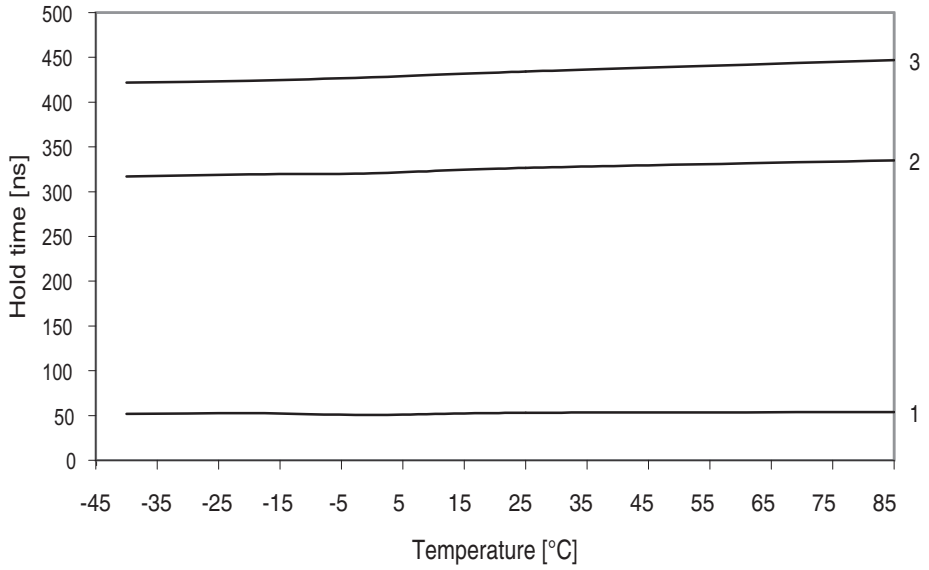


Figure 33-141. SDA Hold Time vs. Supply Voltage

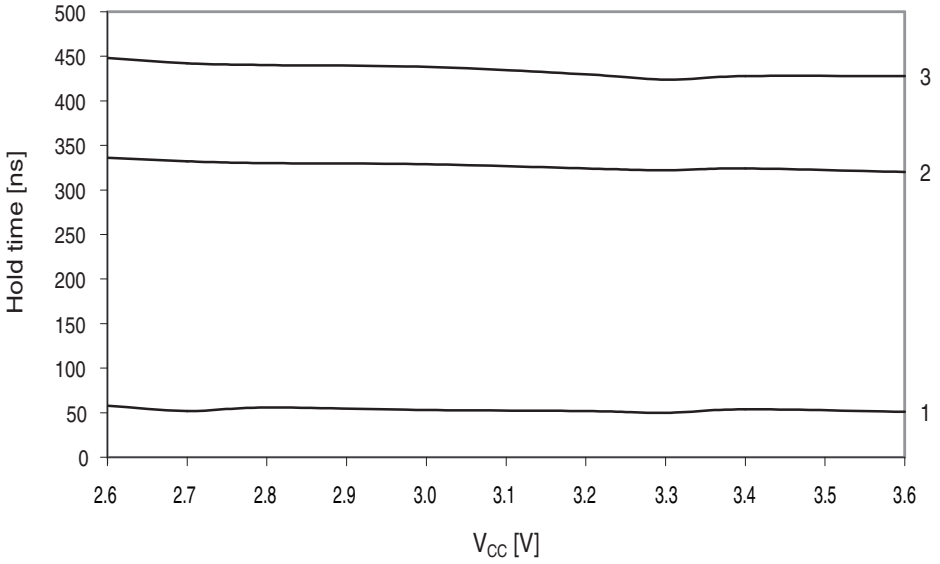
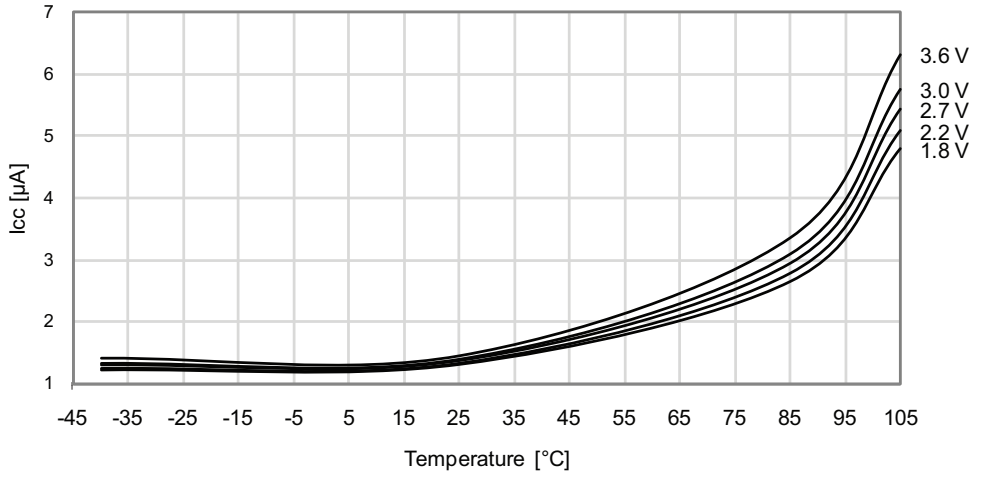


Figure 33-159. Power-down Mode Supply Current vs. Temperature

Watchdog and sampled BOD enabled and running from internal ULP oscillator



33.3.2 I/O Pin Characteristics

33.3.2.1 Pull-up

Figure 33-160. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = 1.8V

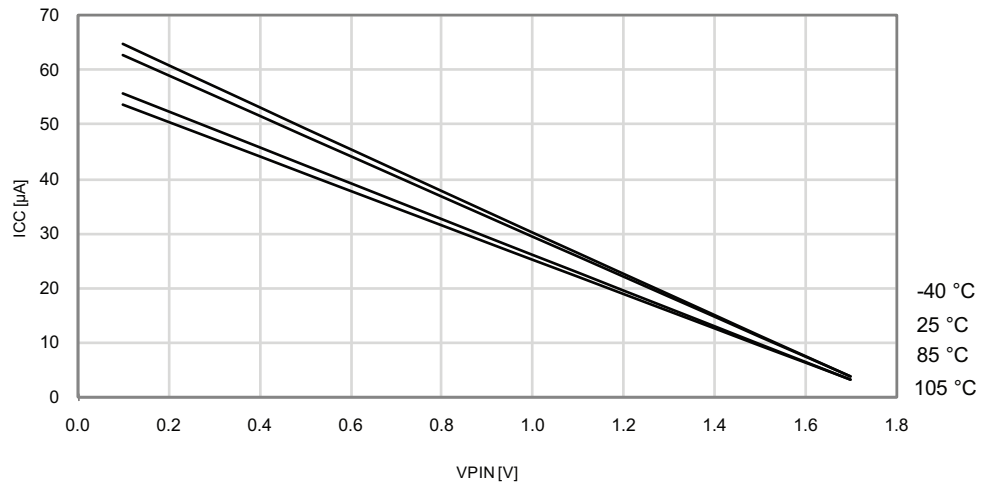
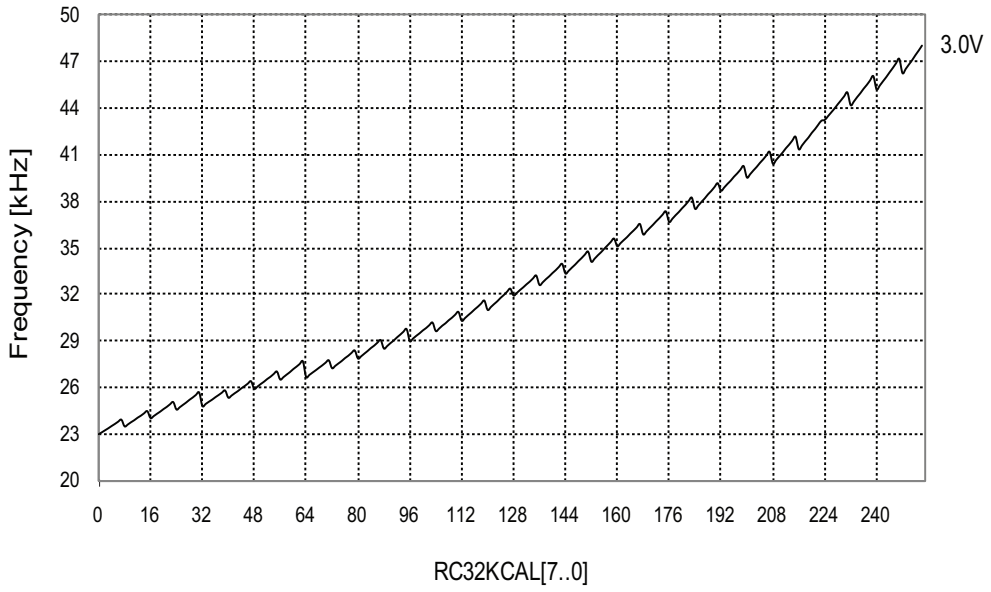


Figure 33-197. 32.768kHz Internal Oscillator Frequency vs. Calibration Value

V_{CC} = 3.0V, T = 25°C



33.3.8.3 2MHz Internal Oscillator

Figure 33-198. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled

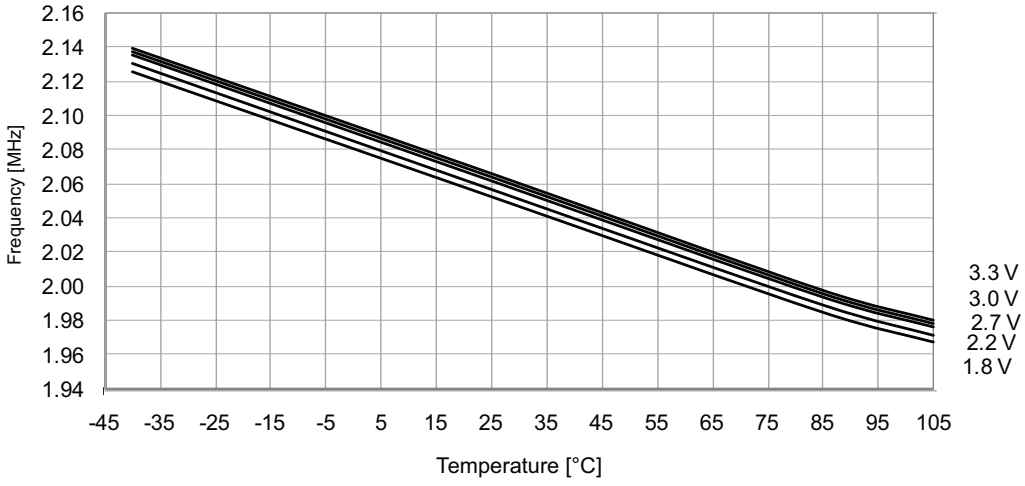


Figure 33-199. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator

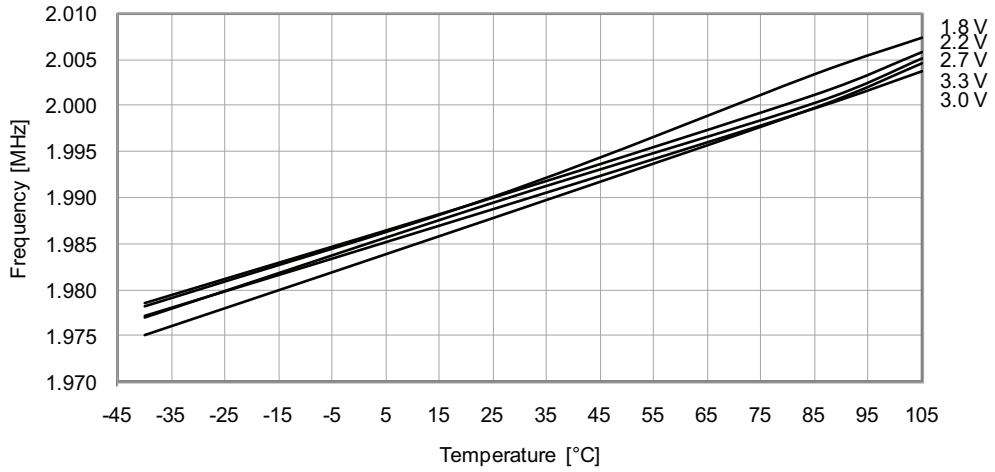
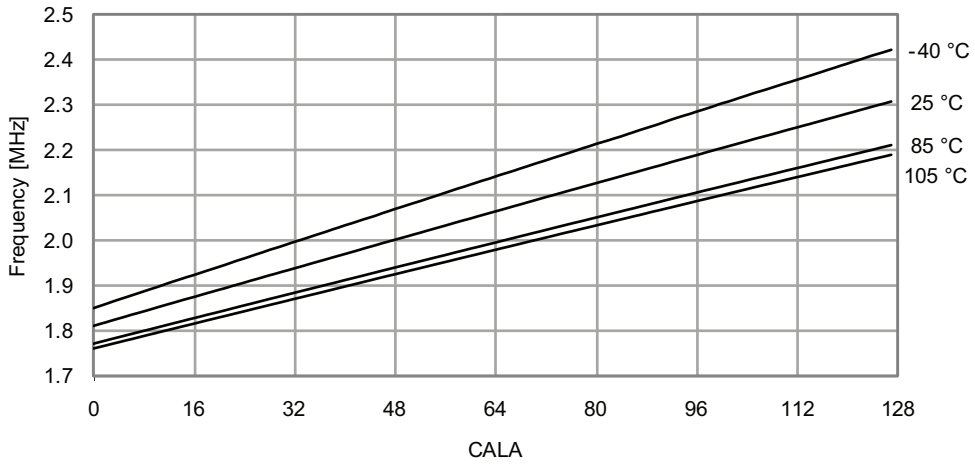


Figure 33-200. 2MHz Internal Oscillator Frequency vs. CALA Calibration Value

V_{CC} = 3V



33.3.8.4 32MHz Internal Oscillator

Figure 33-201. 32MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled

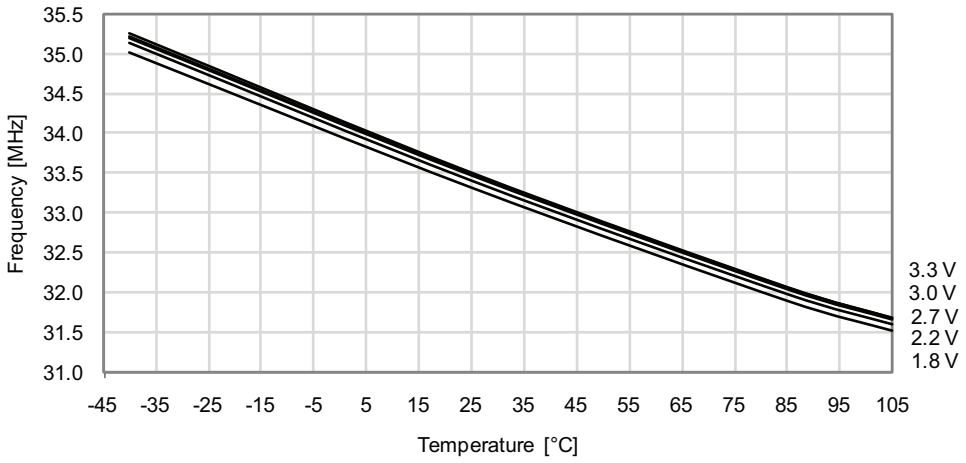
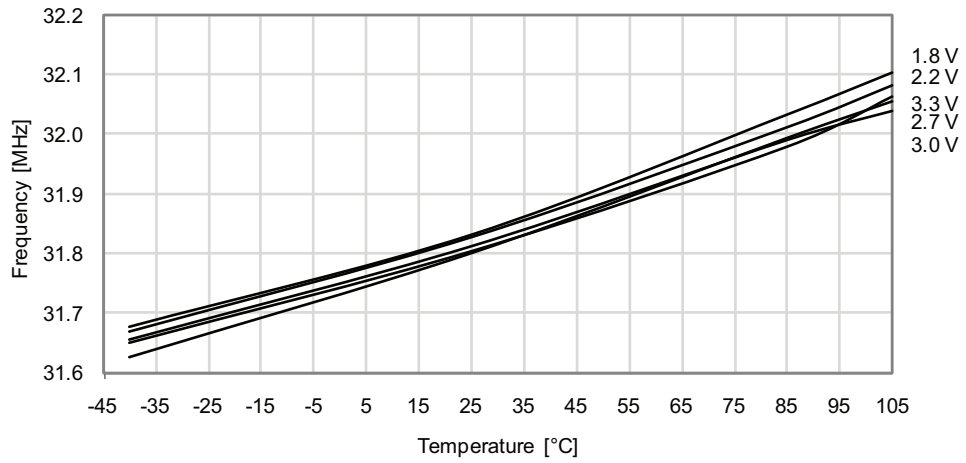


Figure 33-202. 32MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator



Problem fix/workaround

Table 34-1. Configure PWM and CWCM According to this Table:

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

11. PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

Problem fix/workaround

Do a write to any AWeX I/O register to re-enable the output.

12. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the V_{CC} voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until V_{CC} is above the programmed BOD level even if the BOD is disabled.

Problem fix/workaround

Do not set the BOD level higher than V_{CC} even if the BOD is not used.

13. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

14. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/workaround

None.

15. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

Problem fix/workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (that is, connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

Problem fix/workaround

Table 34-6. Configure PWM and CWCM According to this Table:

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

11. PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

Problem fix/workaround

Do a write to any AWeX I/O register to re-enable the output.

12. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the V_{CC} voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until V_{CC} is above the programmed BOD level even if the BOD is disabled.

Problem fix/workaround

Do not set the BOD level higher than V_{CC} even if the BOD is not used.

13. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

14. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/workaround

None.

15. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

Problem fix/workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (that is, connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

- PORT remap functions with alternate pin locations for Timer/Counter output compare channels, USART0 and SPI, and the PORT REMAP register
- PORT RTC clock output option and the RTCOUT bit in the PORT CLKEVOUT register
- PORT remap functions with alternate pin locations for the clock and event output, and the CLKEVPIN bit in the PORT CLKEVOUT register
- TOSC alternate pin locations, and TOSCSEL bit in FUSEBYTE2
- Real Time Counter clock source options of external clock from TOSC1, and 32.768kHz from TOSC, and 32.768kHz from the 32.768kHz internal oscillator, and these configuration options in the RTCSRC bits in the Clock RTCTRL register
- PLL divide by two option, and the PLLDIV bit in the Clock PLLCTRL register
- PLL lock detection failure function and the PLLDIF and PLLFDEN bits in the Clock XOSCFAIL register
- The high drive option for external crystal and the XOSCPWR bit on the Oscillator XOSCCTRL register
- The option to enable sequential startup of the analog modules and the ANAINIT register in MCU Control memory

Problem fix/workaround

None.

25. Sampled BOD in Active mode will cause noise when bandgap is used as reference

Using the BOD in sampled mode when the device is running in Active or Idle mode will add noise on the bandgap reference for ADC, DAC and Analog Comparator.

Problem fix/workaround

If the bandgap is used as reference for either the ADC, DAC and Analog Comparator, the BOD must not be set in sampled mode.

26. Temperature sensor not calibrated

Temperature sensor factory calibration not implemented.

Problem fix/workaround

None.

27. Disabling of USART transmitter does not automatically set the TxD pin direction to input

If the USART transmitter is idle with no frames to transmit, setting TXEN to zero will not automatically set the TxD pin direction to input.

Problem fix/workaround

The TxD pin direction can be set to input using the Port DIR register. Be advised that setting the Port DIR register to input will be immediate. Ongoing transmissions will be truncated.

34.5.6 Rev. D

Not sampled.

34.5.7 Rev. C

Not sampled.

Problem fix/workaround

Table 34-8. Configure PWM and CWCM According to this Table:

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

11. PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

Problem fix/workaround

Do a write to any AWeX I/O register to re-enable the output.

12. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the V_{CC} voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until V_{CC} is above the programmed BOD level even if the BOD is disabled.

Problem fix/workaround

Do not set the BOD level higher than V_{CC} even if the BOD is not used.

13. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

14. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/workaround

None.

15. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

Problem fix/workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (that is, connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.