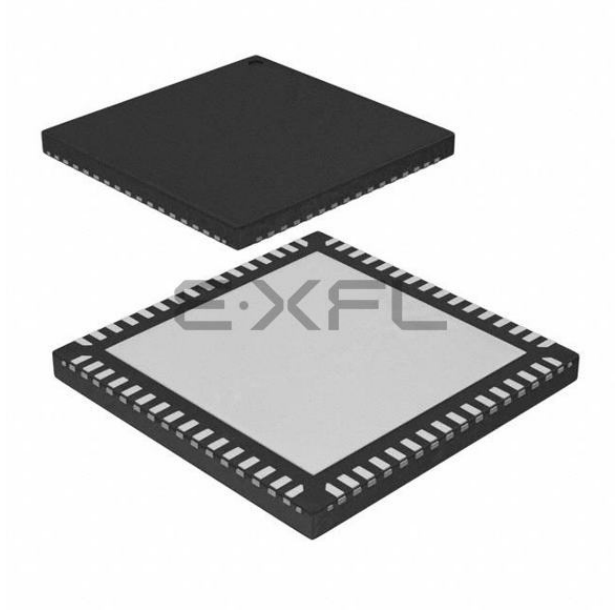

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	192KB (96K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega192d3-mn

device-dependent. These two sections have separate lock bits, and can have different levels of protection. The store program memory (SPM) instruction, which is used to write to the flash from the application software, will only operate when executed from the boot loader section.

The application section contains an application table section with separate lock settings. This enables safe storage of nonvolatile data in the program memory.

Figure 7-1. Flash Program Memory (hexadecimal address)

	Word address					
ATxmega	**32D3**	**64D3**	**128D3**	**192D3**	**256D3**	**384D3**
Application section (32K/64K/128K/192K/256K/384K)	0	0	0	0	0	0
...						
	37FF	77FF	EFFF	16FFF	1EFFF	2EFFF
Application table section (4K/4K/8K/8K/8K/8K)	3800	7800	F000	17000	1F000	2F000
	3FFF	7FFF	FFFF	17FFF	1FFFF	2FFFF
Boot section (4K/4K/8K/8K/8K/8K)	4000	8000	10000	18000	20000	30000
	47FF	87FF	10FFF	18FFF	20FFF	30FFF

7.3.1 Application Section

The application section is the section of the flash that is used for storing the executable application code. The protection level for the application section can be selected by the boot lock bits for this section. The application section can not store any boot loader code since the SPM instruction cannot be executed from the application section.

7.3.2 Application Table Section

The application table section is a part of the application section of the flash memory that can be used for storing data. The size is identical to the boot loader section. The protection level for the application table section can be selected by the boot lock bits for this section. The possibilities for different protection levels on the application section and the application table section enable safe parameter storage in the program memory. If this section is not used for data, application code can reside here.

7.3.3 Boot Loader Section

While the application section is used for storing the application code, the boot loader software must be located in the boot loader section because the SPM instruction can only initiate programming when executing from this section. The SPM instruction can access the entire flash, including the boot loader section itself. The protection level for the boot loader section can be selected by the boot loader lock bits. If this section is not used for boot loader software, the application code can be stored here.

7.3.4 Production Signature Row

The production signature row is a separate memory section for factory programmed data. It contains calibration data for functions such as oscillators and analog modules. Some of the calibration values will be automatically loaded to the corresponding module or peripheral unit during reset. Other values must be loaded from the signature row and written to the corresponding peripheral registers from software. For details on calibration conditions, refer to “Electrical Characteristics” on page 63.

The production signature row also contains an ID that identifies each microcontroller device type and a serial number for each manufactured device. The serial number consists of the production lot number, wafer number, and wafer coordinates for the device. The device ID for the available devices is shown in Table 7-1 on page 15.

PORT C	PIN #	INTERRUPT	TCC0 (1)(2)	AWEXC	TCC1	USARTC0 (3)	SPIC (4)	TWIC	CLOCKOUT (5)	EVENTOUT (6)
PC6	22	SYNC		$\overline{\text{OC0DLS}}$			MISO		RTCOUT	
PC7	23	SYNC		OC0DHS			SCK		clk_{PER}	EVOUT
GND	24									
VCC	25									

Notes:
1. Pin mapping of all TC0 can optionally be moved to high nibble of port.
2. If TC0 is configured as TC2 all eight pins can be used for PWM output.
3. Pin mapping of all USART0 can optionally be moved to high nibble of port.
4. Pins MOSI and SCK for all SPI can optionally be swapped.
5. CLKOUT can optionally be moved between port C, D, and E and between pin 4 and 7.
6. EVOUT can optionally be moved between port C, D, and E and between pin 4 and 7.

Table 28-4. Port D - Alternate Functions

PORT D	PIN #	INTERRUPT	TCD0	USARTD0	SPID	CLOCKOUT	EVENTOUT
PD0	26	SYNC	OC0A				
PD1	27	SYNC	OC0B	XCK0			
PD2	28	SYNC/ASYNC	OC0C	RXD0			
PD3	29	SYNC	OC0D	TXD0			
PD4	30	SYNC			$\overline{\text{SS}}$		
PD5	31	SYNC			MOSI		
PD6	32	SYNC			MISO		
PD7	33	SYNC			SCK	Clk_{PER}	EVOUT
GND	34						
VCC	35						

Table 28-5. Port E - Alternate Functions

PORT E	PIN #	INTERRUPT	TCE0	USARTE0	TOSC	TWIE	CLOCKOUT	EVENTOUT
PE0	36	SYNC	OC0A			SDA		
PE1	37	SYNC	OC0B	XCK0		SCL		
PE2	38	SYNC/ASYNC	OC0C	RXD0				
PE3	39	SYNC	OC0D	TXD0				
PE4	40	SYNC						
PE5	41	SYNC						
PE6	42	SYNC			TOSC2			
PE7	43	SYNC			TOSC1		Clk_{PER}	EVOUT
GND	44							
VCC	45							

32.2.14 SPI Characteristics

Figure 32-12. SPI Timing Requirements in Master Mode

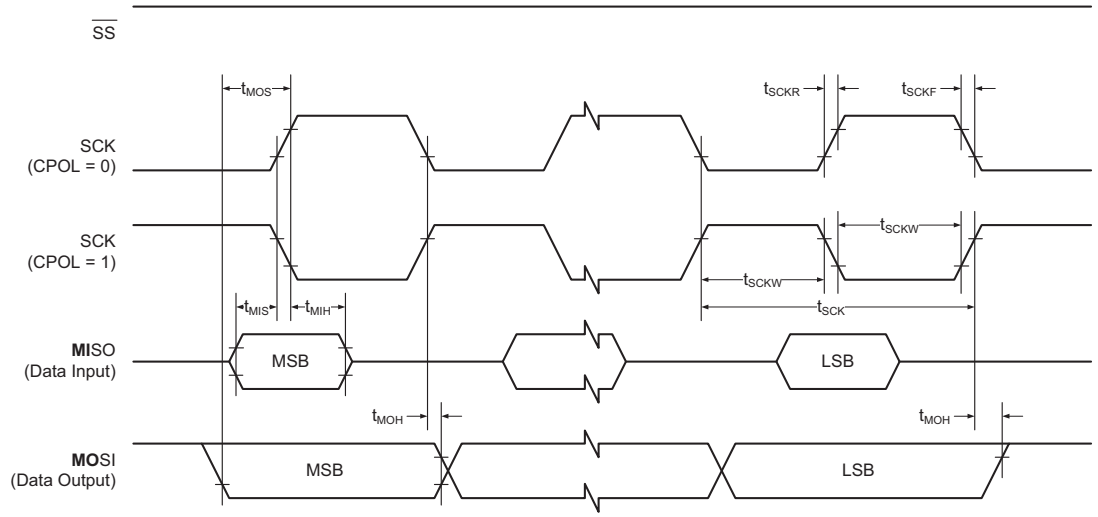
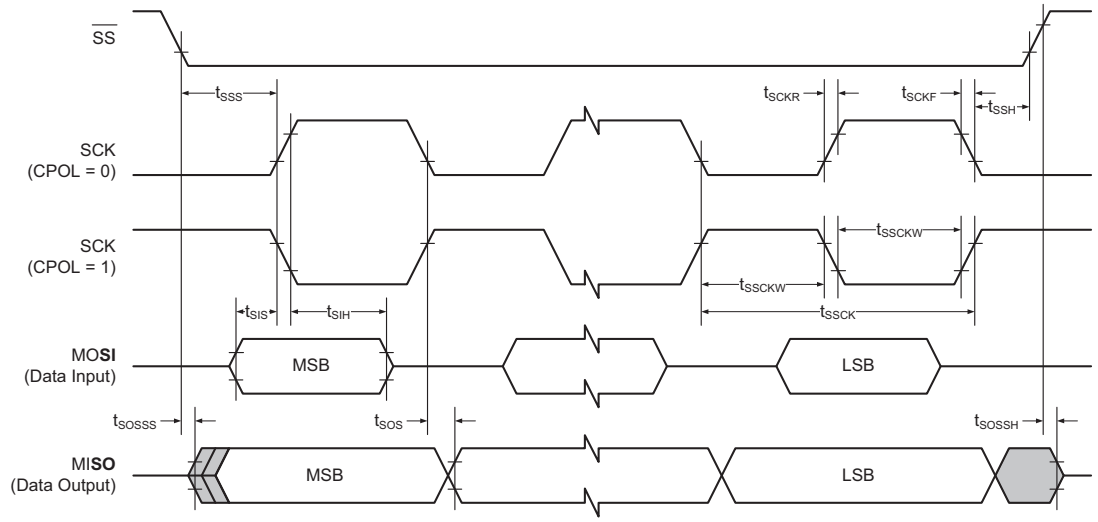


Figure 32-13.SPI Timing Requirements in Slave Mode



32.4.6 ADC Characteristics

Table 32-95. Power Supply, Reference, and Input Range

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC} - 0.3		V_{CC} + 0.3	V
V_{REF}	Reference voltage		1		AV_{CC} - 0.6	
R_{in}	Input resistance	Switched			4.5	kΩ
C_{in}	Input capacitance	Switched			5	pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF
V_{in}	Input range		0		V_{REF}	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	
	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF} - ΔV	
ΔV	Fixed offset voltage			200		lsb

Table 32-96. Clock and Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC clock frequency	Maximum is 1/4 of peripheral clock frequency	100		1800	kHz
		Measuring internal signals	100		125	
f_{ClkADC}	Sample rate		16		300	ksps
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	16		300	
		CURRLIMIT = LOW	16		250	
		CURRLIMIT = MEDIUM	16		150	
		CURRLIMIT = HIGH	16		50	
	Sampling time	Configurable in steps of 1/2 Clk_{ADC} cycles up to 32 Clk_{ADC} cycles	0.28		320	µs
	Conversion time (latency)	(RES+2)/2 + 1 + GAIN RES (Resolution) = 8 or 12, GAIN = 0 to 3	5.5		10	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	
	ADC settling time	After changing reference or input mode		7	7	

Figure 33-37. Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

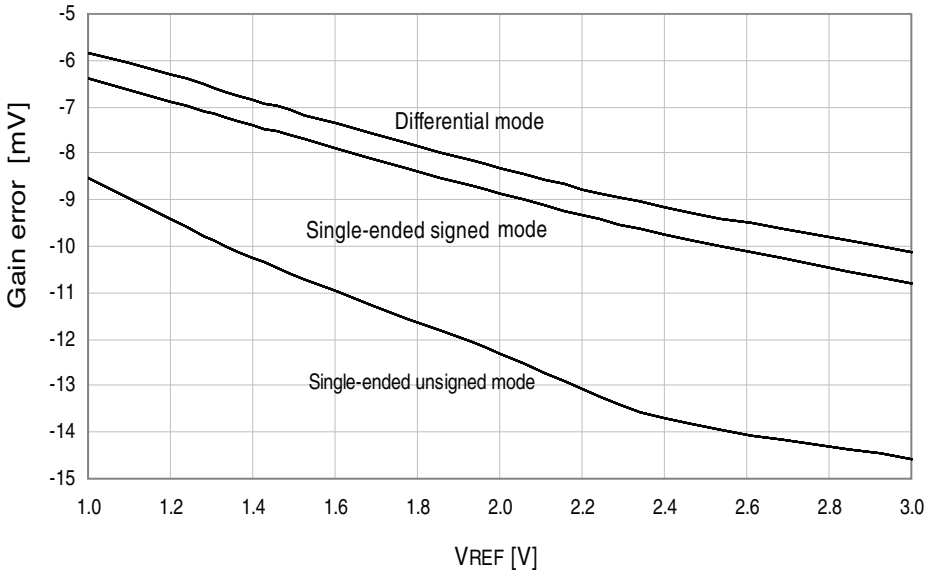


Figure 33-38. Gain Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps

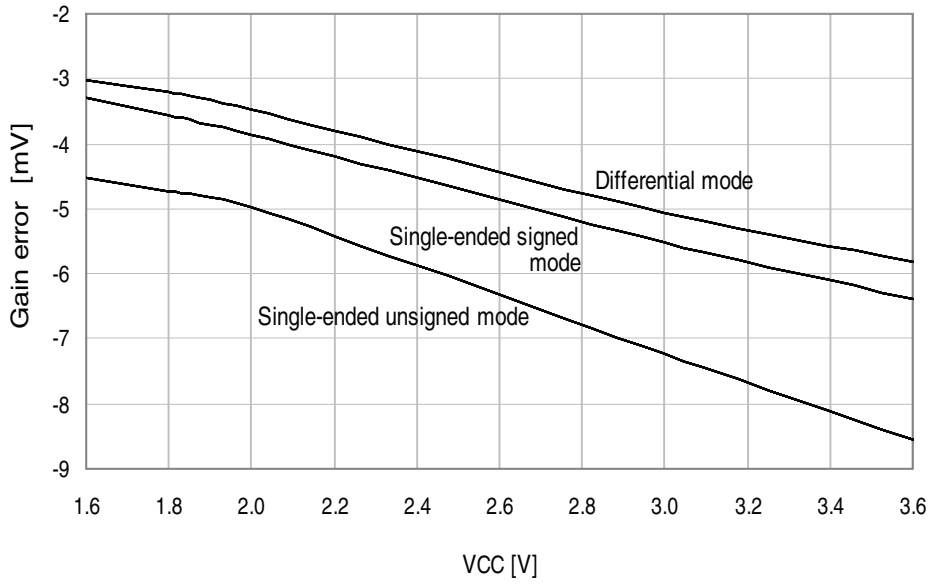


Figure 33-65. 32MHz Internal Oscillator CALA Calibration Step Size

T = 105°C, V_{CC} = 3.0V

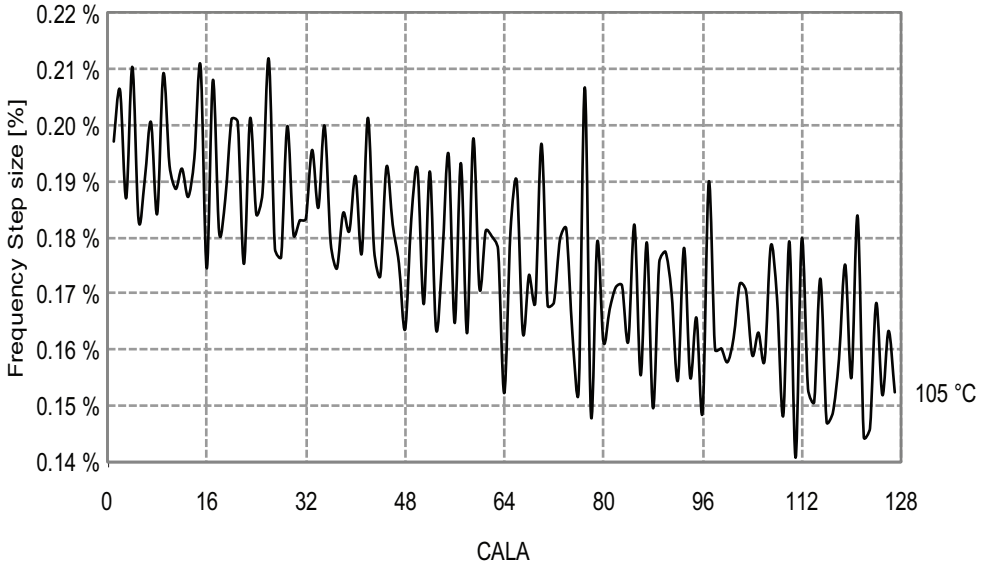


Figure 33-66. 32MHz Internal Oscillator Frequency vs. CALB Calibration Value

V_{CC} = 3.0V

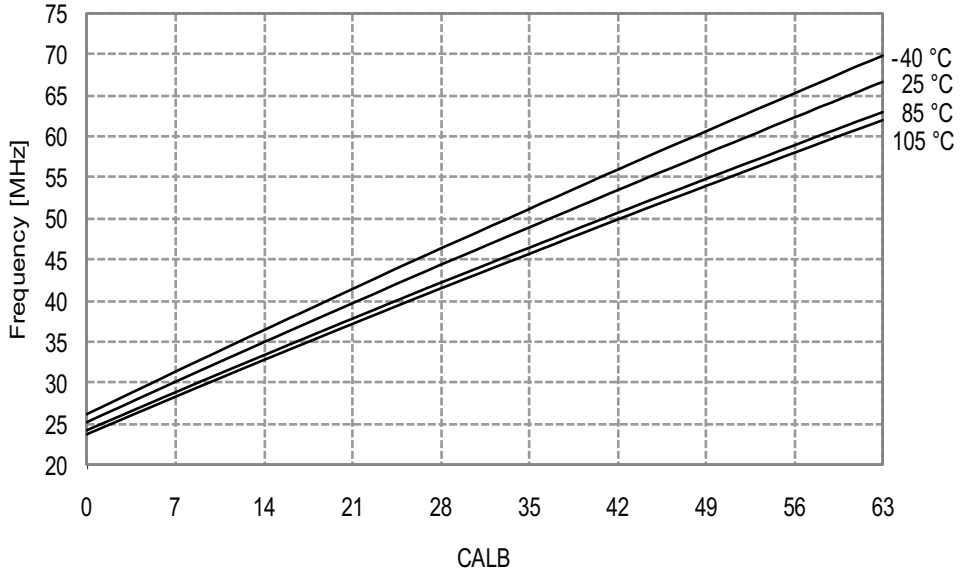


Figure 33-82. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

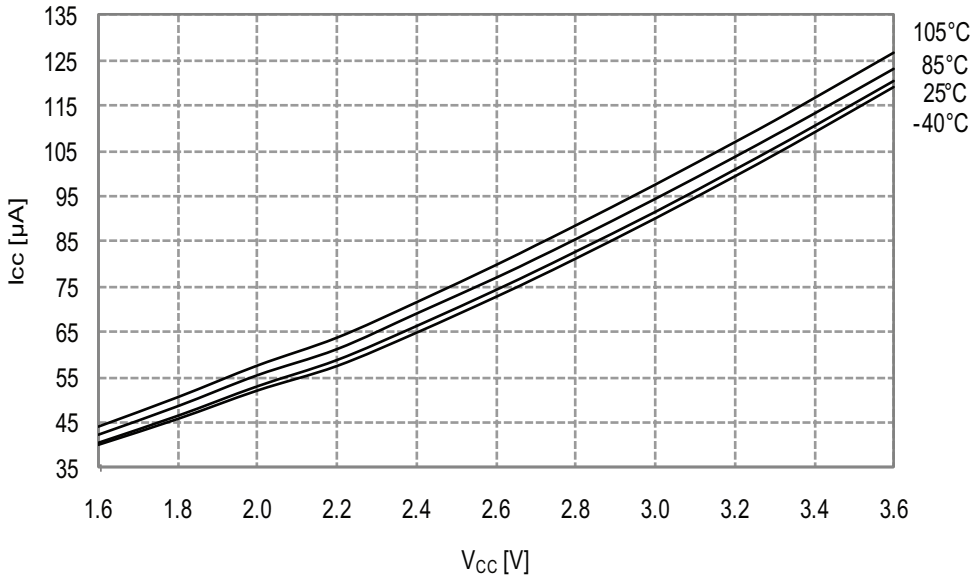
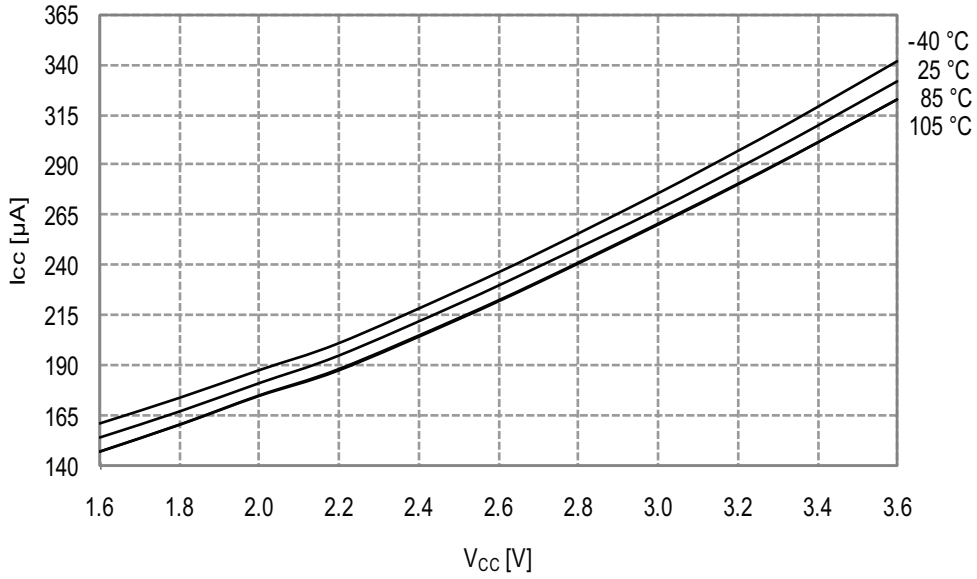


Figure 33-83. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator



33.2.7 External Reset Characteristics

Figure 33-120. Minimum Reset Pin Pulse Width vs. V_{CC}

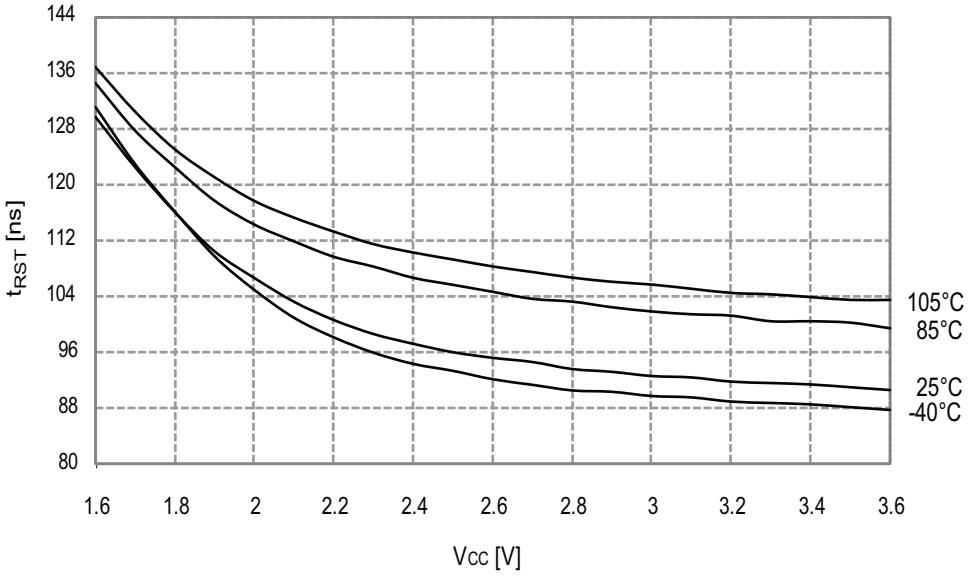


Figure 33-121. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 1.8V

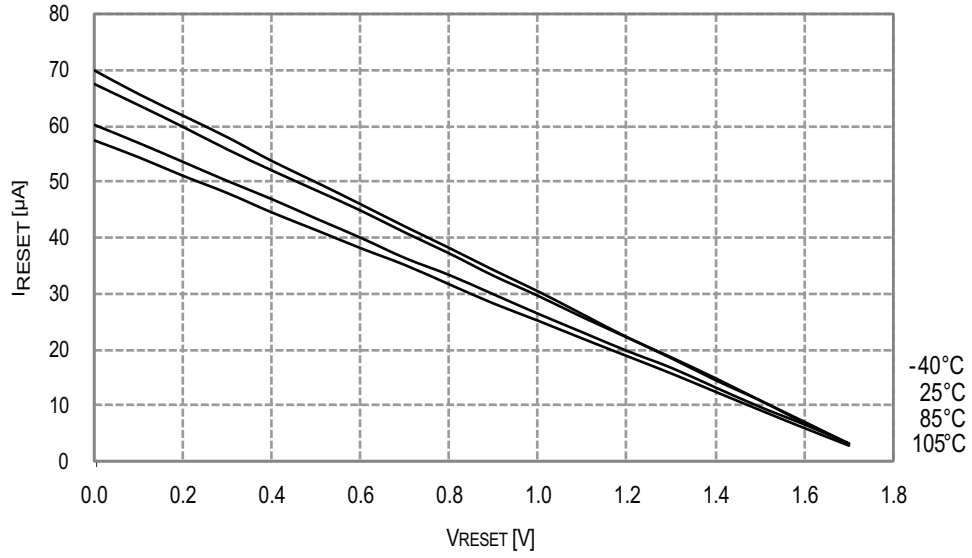


Figure 33-155. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz

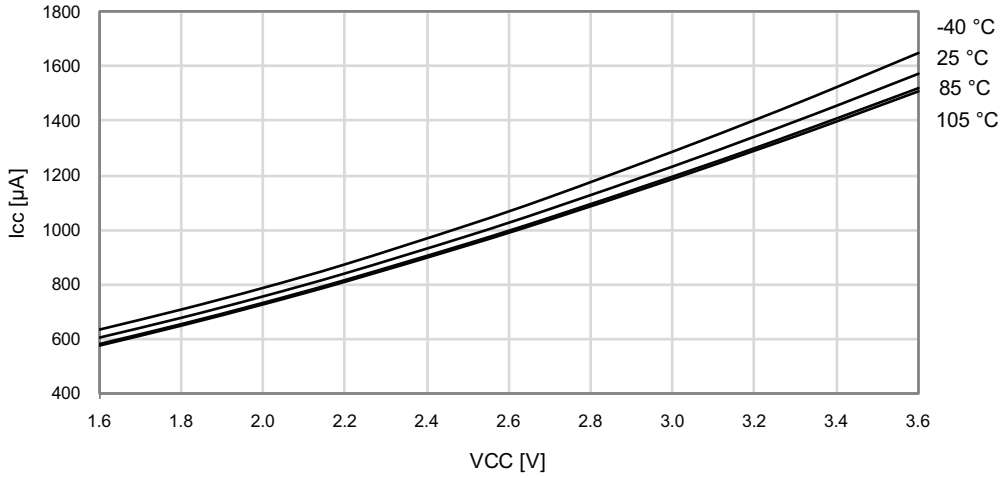


Figure 33-156. Idle Mode Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator

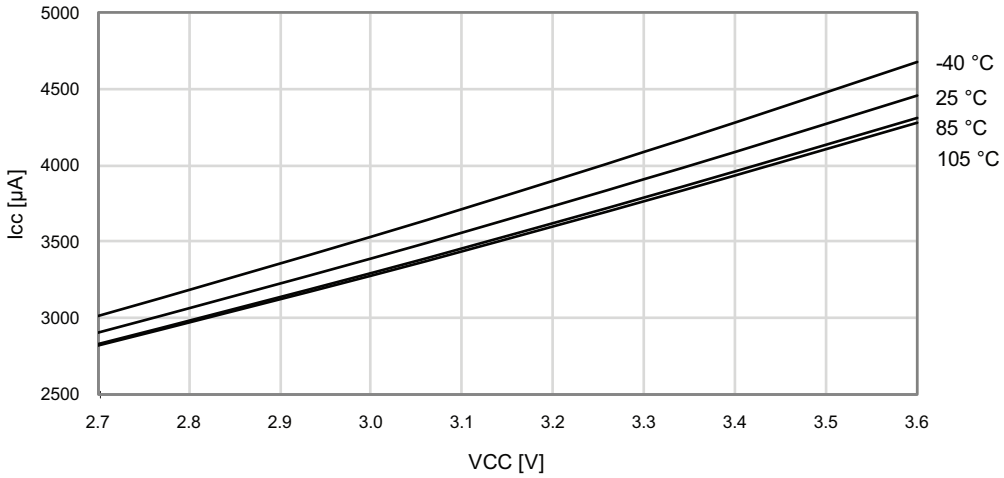


Figure 33-225.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz

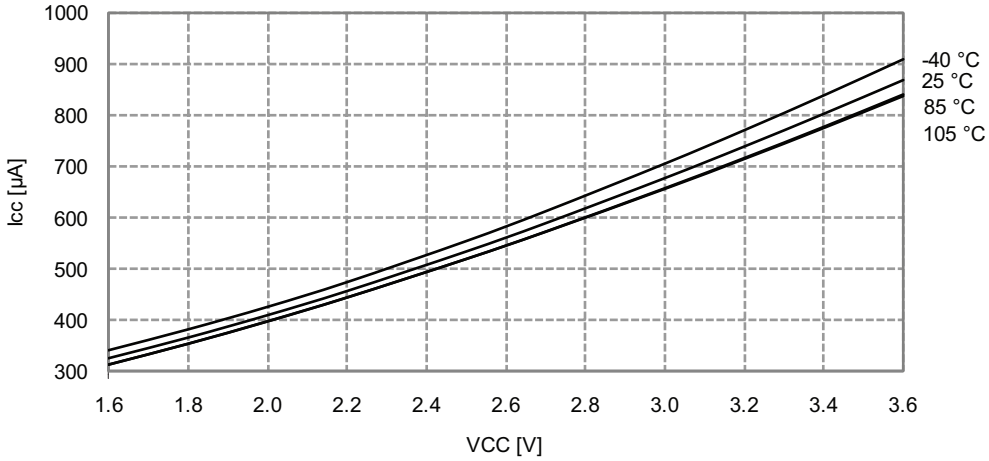
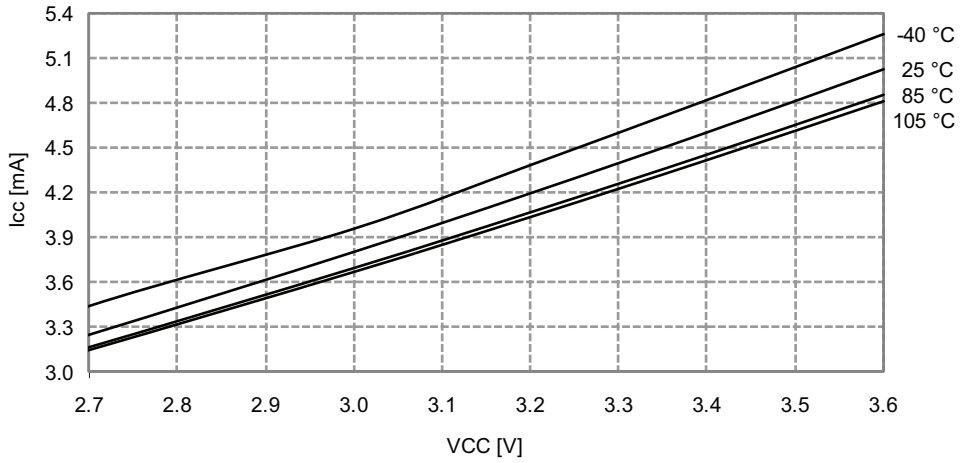


Figure 33-226.Idle Mode Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator



33.4.4 Analog Comparator Characteristics

Figure 33-253.Analog Comparator Hysteresis vs. V_{CC}

Small hysteresis

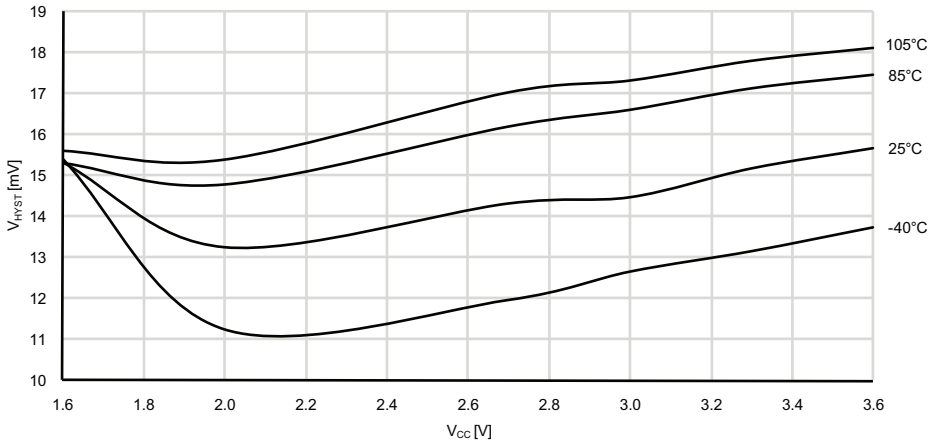


Figure 33-254.Analog Comparator Hysteresis vs. V_{CC}

Large hysteresis

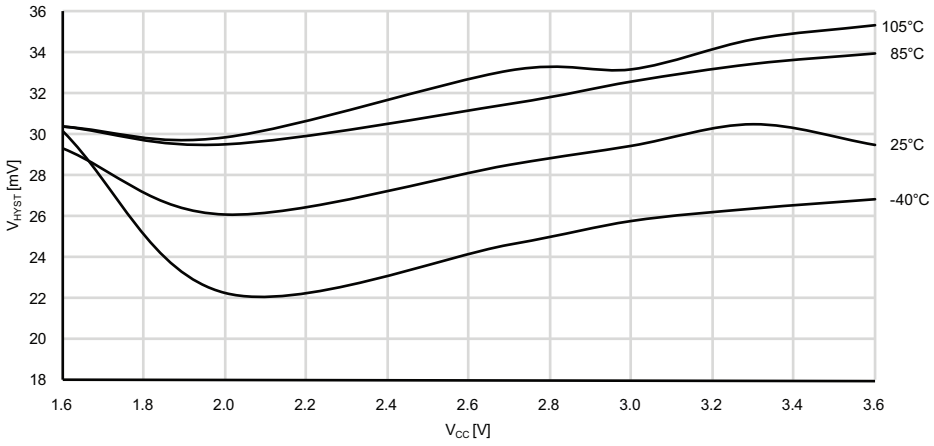


Figure 33-261.Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 1.8V

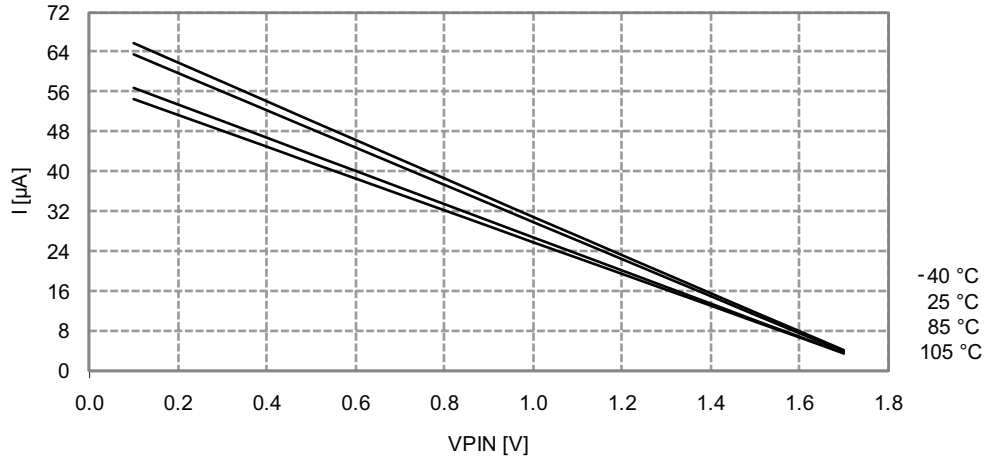
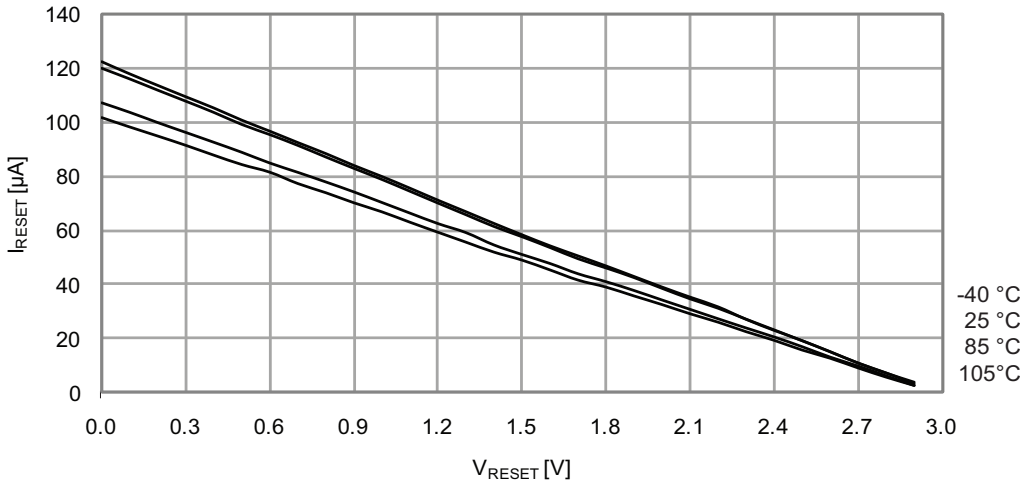


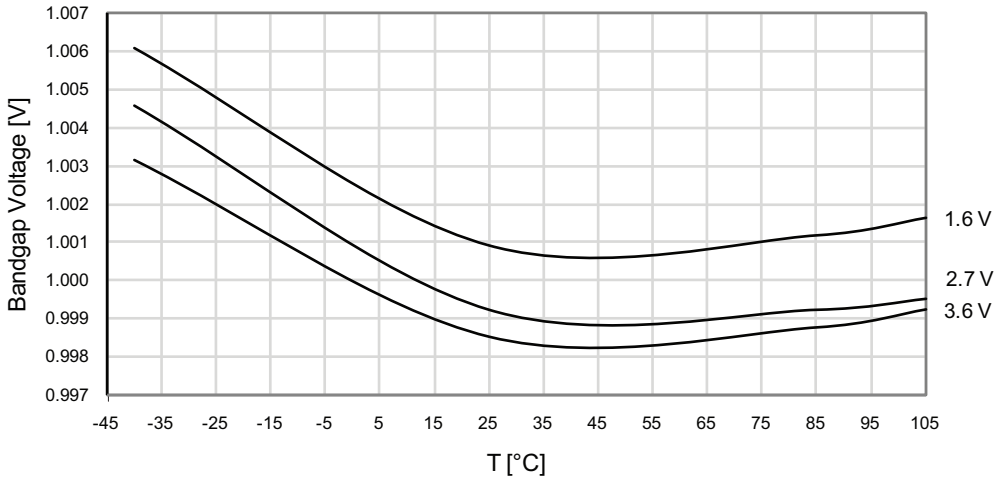
Figure 33-262.Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 3.0V



33.5.5 Internal 1.0V Reference Characteristics

Figure 33-327. ADC Internal 1.0V Reference vs. Temperature



33.5.6 BOD Characteristics

Figure 33-328. BOD Thresholds vs. Temperature

BOD level = 1.6V

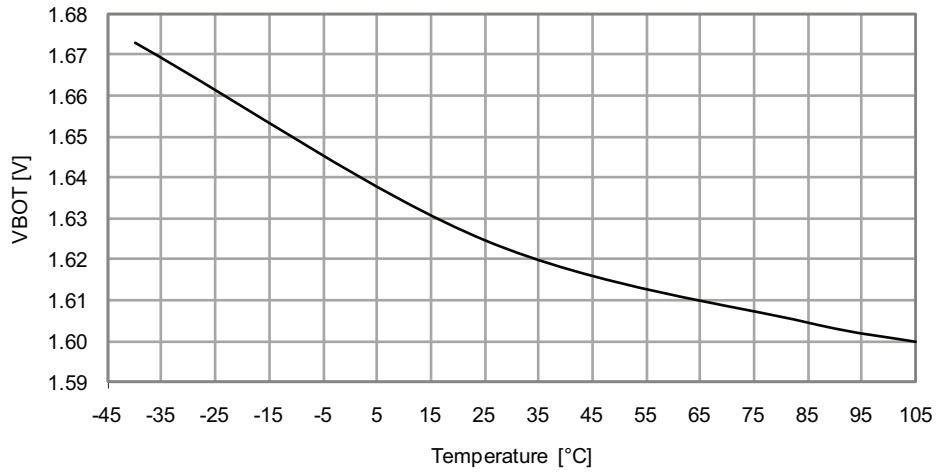
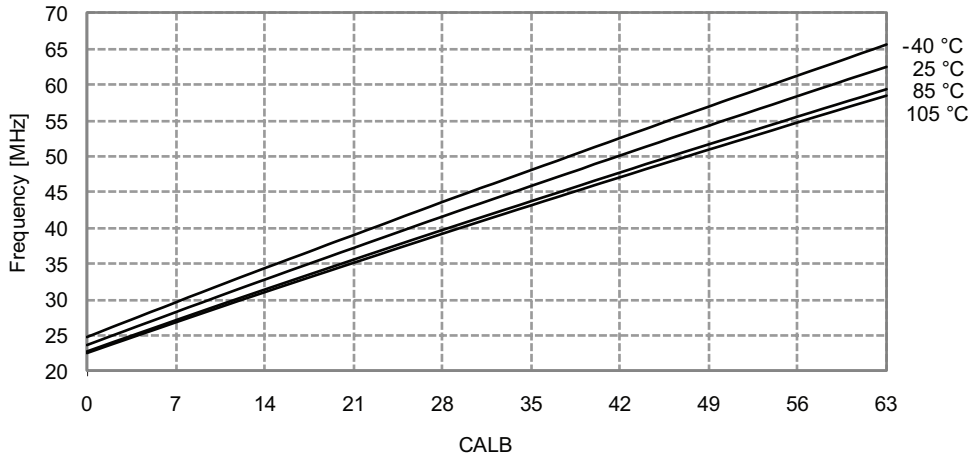


Figure 33-347. 32MHz Internal Oscillator Frequency vs. CALB Calibration Value

V_{CC} = 3.0V



33.5.8.5 32MHz Internal Oscillator Calibrated to 48MHz

Figure 33-348. 48MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled

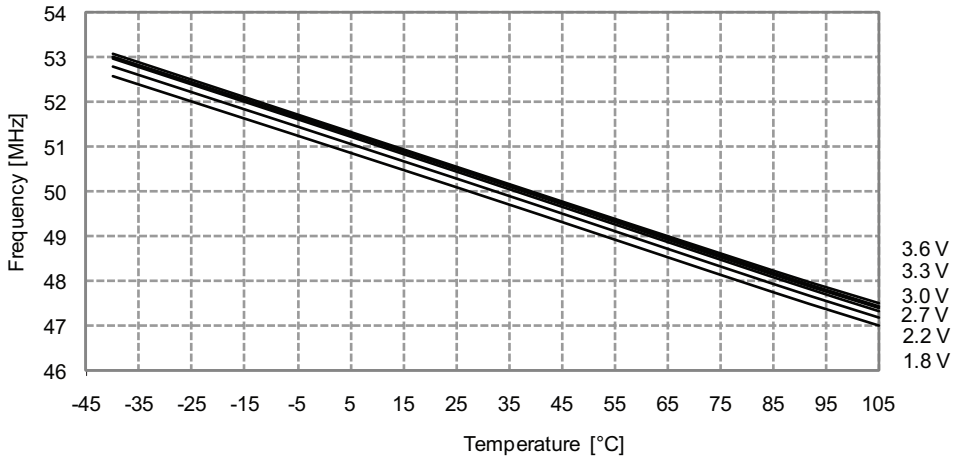


Figure 33-361.Idle Mode Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C

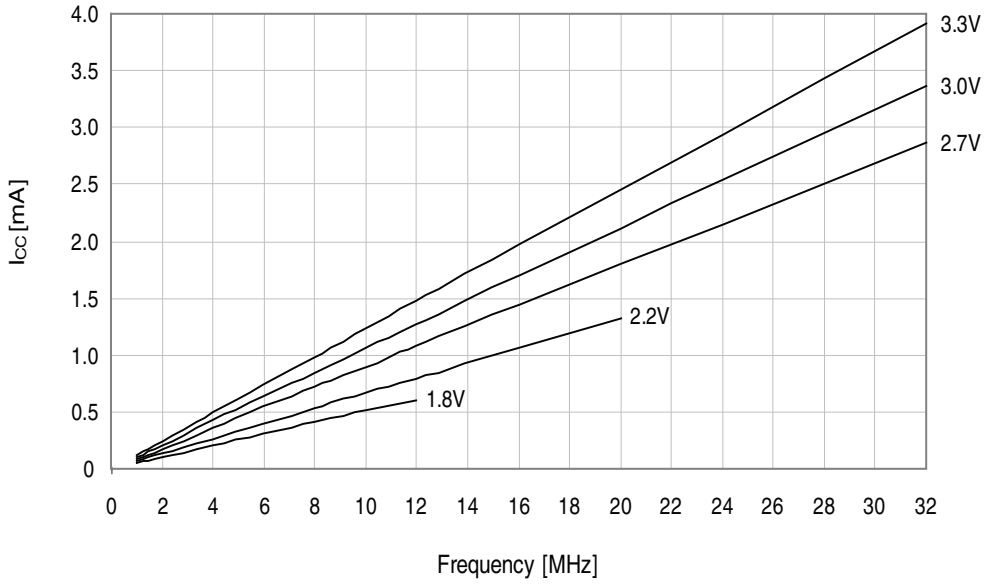


Figure 33-362.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator

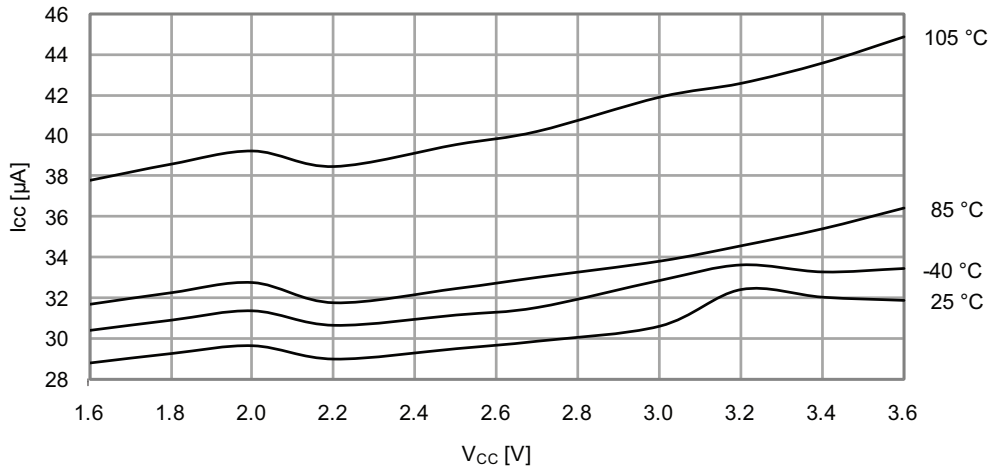


Figure 33-385. DNL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

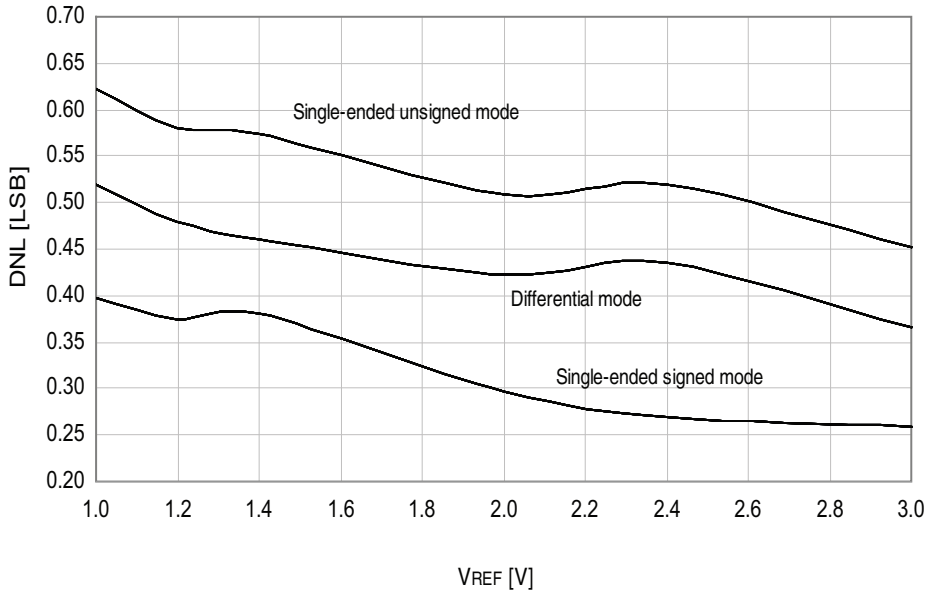
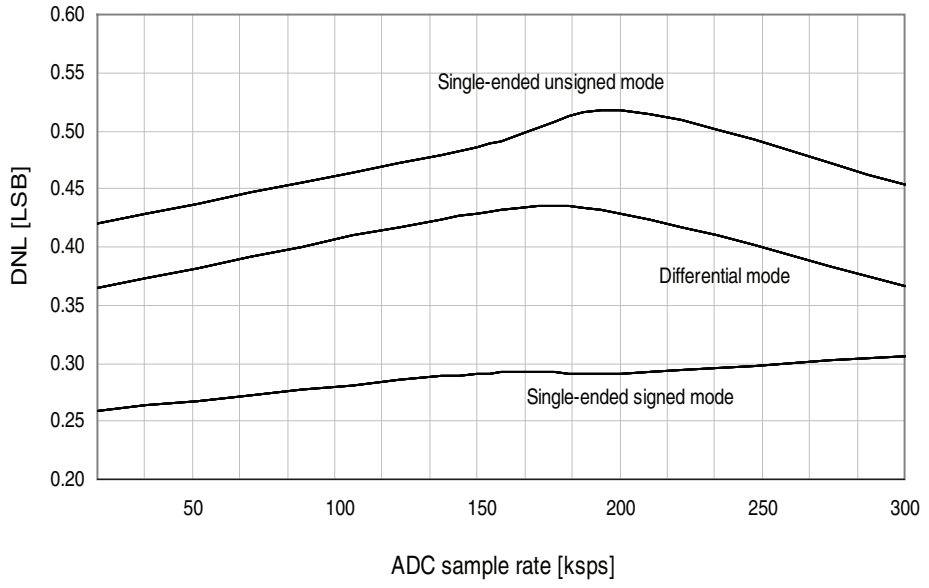


Figure 33-386. DNL Error vs. Sample Rate

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external



- 1× gain: 2.4 V
- 2× gain: 1.2 V
- 4× gain: 0.6 V
- 8× gain: 300 mV
- 16× gain: 150 mV
- 32× gain: 75 mV
- 64× gain: 38 mV

Problem fix/workaround

Keep the amplified voltage output from the ADC gain stage below 2.4V in order to get a correct result, or keep ADC voltage reference below 2.4V.

6. ADC Event on compare match non-functional

ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

Problem fix/workaround

Enable and use interrupt on compare match when using the compare function.

7. ADC propagation delay is not correct when 8× – 64× gain is used

The propagation delay will increase by only one ADC clock cycle for all gain settings.

Problem fix/workaround

None.

8. Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V

The ADC can not be used to do bandgap measurements when V_{CC} is below 2.7V.

Problem fix/workaround

None.

9. Accuracy lost on first three samples after switching input to ADC gain stage

Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

Problem fix/workaround

Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

10. Configuration of PGM and CWCM not as described in XMEGA D Manual

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

34.3 Atmel ATxmega128D3

34.3.1 Rev. J

- AC system status flags are only valid if AC-system is enabled
- Sampled BOD in Active mode will cause noise when bandgap is used as reference
- Temperature sensor not calibrated

1. AC system status flags are only valid if AC-system is enabled

The status flags for the ac-output are updated even though the AC is not enabled which is invalid. Also, it is not possible to clear the AC interrupt flags without enabling either of the Analog comparators.

Problem fix/workaround

Software should clear the AC system flags once, after enabling the AC system before using the AC system status flags.

2. Sampled BOD in Active mode will cause noise when bandgap is used as reference

Using the BOD in sampled mode when the device is running in Active or Idle mode will add noise on the bandgap reference for ADC, DAC and Analog Comparator.

Problem fix/workaround

If the bandgap is used as reference for either the ADC, DAC and Analog Comparator, the BOD must not be set in sampled mode.

3. Temperature sensor not calibrated

Temperature sensor factory calibration not implemented.

Problem fix/workaround

None.

34.3.2 Rev. I

Not sampled.

34.3.3 Rev. H

Not sampled.

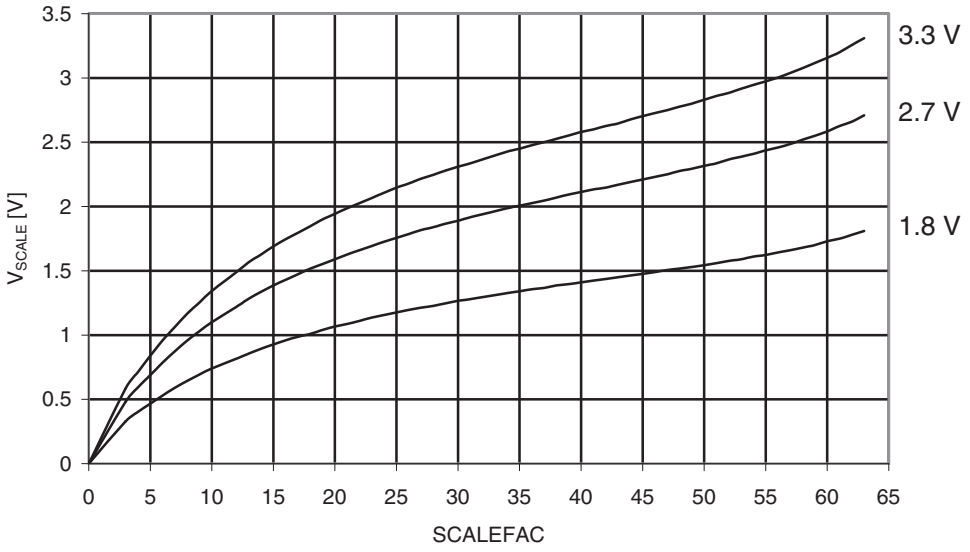
34.3.4 Rev. G

Not sampled.

34.3.5 Rev. F

Not sampled.

Figure 34-4. Analog Comparator Voltage Scaler vs. Scalefac
T = 25°C



Problem fix/workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed.

3. ADC gain stage cannot be used for single conversion

The ADC gain stage will not output correct result for single conversion that is triggered and started from software or event system.

Problem fix/workaround

When the gain stage is used, the ADC must be set in free running mode for correct results.

4. ADC has increased INL error for some operating conditions

Some ADC configurations or operating condition will result in increased INL error.

In signed mode INL is increased to:

6LSB for sample rates above 130ksps, and up to 8LSB for 200ksps sample rate.

6LSB for reference voltage below 1.1V when V_{CC} is above 3.0V.

20LSB for ambient temperature below 0°C and reference voltage below 1.3V.

In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

Problem fix/workaround

None, avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

5. ADC gain stage output range is limited to 2.4V

The amplified output of the ADC gain stage will never go above 2.4V, hence the differential input will only give correct output when below 2.4V/gain. For the available gain settings, this gives a differential input range of:

35. Datasheet revision history

Note that the referring page numbers in this section are referred to this document. The referring revisions in this section are referring to the document revision.

35.1 8134Q – 10/2015

1.	Updated "Ordering Information" on page 2. • All ATxmegayyD3-MT and ATxmegayyD3-MTR changed respectively to ATxmegayyD3-MN and ATxmegayyD3-MNR

35.2 8134P – 11/2014

1.	Changed EEPROM value for ATxmega32D3 to 1K in Section 1. "Ordering Information" on page 2, in Figure 7-2 on page 16 and in Table 7-3 on page 18.
2.	Section naming in Chapter "Typical Characteristics" has been corrected.

35.3 8134O – 09/2014

1.	Updated "Ordering Information" on page 2. Added Ordering codes for the devices characterized @ 105°C.
2.	Updated "Electrical Characteristics" on page 63: • Updated Table 32-4 on page 65, Table 32-33 on page 84, Table 32-62 on page 103, Table 32-91 on page 122, Table 32-120 on page 141 and Table 32-149 on page 160. Added I_{CC} Power-down power consumption for T=105°C for all functions disabled and for WDT and sampled BOD enabled. • Updated,Table 32-17 on page 73, Table 32-46 on page 92, Table 32-75 on page 111, Table 32-104 on page 130, Table 32-133 on page 149, and Table 32-162 on page 168. Updated all tables to include values for T=85°C and T=105°C. Removed T=55°C.
3.	Updated "Typical Characteristics" on page 177. Added 105°C characteristics.
4.	Changed Vcc to AV_{CC} in Section 25. "ADC – 12-bit Analog to Digital Converter" on page 45 and Section 26. "AC – Analog Comparator" on page 47.
5.	Added ERRATA concerning disabling of the USART transmitter in Section 34.2 "Atmel ATxmega64D3" on page 389, Section 34.3 "Atmel ATxmega128D3" on page 405 and Section 34.5 "Atmel ATxmega256D3" on page 437.

35.4 8134N – 03/2014

1.	Updated Table 28-2 on page 52. PORT PB1 has PIN# 7