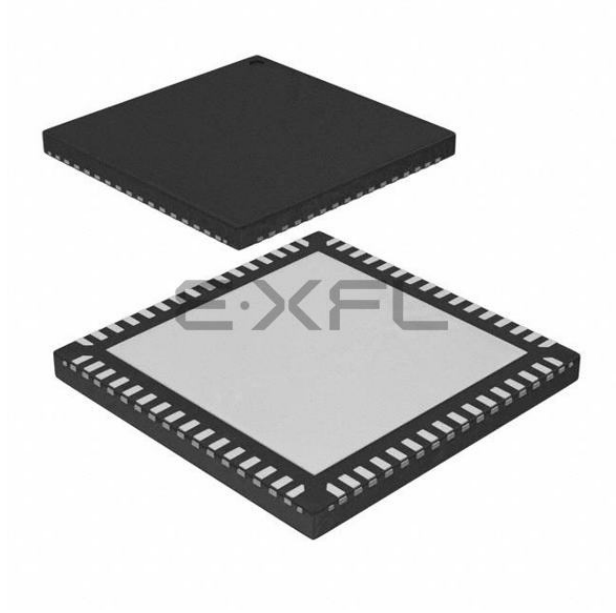

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

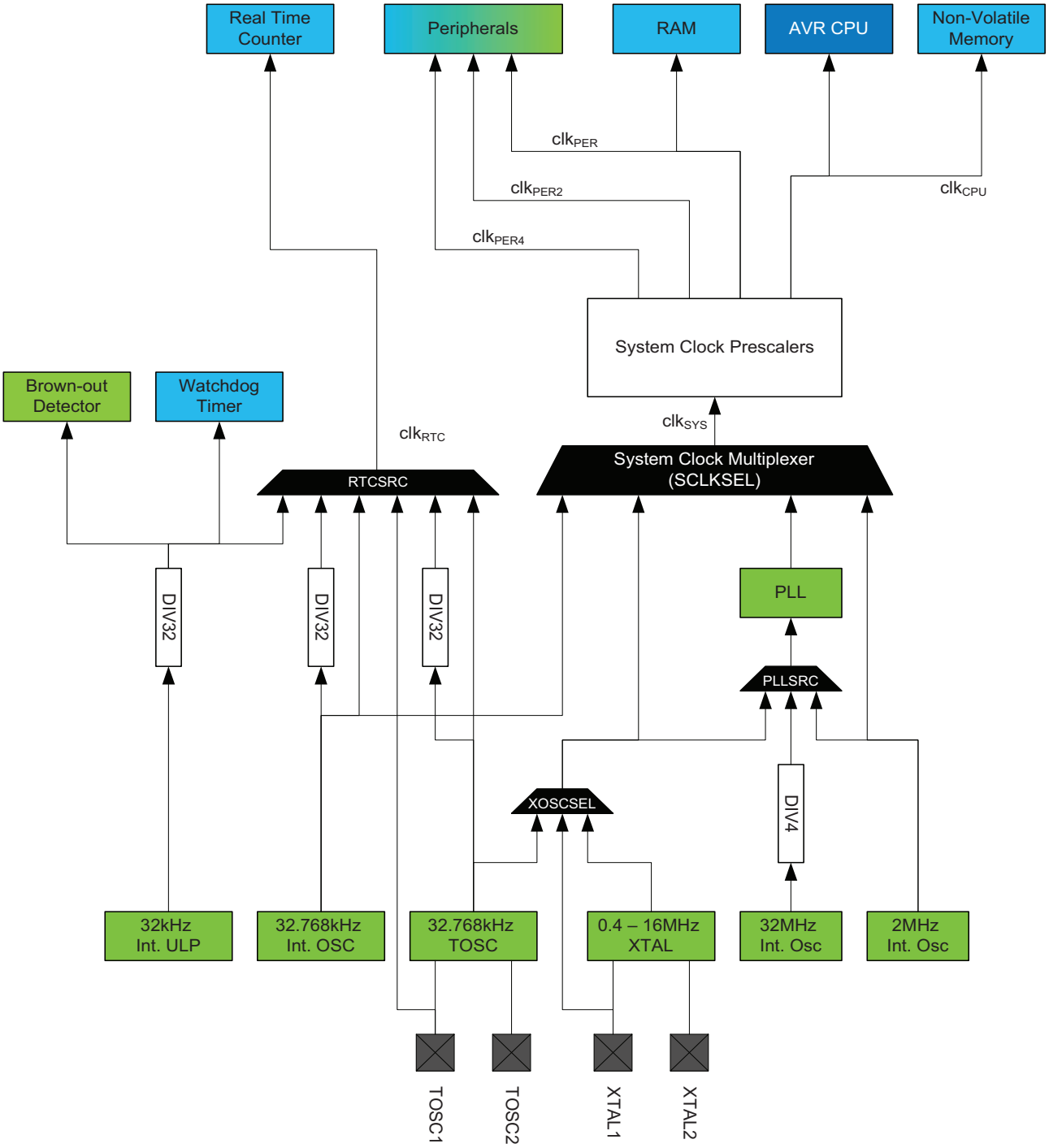
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega256d3-mh

Ordering code	Flash [bytes]	EEPROM [bytes]	SRAM [bytes]	Speed [MHz]	Power supply	Package (1)(2)(3)	Temp.
ATxmega32D3-AN	32K + 4K	1K	4K	32	1.6 - 3.6V	64A	-40°C - 105°C
ATxmega32D3-ANR (4)	32K + 4K	1K	4K				
ATxmega64D3-AN	64K + 4K	2K	4K				
ATxmega64D3-ANR (4)	64K + 4K	2K	4K				
ATxmega128D3-AN	128K + 8K	2K	8K				
ATxmega128D3-ANR (4)	128K + 8K	2K	8K				
ATxmega192D3-AN	192K + 8K	2K	16K				
ATxmega192D3-ANR (4)	192K + 8K	2K	16K				
ATxmega256D3-AN	256K + 8K	4K	16K				
ATxmega256D3-ANR (4)	256K + 8K	4K	16K				
ATxmega384D3-AN	384K + 8K	4K	32K				
ATxmega384D3-ANR (4)	384K + 8K	4K	32K				
ATxmega32D3-MN	32K + 4K	1K	4K			64M	
ATxmega32D3-MNR (4)	32K + 4K	1K	4K				
ATxmega64D3-MN	64K + 4K	2K	4K				
ATxmega64D3-MNR (4)	64K + 4K	2K	4K				
ATxmega128D3-MN	128K + 8K	2K	8K				
ATxmega128D3-MNR (4)	128K + 8K	2K	8K				
ATxmega192D3-MN	192K + 8K	2K	16K				
ATxmega192D3-MNR (4)	192K + 8K	2K	16K				
ATxmega256D3-MN	256K + 8K	4K	16K				
ATxmega256D3-MNR (4)	256K + 8K	4K	16K				
ATxmega384D3-MN	384K + 8K	4K	32K				
ATxmega384D3-MNR (4)	384K + 8K	4K	32K				

Notes:
1. This device can also be supplied in wafer form. Contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information, see "Packaging Information" on page 61.
4. Tape and Reel.

Figure 9-1. The Clock System, Clock Sources, and Clock Distribution



9.3 Clock Sources

The clock sources are divided in two main groups: internal oscillators and external clock sources. Most of the clock sources can be directly enabled and disabled from software, while others are automatically enabled or disabled, depending on peripheral settings. After reset, the device starts up running from the 2MHz internal oscillator. The other clock sources, DFLLs and PLL, are turned off by default.

The internal oscillators do not require any external components to run. For details on characteristics and accuracy of the internal oscillators, refer to the device datasheet.

11.4 Reset Sources

11.4.1 Power-on Reset

A power-on reset (POR) is generated by an on-chip detection circuit. The POR is activated when the V_{CC} rises and reaches the POR threshold voltage (V_{POT}), and this will start the reset sequence.

The POR is also activated to power down the device properly when the V_{CC} falls and drops below the V_{POT} level.

The V_{POT} level is higher for falling V_{CC} than for rising V_{CC}. Consult the datasheet for POR characteristics data.

11.4.2 Brownout Detection

The on-chip brownout detection (BOD) circuit monitors the V_{CC} level during operation by comparing it to a fixed, programmable level that is selected by the BODLEVEL fuses. If disabled, BOD is forced on at the lowest level during chip erase and when the PDI is enabled.

11.4.3 External Reset

The external reset circuit is connected to the external $\overline{\text{RESET}}$ pin. The external reset will trigger when the $\overline{\text{RESET}}$ pin is driven below the $\overline{\text{RESET}}$ pin threshold voltage, V_{RST}, for longer than the minimum pulse period, t_{EXT}. The reset will be held as long as the pin is kept low. The $\overline{\text{RESET}}$ pin includes an internal pull-up resistor.

11.4.4 Watchdog Reset

The watchdog timer (WDT) is a system function for monitoring correct program operation. If the WDT is not reset from the software within a programmable timeout period, a watchdog reset will be given. The watchdog reset is active for one to two clock cycles of the 2MHz internal oscillator. For more details see “WDT – Watchdog Timer” on page 27.

11.4.5 Software Reset

The software reset makes it possible to issue a system reset from software by writing to the software reset bit in the reset control register. The reset will be issued within two CPU clock cycles after writing the bit. It is not possible to execute any instruction from when a software reset is requested until it is issued.

11.4.6 Program and Debug Interface Reset

The program and debug interface reset contains a separate reset source that is used to reset the device during external programming and debugging. This reset source is accessible only from external debuggers and programmers.

21. SPI – Serial Peripheral Interface

21.1 Features

- Two identical SPI peripherals
- Full-duplex, three-wire synchronous data transfer
- Master or slave operation
- Lsb first or msb first data transfer
- Eight programmable bit rates
- Interrupt flag at the end of transmission
- Write collision flag to indicate data collision
- Wake up from idle sleep mode
- Double speed master mode

21.2 Overview

The Serial Peripheral Interface (SPI) is a high-speed synchronous data transfer interface using three or four pins. It allows fast communication between an Atmel AVR XMEGA device and peripheral devices or between several microcontrollers. The SPI supports full-duplex communication.

A device connected to the bus must act as a master or slave. The master initiates and controls all data transactions.

PORTC and PORTD each has one SPI. Notation of these peripherals are SPIC and SPID, respectively.

32.2.13 Clock and Oscillator Characteristics

32.2.13.1 Calibrated 32.768kHz Internal Oscillator Characteristics

Table 32-48. 32.768kHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

32.2.13.2 Calibrated 2MHz RC Internal Oscillator Characteristics

Table 32-49. 2MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8	2.0	2.2	MHz
	Factory calibrated frequency			2.0		
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration stepsize			0.18		

32.2.13.3 Calibrated 32MHz Internal Oscillator Characteristics

Table 32-50. 32MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30	32	55	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration step size			0.19		

32.2.13.4 32kHz Internal ULP Oscillator Characteristics

Table 32-51. 32kHz Internal ULP Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			32		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-12		12	%
	Accuracy		-30		30	

32.3.8 Bandgap and Internal 1.0V Reference Characteristics

Table 32-71. Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC		1 Clk_{PER} + 2.5µs		µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T = 85°C, after calibration	0.99	1.0	1.01	
	Variation over voltage and temperature	Calibrated at T = 85°C		1		%

32.3.9 Brownout Detection Characteristics

Table 32-72. Brownout Detection Characteristics (1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.40	1.60	1.70	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.0		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

32.3.10 External Reset Characteristics

Table 32-73. External Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width		1000	100		ns
V_{RST}	Reset threshold voltage	V_{CC} = 2.7 - 3.6V		0.45 * V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.45 * V_{CC}		
R_{RST}	Reset pin pull-up resistor			27		kΩ

32.3.14 SPI Characteristics

Figure 32-19.SPI Timing Requirements in Master Mode

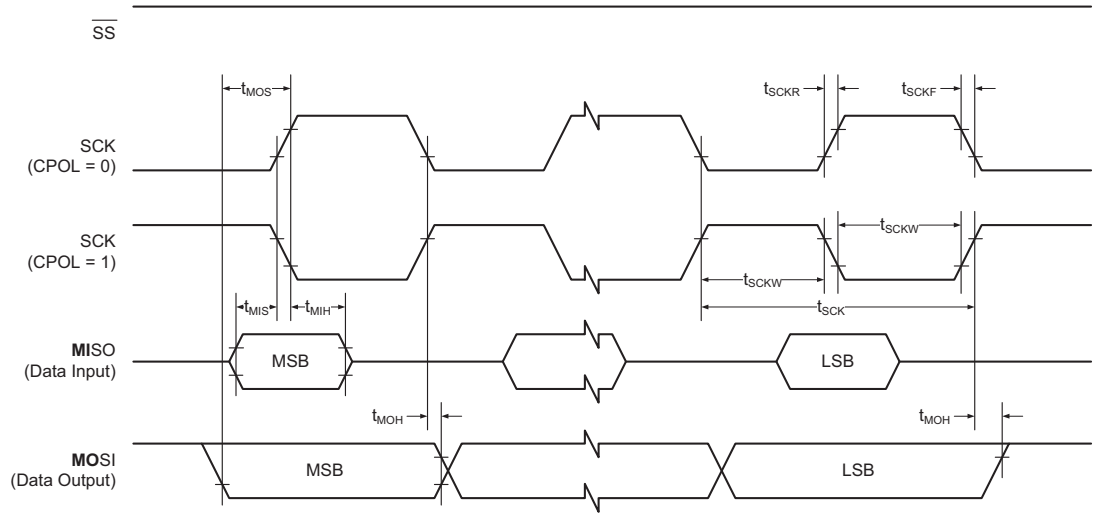


Figure 32-20.SPI Timing Requirements in Slave Mode

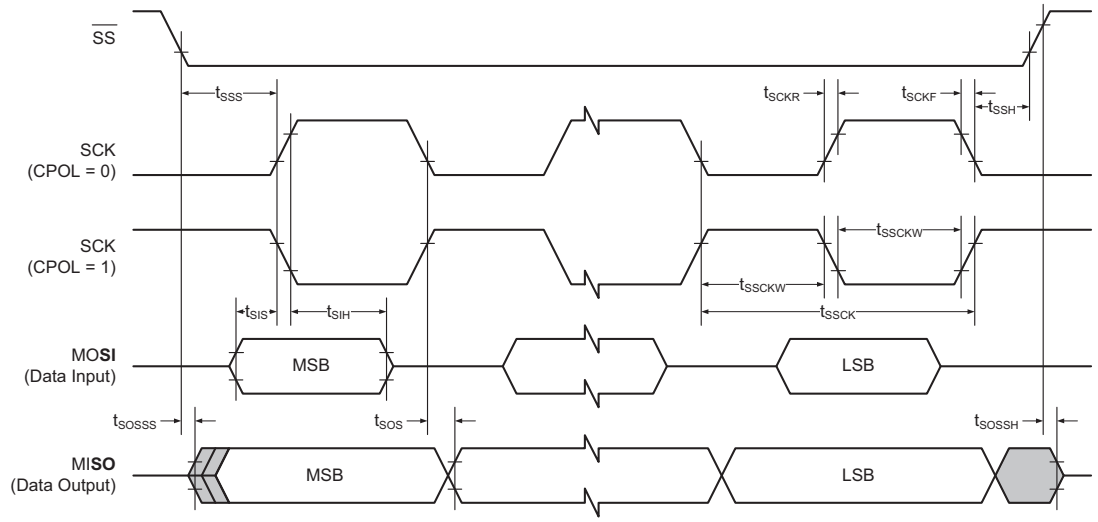


Figure 32-22.Maximum Frequency vs. V_{CC}

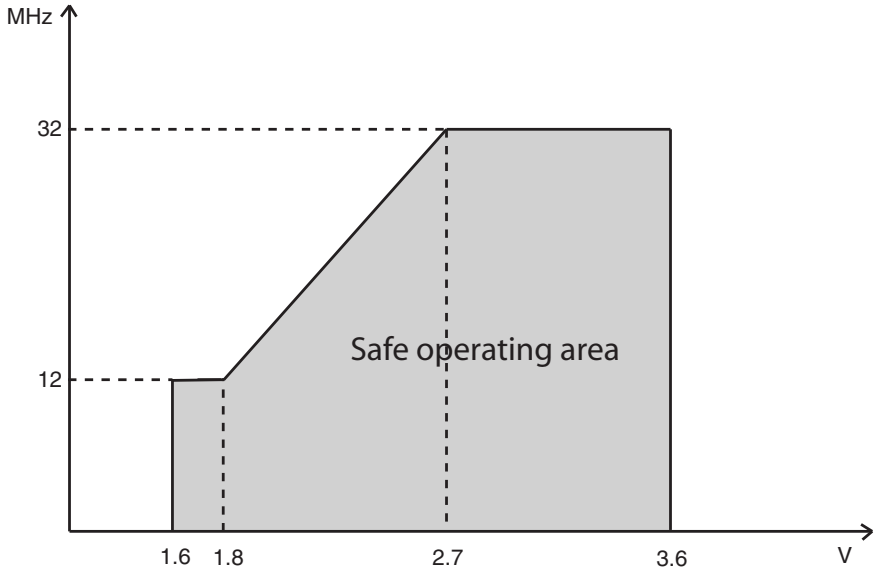
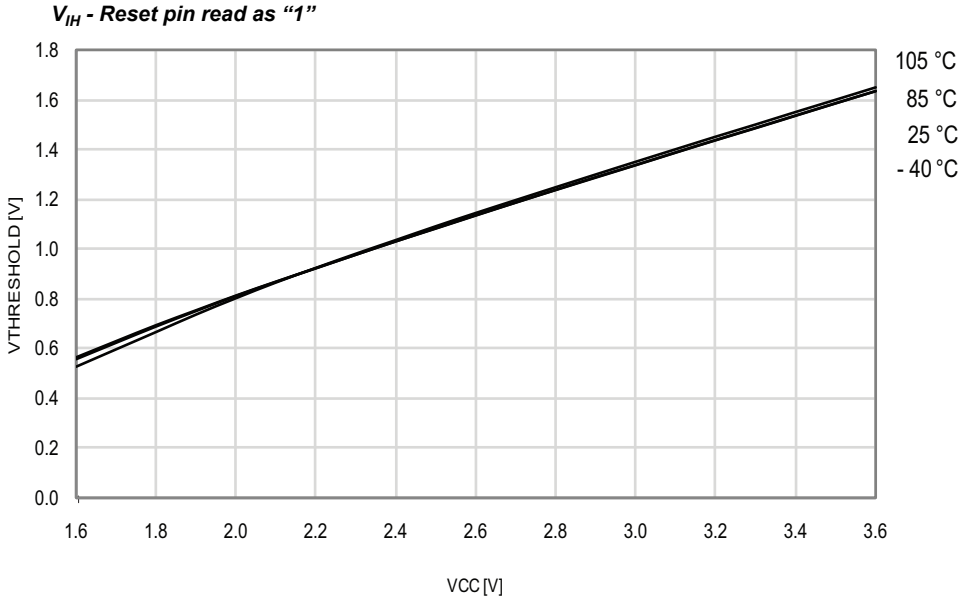


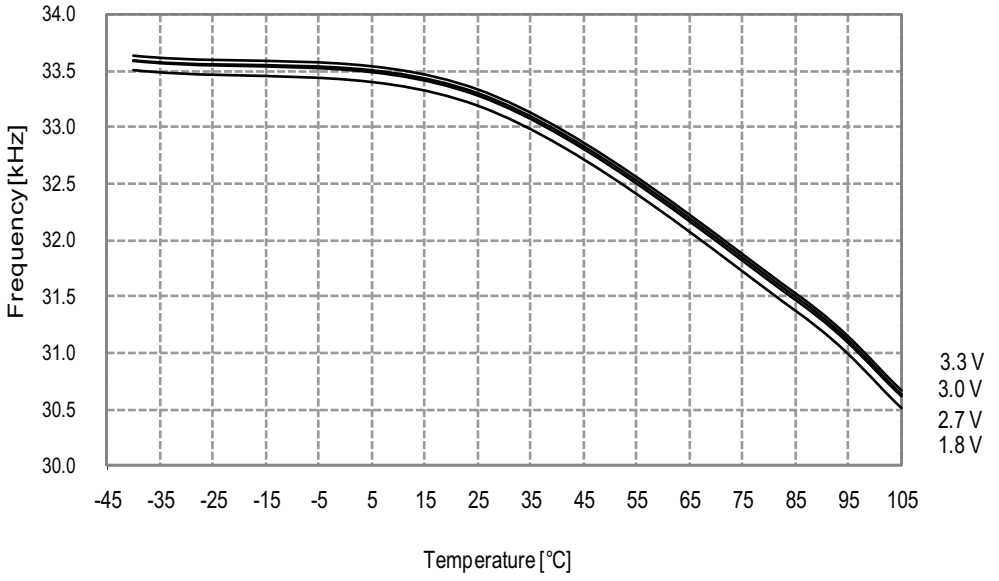
Figure 33-53. Reset Pin Input Threshold Voltage vs. V_{CC}



33.1.8 Oscillator Characteristics

33.1.8.1 Ultra Low-power Internal Oscillator

Figure 33-54. Ultra Low-power Internal Oscillator Frequency vs. Temperature



33.2.1.3 Power-down Mode Supply Current

Figure 33-86. Power-down Mode Supply Current vs. V_{CC}

All functions disabled

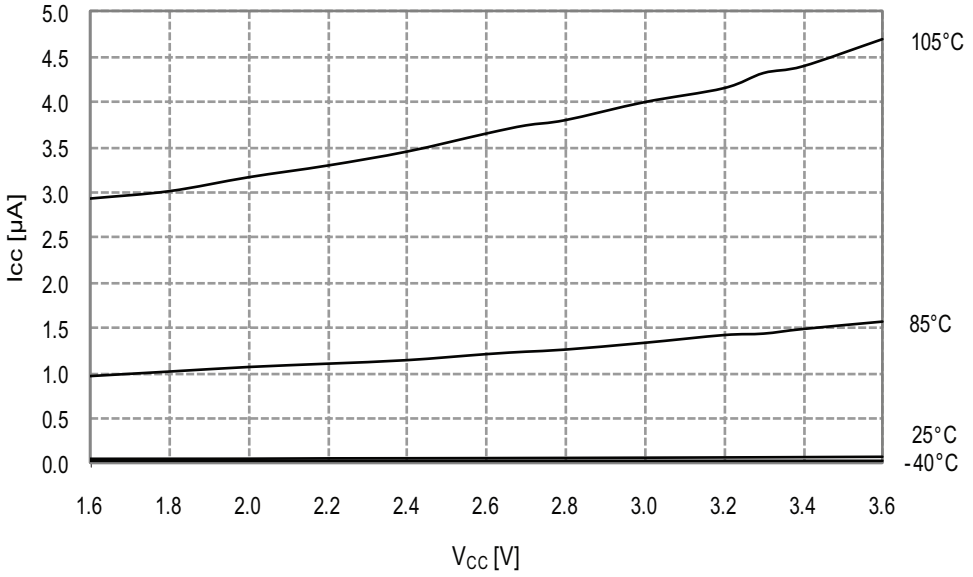
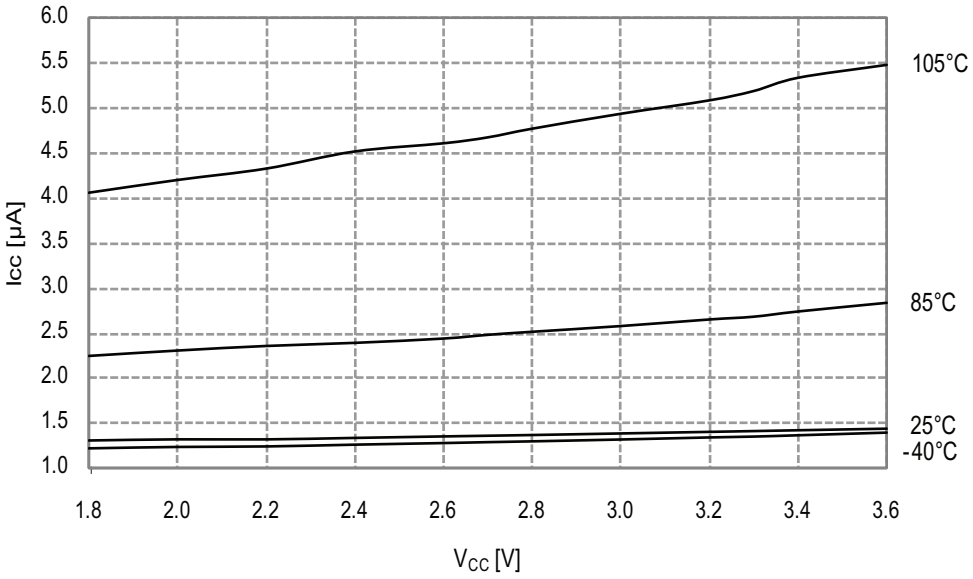


Figure 33-87. Power-down Mode Supply Current vs. V_{CC}

Watchdog and sampled BOD enabled



33.2.2 I/O Pin Characteristics

33.2.2.1 Pull-up

Figure 33-90. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = 1.8V

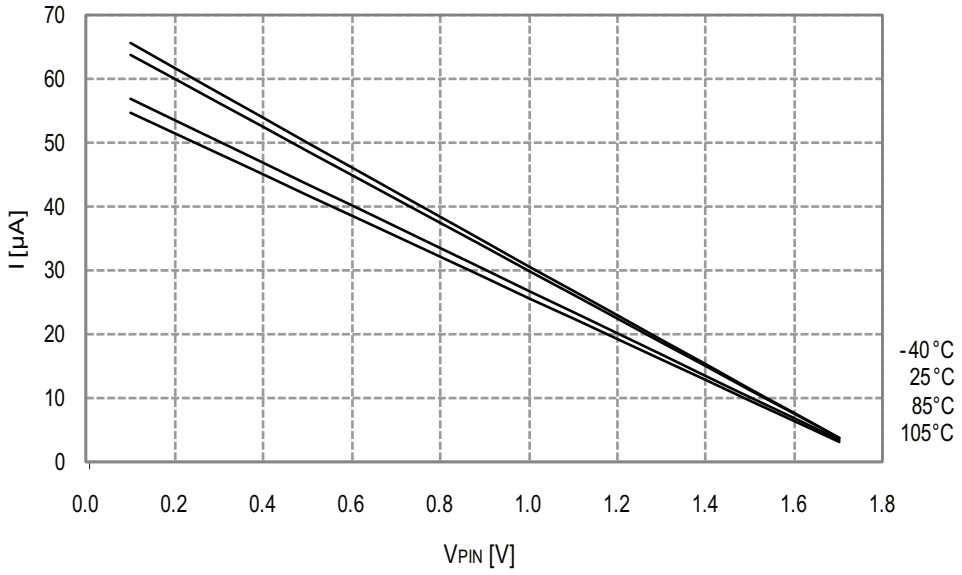


Figure 33-91. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = 3.0V

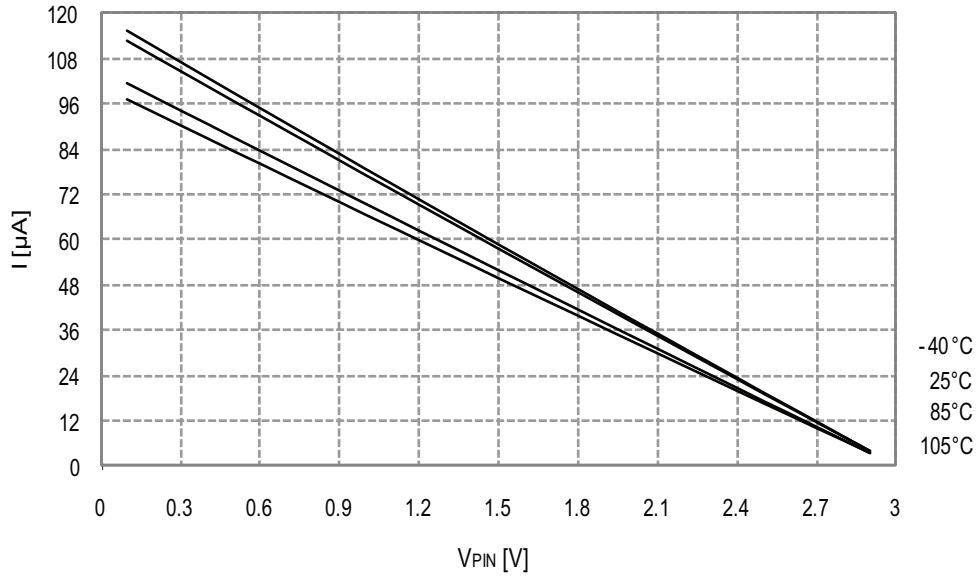
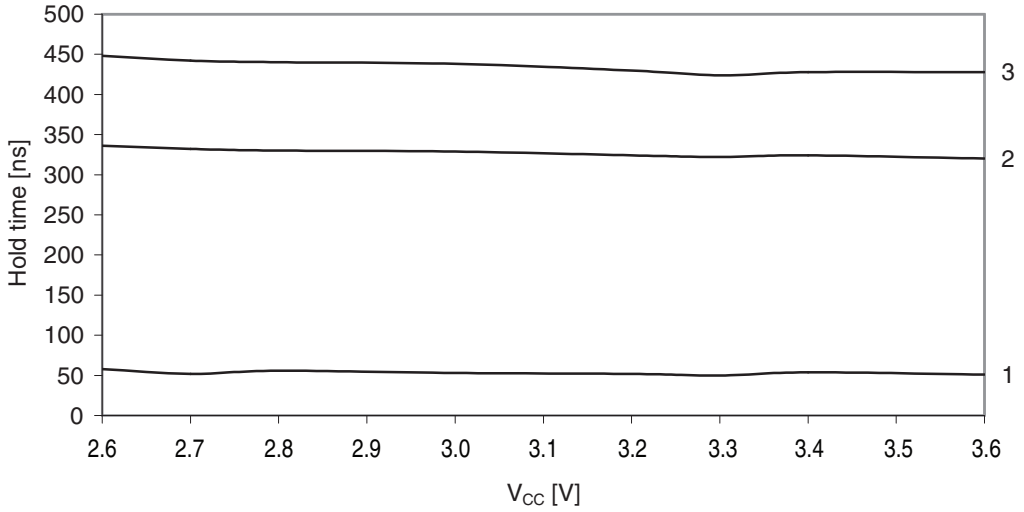
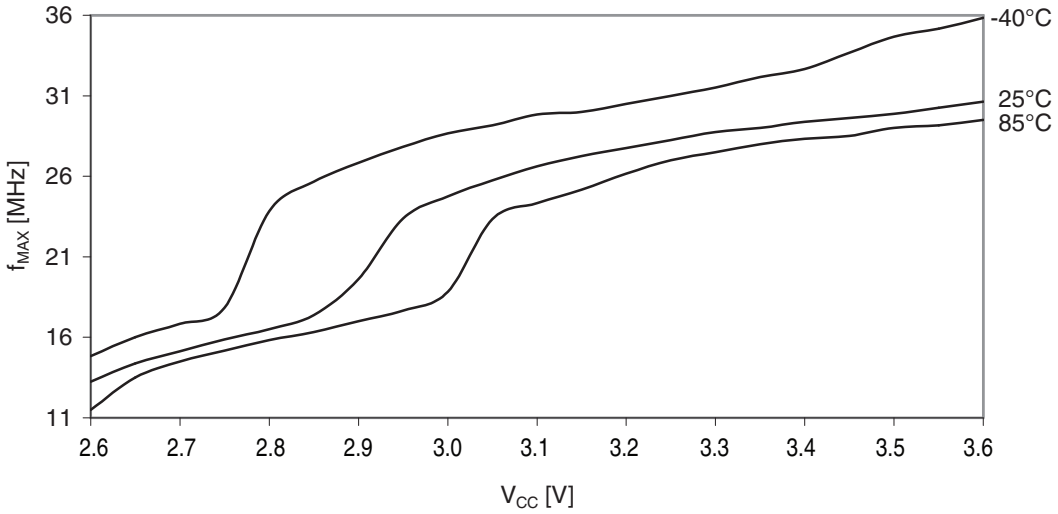


Figure 33-281.SDA Hold Time vs. Supply Voltage



33.4.10 PDI Characteristics

Figure 33-282.Maximum PDI Frequency vs. V_{CC}



33.5.1.3 Power-down Mode Supply Current

Figure 33-297.Power-down Mode Supply Current vs. V_{CC}

All functions disabled

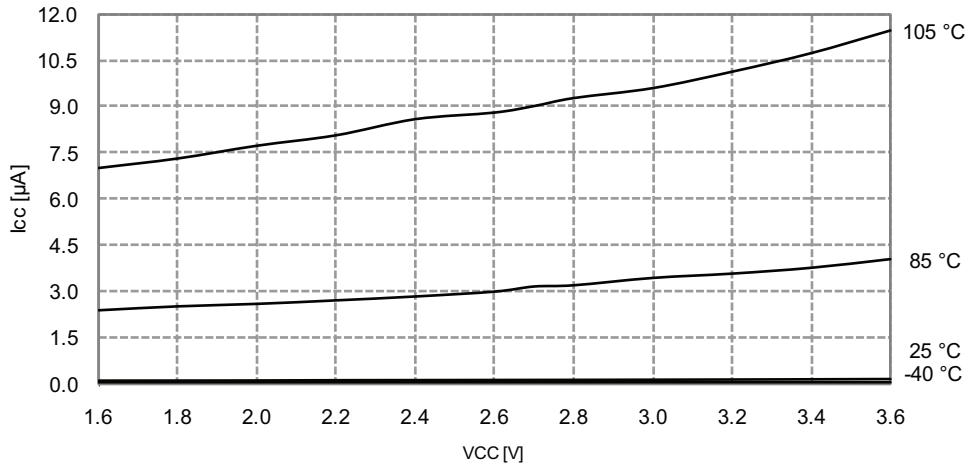


Figure 33-298.Power-down Mode Supply Current vs. V_{CC}

Watchdog and sampled BOD enabled

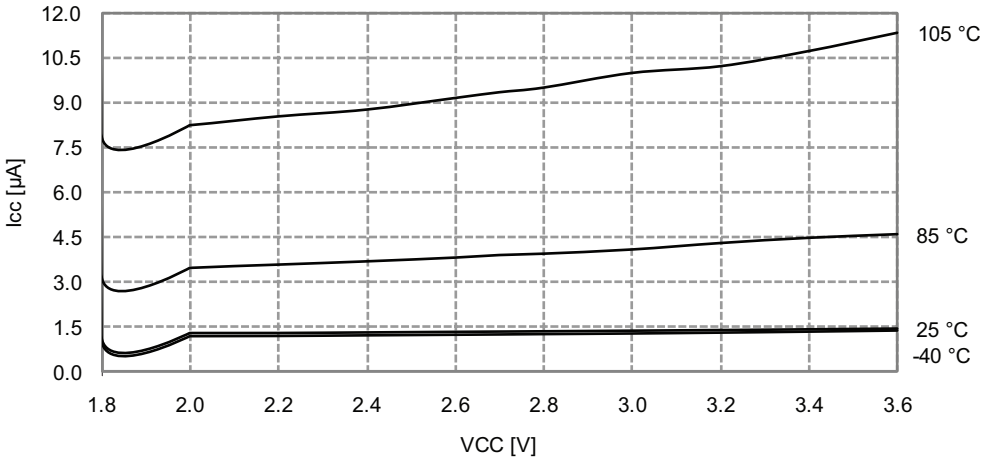


Figure 33-301.I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = 3.0V

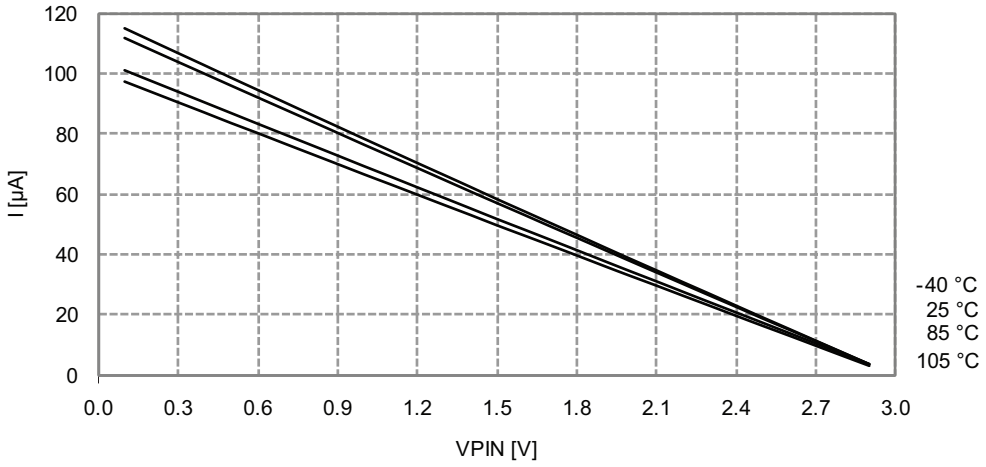
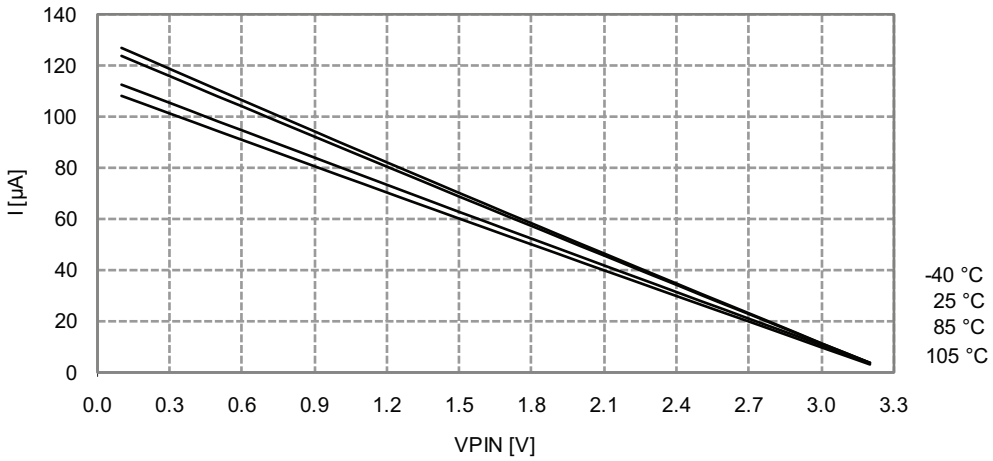


Figure 33-302.I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = 3.3V



33.5.2.2 Output Voltage vs. Sink/Source Current

Figure 33-303.I/O Pin Output Voltage vs. Source Current

V_{CC} = *1.8V*

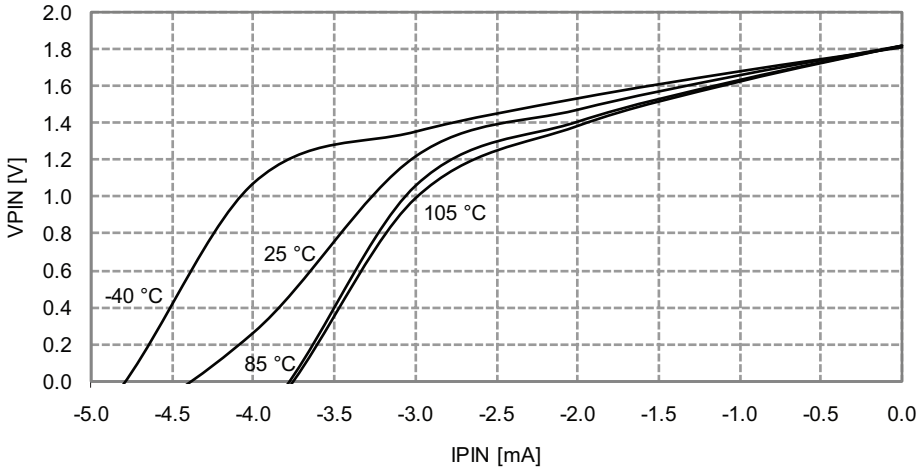
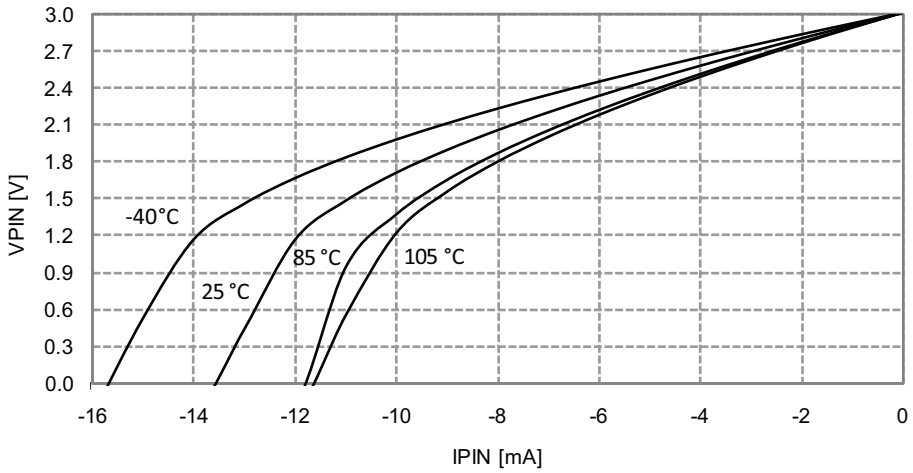


Figure 33-304.I/O Pin Output Voltage vs. Source Current

V_{CC} = *3.0V*



33.6.2.2 Output Voltage vs. Sink/Source Current

Figure 33-373.I/O Pin Output Voltage vs. Source Current

V_{CC} = *1.8V*

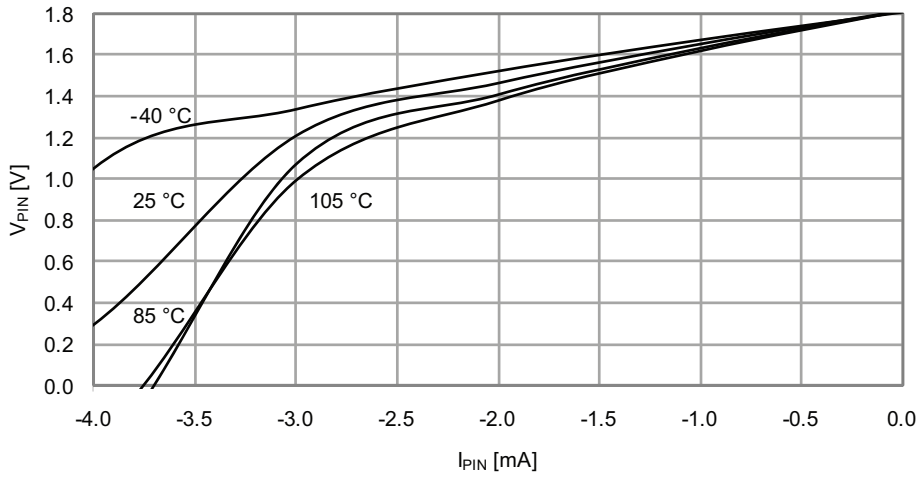
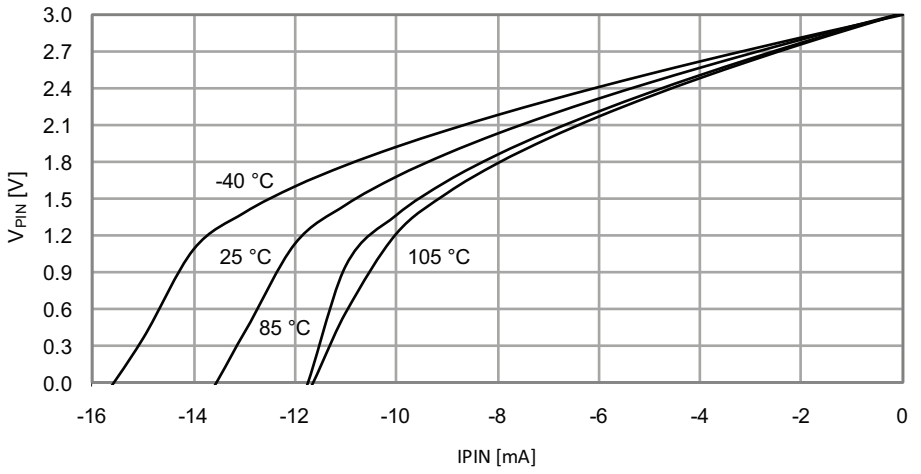


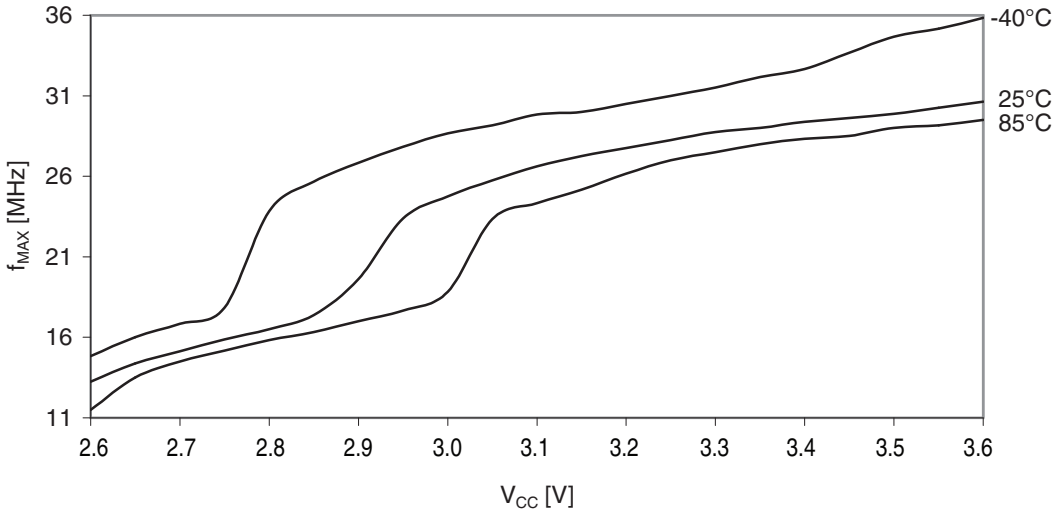
Figure 33-374.I/O Pin Output Voltage vs. Source Current

V_{CC} = *3.0V*



33.6.10 PDI Characteristics

Figure 33-419. Maximum PDI Frequency vs. V_{CC}



34. Errata

34.1 Atmel ATxmega32D3

34.1.1 Rev. I

- AC system status flags are only valid if AC-system is enabled
- Sampled BOD in Active mode will cause noise when bandgap is used as reference
- Temperature sensor not calibrated

1. AC system status flags are only valid if AC-system is enabled

The status flags for the ac-output are updated even though the AC is not enabled which is invalid. Also, it is not possible to clear the AC interrupt flags without enabling either of the Analog comparators.

Problem fix/workaround

Software should clear the AC system flags once, after enabling the AC system before using the AC system status flags.

2. Sampled BOD in Active mode will cause noise when bandgap is used as reference

Using the BOD in sampled mode when the device is running in Active or Idle mode will add noise on the bandgap reference for ADC, DAC, and Analog Comparator.

Problem fix/workaround

If the bandgap is used as reference for either the ADC, DAC and Analog Comparator, the BOD must not be set in sampled mode.

3. Temperature sensor not calibrated

Temperature sensor factory calibration not implemented.

Problem fix/workaround

None.

34.1.2 Rev A - H

Not sampled.

- PORT remap functions with alternate pin locations for Timer/Counter output compare channels, USART0 and SPI, and the PORT REMAP register
- PORT RTC clock output option and the RTCOUT bit in the PORT CLKEVOUT register
- PORT remap functions with alternate pin locations for the clock and event output, and the CLKEVPIN bit in the PORT CLKEVOUT register
- TOSC alternate pin locations, and TOSCSEL bit in FUSEBYTE2
- Real Time Counter clock source options of external clock from TOSC1, and 32.768kHz from TOSC, and 32.768kHz from the 32.768kHz internal oscillator, and these configuration options in the RTCSRC bits in the Clock RTCTRL register
- PLL divide by two option, and the PLLDIV bit in the Clock PLLCTRL register
- PLL lock detection failure function and the PLLDIF and PLLFDEN bits in the Clock XOSCFAIL register
- The high drive option for external crystal and the XOSCPWR bit on the Oscillator XOSCCTRL register
- The option to enable sequential startup of the analog modules and the ANAINIT register in MCU Control memory

Problem fix/workaround

None.

25. Sampled BOD in Active mode will cause noise when bandgap is used as reference

Using the BOD in sampled mode when the device is running in Active or Idle mode will add noise on the bandgap reference for ADC, DAC and Analog Comparator.

Problem fix/workaround

If the bandgap is used as reference for either the ADC, DAC and Analog Comparator, the BOD must not be set in sampled mode.

26. Temperature sensor not calibrated

Temperature sensor factory calibration not implemented.

Problem fix/workaround

None.

27. Disabling of USART transmitter does not automatically set the TxD pin direction to input

If the USART transmitter is idle with no frames to transmit, setting TXEN to zero will not automatically set the TxD pin direction to input.

Problem fix/workaround

The TxD pin direction can be set to input using the Port DIR register. Be advised that setting the Port DIR register to input will be immediate. Ongoing transmissions will be truncated.

34.3.7 Rev. D

Not sampled.

34.3.8 Rev. C

Not sampled.

28. Disabling of USART transmitter does not automatically set the TxD pin direction to input

If the USART transmitter is idle with no frames to transmit, setting TXEN to zero will not automatically set the TxD pin direction to input.

Problem fix/workaround

The TxD pin direction can be set to input using the Port DIR register. Be advised that setting the Port DIR register to input will be immediate. Ongoing transmissions will be truncated.

34.5.9 Rev. A

Not sampled.