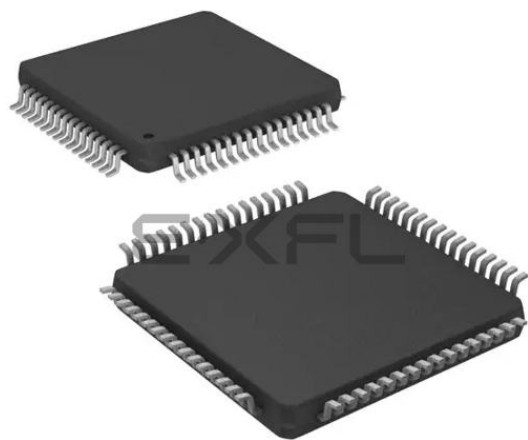




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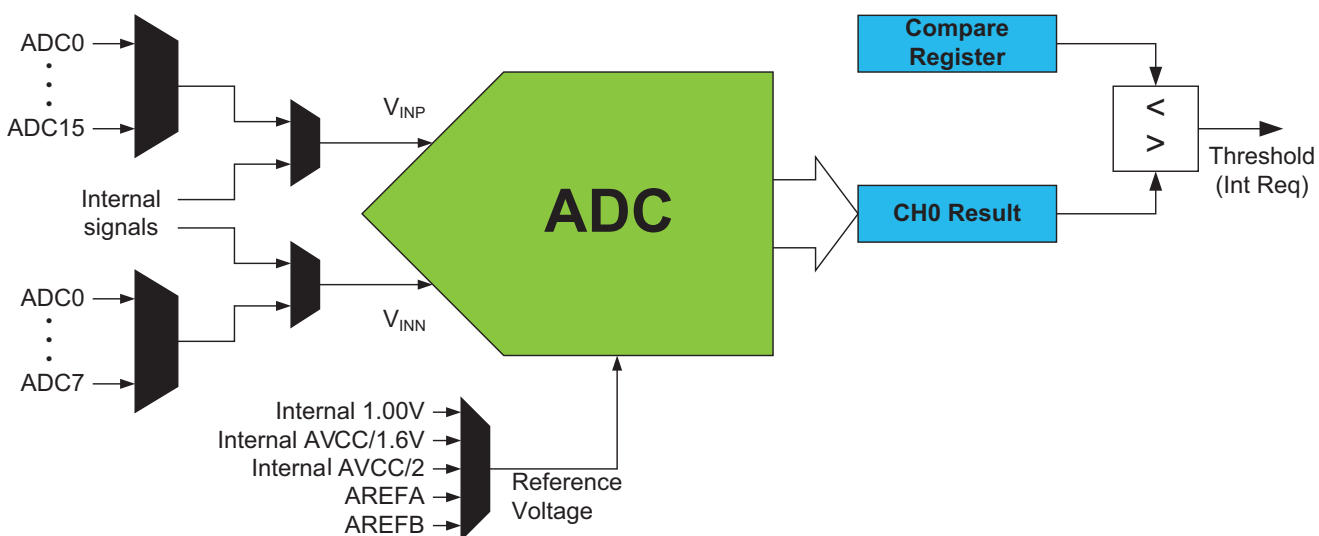
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                                                                 |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Active                                                                                                                                                          |
| Core Processor             | AVR                                                                                                                                                             |
| Core Size                  | 8/16-Bit                                                                                                                                                        |
| Speed                      | 32MHz                                                                                                                                                           |
| Connectivity               | I <sup>2</sup> C, IrDA, SPI, UART/USART                                                                                                                         |
| Peripherals                | Brown-out Detect/Reset, POR, PWM, WDT                                                                                                                           |
| Number of I/O              | 50                                                                                                                                                              |
| Program Memory Size        | 32KB (16K x 16)                                                                                                                                                 |
| Program Memory Type        | FLASH                                                                                                                                                           |
| EEPROM Size                | 1K x 8                                                                                                                                                          |
| RAM Size                   | 4K x 8                                                                                                                                                          |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 3.6V                                                                                                                                                     |
| Data Converters            | A/D 16x12b                                                                                                                                                      |
| Oscillator Type            | Internal                                                                                                                                                        |
| Operating Temperature      | -40°C ~ 105°C (TA)                                                                                                                                              |
| Mounting Type              | Surface Mount                                                                                                                                                   |
| Package / Case             | 64-TQFP                                                                                                                                                         |
| Supplier Device Package    | 64-TQFP (14x14)                                                                                                                                                 |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/microchip-technology/atxmega32d3-an">https://www.e-xfl.com/product-detail/microchip-technology/atxmega32d3-an</a> |

**Figure 25-1. ADC Overview**



The ADC may be configured for 8- or 12-bit result, reducing the minimum conversion time (propagation delay) from 3.35 $\mu$ s for 12-bit to 2.3 $\mu$ s for 8-bit result.

ADC conversion results are provided left- or right adjusted with optional '1' or '0' padding. This eases calculation when the result is represented as a signed integer (signed 16-bit number).

PORTA has one ADC. Notation of this peripheral is ADCA.

### 32.1.11 Power-on Reset Characteristics

**Table 32-16. Power-on Reset Characteristics**

| Symbol                    | Parameter                              | Condition                         | Min. | Typ. | Max. | Units |
|---------------------------|----------------------------------------|-----------------------------------|------|------|------|-------|
| $V_{POT-}$ <sup>(1)</sup> | POR threshold voltage falling $V_{CC}$ | $V_{CC}$ falls faster than 1V/ms  | 0.4  | 1.0  |      | V     |
|                           |                                        | $V_{CC}$ falls at 1V/ms or slower | 0.8  | 1.3  |      |       |
| $V_{POT+}$                | POR threshold voltage rising $V_{CC}$  |                                   |      | 1.3  | 1.59 |       |

Note: 1.  $V_{POT-}$  values are only valid when BOD is disabled. When BOD is enabled  $V_{POT-} = V_{POT+}$ .

### 32.1.12 Flash and EEPROM Memory Characteristics

**Table 32-17. Endurance and Data Retention**

| Symbol | Parameter | Condition          |       | Min. | Typ. | Max. | Units |
|--------|-----------|--------------------|-------|------|------|------|-------|
|        | Flash     | Write/Erase cycles | 25°C  | 10K  |      |      | Cycle |
|        |           |                    | 85°C  | 10K  |      |      |       |
|        |           |                    | 105°C | 2K   |      |      |       |
|        |           | Data retention     | 25°C  | 100  |      |      | Year  |
|        |           |                    | 85°C  | 25   |      |      |       |
|        |           |                    | 105°C | 10   |      |      |       |
|        | EEPROM    | Write/Erase cycles | 25°C  | 100K |      |      | Cycle |
|        |           |                    | 85°C  | 100K |      |      |       |
|        |           |                    | 105°C | 30K  |      |      |       |
|        |           | Data retention     | 25°C  | 100  |      |      | Year  |
|        |           |                    | 85°C  | 25   |      |      |       |
|        |           |                    | 105°C | 10   |      |      |       |

**Table 32-18. Programming Time**

| Symbol | Parameter                 | Condition                   |  | Min. | Typ. <sup>(1)</sup> | Max. | Units |
|--------|---------------------------|-----------------------------|--|------|---------------------|------|-------|
|        | Chip erase <sup>(2)</sup> | 32KB Flash, EEPROM          |  |      | 50                  |      | ms    |
|        | Application erase         | Section erase               |  |      | 6                   |      |       |
|        | Flash                     | Page erase                  |  |      | 4                   |      |       |
|        |                           | Page write                  |  |      | 4                   |      |       |
|        |                           | Atomic page erase and write |  |      | 8                   |      |       |
|        | EEPROM                    | Page erase                  |  |      | 4                   |      |       |
|        |                           | Page write                  |  |      | 4                   |      |       |
|        |                           | Atomic page erase and write |  |      | 8                   |      |       |

Notes: 1. Programming is timed from the 2MHz internal oscillator.  
2. EEPROM is not erased if the EESAVE fuse is programmed.

### 32.2.3 Current Consumption

**Table 32-33. Current Consumption for Active Mode and Sleep Modes**

| Symbol          | Parameter                                   | Condition                                                 | Min.                   | Typ. | Max. | Units |
|-----------------|---------------------------------------------|-----------------------------------------------------------|------------------------|------|------|-------|
| I <sub>CC</sub> | Active power consumption <sup>(1)</sup>     | 32kHz, Ext. Clk                                           | V <sub>CC</sub> = 1.8V | 50   |      | μA    |
|                 |                                             |                                                           | V <sub>CC</sub> = 3.0V | 130  |      |       |
|                 |                                             | 1MHz, Ext. Clk                                            | V <sub>CC</sub> = 1.8V | 215  |      |       |
|                 |                                             |                                                           | V <sub>CC</sub> = 3.0V | 475  |      |       |
|                 |                                             | 2MHz, Ext. Clk                                            | V <sub>CC</sub> = 1.8V | 445  | 600  | mA    |
|                 |                                             |                                                           | V <sub>CC</sub> = 3.0V | 0.95 | 1.5  |       |
|                 | Idle power consumption <sup>(1)</sup>       | 32kHz, Ext. Clk                                           | V <sub>CC</sub> = 1.8V | 2.8  |      | μA    |
|                 |                                             |                                                           | V <sub>CC</sub> = 3.0V | 3    |      |       |
|                 |                                             | 1MHz, Ext. Clk                                            | V <sub>CC</sub> = 1.8V | 46   |      |       |
|                 |                                             |                                                           | V <sub>CC</sub> = 3.0V | 92   |      |       |
|                 |                                             | 2MHz, Ext. Clk                                            | V <sub>CC</sub> = 1.8V | 93   | 225  | mA    |
|                 |                                             |                                                           | V <sub>CC</sub> = 3.0V | 184  | 350  |       |
|                 | Power-down power consumption                | T = 25°C                                                  | V <sub>CC</sub> = 3.0V | 0.07 | 1.0  | μA    |
|                 |                                             |                                                           |                        | 1.3  | 5.0  |       |
|                 |                                             |                                                           |                        | 4.0  | 8.0  |       |
|                 |                                             | WDT and sampled BOD enabled, T = 25°C                     | V <sub>CC</sub> = 3.0V | 1.3  | 2.0  |       |
|                 |                                             | WDT and sampled BOD enabled, T = 85°C                     |                        | 2.6  | 6.0  |       |
|                 |                                             | WDT and sampled BOD enabled, T = 105°C                    |                        | 5.0  | 10   |       |
|                 | Power-save power consumption <sup>(2)</sup> | RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C | V <sub>CC</sub> = 1.8V | 1.7  |      |       |
|                 |                                             |                                                           | V <sub>CC</sub> = 3.0V | 1.8  |      |       |
|                 |                                             | RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C      | V <sub>CC</sub> = 1.8V | 0.5  | 2.0  |       |
|                 |                                             |                                                           | V <sub>CC</sub> = 3.0V | 0.7  | 2.0  |       |
|                 |                                             | RTC from low power 32.768kHz TOSC, T = 25°C               | V <sub>CC</sub> = 1.8V | 0.9  | 3.0  |       |
|                 |                                             |                                                           | V <sub>CC</sub> = 3.0V | 1.2  | 3.0  |       |
|                 | Reset power consumption                     | Current through RESET pin subtracted                      | V <sub>CC</sub> = 3.0V | 120  |      |       |

- Notes:
1. All Power Reduction Registers set.
  2. Maximum limits are based on characterization, and not tested in production.



Figure 32-36. Maximum Frequency vs.  $V_{CC}$

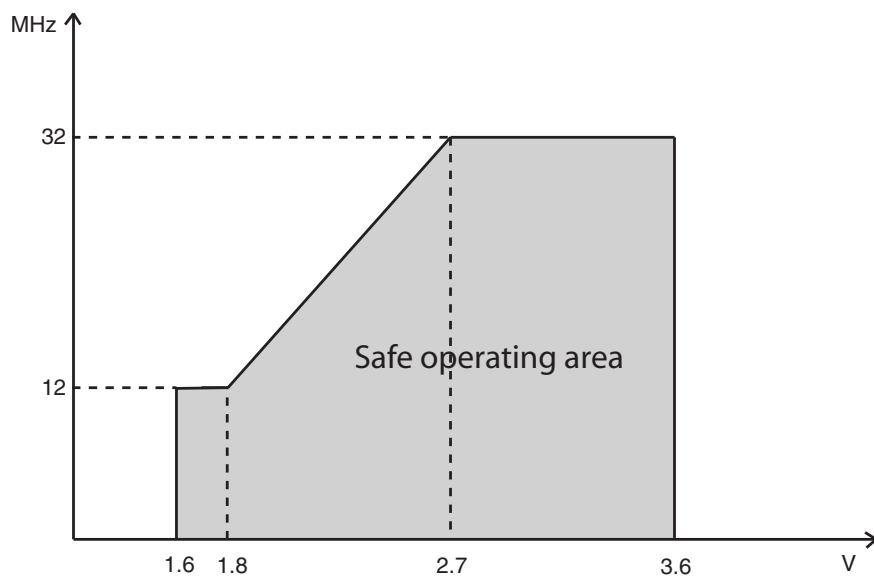


Table 32-155. Accuracy Characteristics

| Symbol             | Parameter                  | Condition <sup>(1)</sup>   |                                   | Min. | Typ. | Max. | Units |
|--------------------|----------------------------|----------------------------|-----------------------------------|------|------|------|-------|
| RES                | Resolution                 | 12-bit resolution          | Differential                      | 8    | 12   | 12   | Bits  |
|                    |                            |                            | Single ended signed               | 7    | 11   | 11   |       |
|                    |                            |                            | Single ended unsigned             | 8    | 12   | 12   |       |
| INL <sup>(2)</sup> | Integral non-linearity     | Differential mode          | 16ksps, $V_{REF} = 3V$            |      | 0.5  | 1    | lsb   |
|                    |                            |                            | 16ksps, all $V_{REF}$             |      | 0.8  | 2    |       |
|                    |                            |                            | 300ksps, $V_{REF} = 3V$           |      | 0.6  | 1    |       |
|                    |                            |                            | 300ksps, all $V_{REF}$            |      | 1    | 2    |       |
|                    |                            | Single ended unsigned mode | 16ksps, $V_{REF} = 3.0V$          |      | 0.5  | 1    |       |
|                    |                            |                            | 16ksps, all $V_{REF}$             |      | 1.3  | 2    |       |
| DNL <sup>(2)</sup> | Differential non-linearity | Differential mode          | 16ksps, $V_{REF} = 3V$            |      | 0.3  | 1    |       |
|                    |                            |                            | 16ksps, all $V_{REF}$             |      | 0.5  | 1    |       |
|                    |                            |                            | 300ksps, $V_{REF} = 3V$           |      | 0.35 | 1    |       |
|                    |                            |                            | 300ksps, all $V_{REF}$            |      | 0.5  | 1    |       |
|                    |                            | Single ended unsigned mode | 16ksps, $V_{REF} = 3.0V$          |      | 0.6  | 1    |       |
|                    |                            |                            | 16ksps, all $V_{REF}$             |      | 0.6  | 1    |       |
|                    | Offset error               | Differential mode          | 300ksps, $V_{REF} = 3V$           |      | -7   |      | mV    |
|                    |                            |                            | Temperature drift, $V_{REF} = 3V$ |      | 0.01 |      | mV/K  |
|                    |                            |                            | Operating voltage drift           |      | 0.16 |      | mV/V  |
|                    | Gain error                 | Differential mode          | External reference                |      | -5   |      | mV    |
|                    |                            |                            | $AV_{CC}/1.6$                     |      | -5   |      |       |
|                    |                            |                            | $AV_{CC}/2.0$                     |      | -6   |      |       |
|                    |                            |                            | Bandgap                           |      | ±10  |      |       |
|                    |                            |                            | Temperature drift                 |      | 0.02 |      | mV/K  |
|                    |                            |                            | Operating voltage drift           |      | 2    |      | mV/V  |
|                    | Gain error                 | Single ended unsigned mode | External reference                |      | -8   |      | mV    |
|                    |                            |                            | $AV_{CC}/1.6$                     |      | -8   |      |       |
|                    |                            |                            | $AV_{CC}/2.0$                     |      | -8   |      |       |
|                    |                            |                            | Bandgap                           |      | ±10  |      |       |
|                    |                            |                            | Temperature drift                 |      | 0.03 |      | mV/K  |
|                    |                            |                            | Operating voltage drift           |      | 2    |      | mV/V  |

- Notes:
1. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external  $V_{REF}$  is used.
  2. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

### 32.6.8 Bandgap and Internal 1.0V Reference Characteristics

**Table 32-158. Bandgap and Internal 1.0V Reference Characteristics**

| Symbol | Parameter                              | Condition                      | Min.                         | Typ. | Max. | Units |
|--------|----------------------------------------|--------------------------------|------------------------------|------|------|-------|
|        | Startup time                           | As reference for ADC           | 1 Clk <sub>PER</sub> + 2.5μs |      |      | μs    |
|        |                                        | As input voltage to ADC and AC |                              | 1.5  |      |       |
|        | Bandgap voltage                        |                                |                              | 1.1  |      | V     |
| INT1V  | Internal 1.00V reference               | T = 85°C, after calibration    | 0.99                         | 1    | 1.01 |       |
|        | Variation over voltage and temperature | Calibrated at T = 85°C         |                              | 2    |      |       |

### 32.6.9 Brownout Detection Characteristics

**Table 32-159. Brownout Detection Characteristics <sup>(1)</sup>**

| Symbol            | Parameter                           | Condition       | Min. | Typ. | Max. | Units |
|-------------------|-------------------------------------|-----------------|------|------|------|-------|
| V <sub>BOT</sub>  | BOD level 0 falling V <sub>CC</sub> |                 | 1.60 | 1.62 | 1.72 | V     |
|                   | BOD level 1 falling V <sub>CC</sub> |                 |      | 1.9  |      |       |
|                   | BOD level 2 falling V <sub>CC</sub> |                 |      | 2.0  |      |       |
|                   | BOD level 3 falling V <sub>CC</sub> |                 |      | 2.2  |      |       |
|                   | BOD level 4 falling V <sub>CC</sub> |                 |      | 2.4  |      |       |
|                   | BOD level 5 falling V <sub>CC</sub> |                 |      | 2.6  |      |       |
|                   | BOD level 6 falling V <sub>CC</sub> |                 |      | 2.8  |      |       |
|                   | BOD level 7 falling V <sub>CC</sub> |                 |      | 3.0  |      |       |
| t <sub>BOD</sub>  | Detection time                      | Continuous mode |      | 0.4  |      | μs    |
|                   |                                     | Sampled mode    |      | 1000 |      |       |
| V <sub>HYST</sub> | Hysteresis                          |                 |      | 1.0  |      | %     |

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

### 32.6.10 External Reset Characteristics

**Table 32-160. External Reset Characteristics**

| Symbol           | Parameter                  | Condition                    | Min. | Typ.                   | Max. | Units |
|------------------|----------------------------|------------------------------|------|------------------------|------|-------|
| t <sub>EXT</sub> | Minimum reset pulse width  |                              | 1000 | 90                     |      | ns    |
| V <sub>RST</sub> | Reset threshold voltage    | V <sub>CC</sub> = 2.7 - 3.6V |      | 0.45 * V <sub>CC</sub> |      | V     |
|                  |                            | V <sub>CC</sub> = 1.6 - 2.7V |      | 0.42 * V <sub>CC</sub> |      |       |
| R <sub>RST</sub> | Reset pin pull-up resistor |                              |      | 25                     |      | kΩ    |

### 32.6.13.5 Internal Phase Locked Loop (PLL) Characteristics

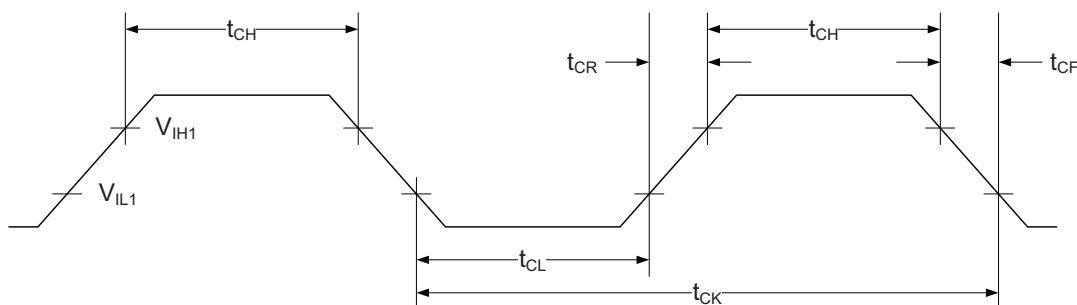
**Table 32-168. Internal PLL Characteristics**

| Symbol    | Parameter                       | Condition                                 | Min. | Typ. | Max. | Units   |
|-----------|---------------------------------|-------------------------------------------|------|------|------|---------|
| $f_{IN}$  | Input frequency                 | Output frequency must be within $f_{OUT}$ | 0.4  |      | 64   | MHz     |
| $f_{OUT}$ | Output frequency <sup>(1)</sup> | $V_{CC} = 1.6 - 1.8V$                     | 20   |      | 48   |         |
|           |                                 | $V_{CC} = 2.7 - 3.6V$                     | 20   |      | 128  |         |
|           | Start-up time                   |                                           |      | 25   |      | $\mu s$ |
|           | Re-lock time                    |                                           |      | 25   |      |         |

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

### 32.6.13.6 External Clock Characteristics

**Figure 32-38. External Clock Drive Waveform**



**Table 32-169. External Clock used as System Clock without Prescaling**

| Symbol          | Parameter                                         | Condition        | Min. | Typ. | Max. | Units |
|-----------------|---------------------------------------------------|------------------|------|------|------|-------|
| $1/t_{CK}$      | Clock Frequency <sup>(1)</sup>                    | $V_{CC} = 1.6 -$ | 0    |      | 12   | MHz   |
|                 |                                                   | $V_{CC} = 2.7 -$ | 0    |      | 32   |       |
| $t_{CK}$        | Clock Period                                      | $V_{CC} = 1.6 -$ | 83.3 |      |      | ns    |
|                 |                                                   | $V_{CC} = 2.7 -$ | 31.5 |      |      |       |
| $t_{CH}$        | Clock High Time                                   | $V_{CC} = 1.6 -$ | 30.0 |      |      |       |
|                 |                                                   | $V_{CC} = 2.7 -$ | 12.5 |      |      |       |
| $t_{CL}$        | Clock Low Time                                    | $V_{CC} = 1.6 -$ | 30.0 |      |      |       |
|                 |                                                   | $V_{CC} = 2.7 -$ | 12.5 |      |      |       |
| $t_{CR}$        | Rise Time (for maximum frequency)                 | $V_{CC} = 1.6 -$ |      |      | 10   |       |
|                 |                                                   | $V_{CC} = 2.7 -$ |      |      | 3    |       |
| $t_{CF}$        | Fall Time (for maximum frequency)                 | $V_{CC} = 1.6 -$ |      |      | 10   |       |
|                 |                                                   | $V_{CC} = 2.7 -$ |      |      | 3    |       |
| $\Delta t_{CK}$ | Change in period from one clock cycle to the next |                  |      |      | 10   | %     |

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

**Table 32-170. External Clock with Prescaler <sup>(1)</sup> for System Clock**

| Symbol            | Parameter                                         | Condition                    | Min. | Typ. | Max. | Units |
|-------------------|---------------------------------------------------|------------------------------|------|------|------|-------|
| 1/t <sub>CK</sub> | Clock Frequency <sup>(2)</sup>                    | V <sub>CC</sub> = 1.6 - 1.8V | 0    |      | 90   | MHz   |
|                   |                                                   | V <sub>CC</sub> = 2.7 - 3.6V | 0    |      | 142  |       |
| t <sub>CK</sub>   | Clock Period                                      | V <sub>CC</sub> = 1.6 - 1.8V | 11   |      |      | ns    |
|                   |                                                   | V <sub>CC</sub> = 2.7 - 3.6V | 7    |      |      |       |
| t <sub>CH</sub>   | Clock High Time                                   | V <sub>CC</sub> = 1.6 - 1.8V | 4.5  |      |      |       |
|                   |                                                   | V <sub>CC</sub> = 2.7 - 3.6V | 2.4  |      |      |       |
| t <sub>CL</sub>   | Clock Low Time                                    | V <sub>CC</sub> = 1.6 - 1.8V | 4.5  |      |      |       |
|                   |                                                   | V <sub>CC</sub> = 2.7 - 3.6V | 2.4  |      |      |       |
| t <sub>CR</sub>   | Rise Time (for maximum frequency)                 | V <sub>CC</sub> = 1.6 - 1.8V |      |      | 1.5  |       |
|                   |                                                   | V <sub>CC</sub> = 2.7 - 3.6V |      |      | 1.0  |       |
| t <sub>CF</sub>   | Fall Time (for maximum frequency)                 | V <sub>CC</sub> = 1.6 - 1.8V |      |      | 1.5  |       |
|                   |                                                   | V <sub>CC</sub> = 2.7 - 3.6V |      |      | 1.0  |       |
| Δt <sub>CK</sub>  | Change in period from one clock cycle to the next |                              |      |      | 10   | %     |

- Notes:
1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
  2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

### 32.6.13.7 External 16MHz Crystal Oscillator and XOSC Characteristics

**Table 32-171. External 16MHz Crystal Oscillator and XOSC Characteristics**

| Symbol | Parameter             | Condition | Min.                | Typ.  | Max. | Units |
|--------|-----------------------|-----------|---------------------|-------|------|-------|
|        | Cycle to cycle jitter | XOSCPWR=0 | FRQRANGE=0          | 0     |      | ns    |
|        |                       |           | FRQRANGE=1, 2, or 3 | 0     |      |       |
|        |                       | XOSCPWR=1 |                     | 0     |      |       |
|        | Long term jitter      | XOSCPWR=0 | FRQRANGE=0          | 0     |      | ns    |
|        |                       |           | FRQRANGE=1, 2, or 3 | 0     |      |       |
|        |                       | XOSCPWR=1 |                     | 0     |      |       |
|        | Frequency error       | XOSCPWR=0 | FRQRANGE=0          | 0.03  |      | %     |
|        |                       |           | FRQRANGE=1          | 0.03  |      |       |
|        |                       |           | FRQRANGE=2 or 3     | 0.03  |      |       |
|        |                       | XOSCPWR=1 |                     | 0.003 |      |       |
|        | Duty cycle            | XOSCPWR=0 | FRQRANGE=0          | 50    |      | %     |
|        |                       |           | FRQRANGE=1          | 50    |      |       |
|        |                       |           | FRQRANGE=2 or 3     | 50    |      |       |
|        |                       | XOSCPWR=1 |                     | 50    |      |       |

### 33.2.7 External Reset Characteristics

Figure 33-120. Minimum Reset Pin Pulse Width vs.  $V_{CC}$

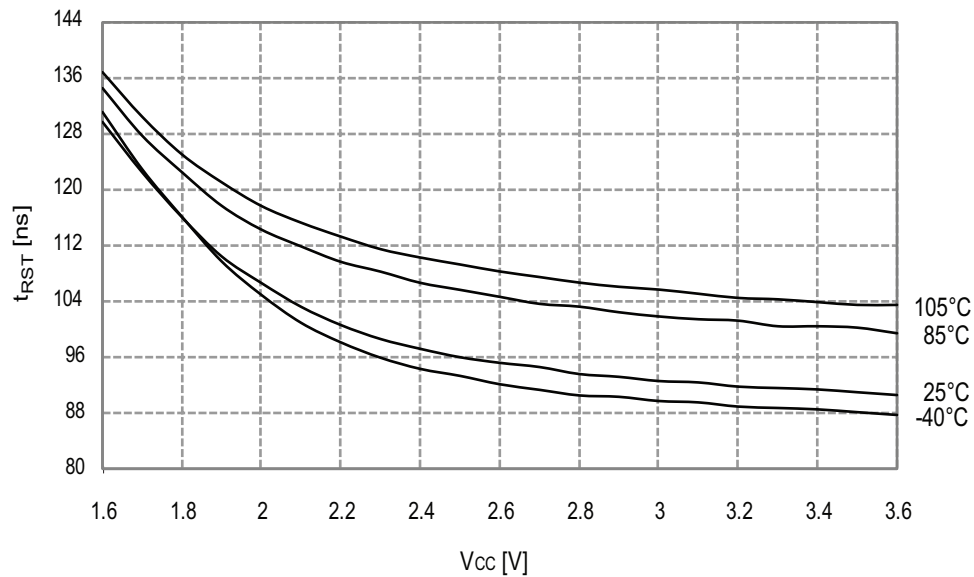
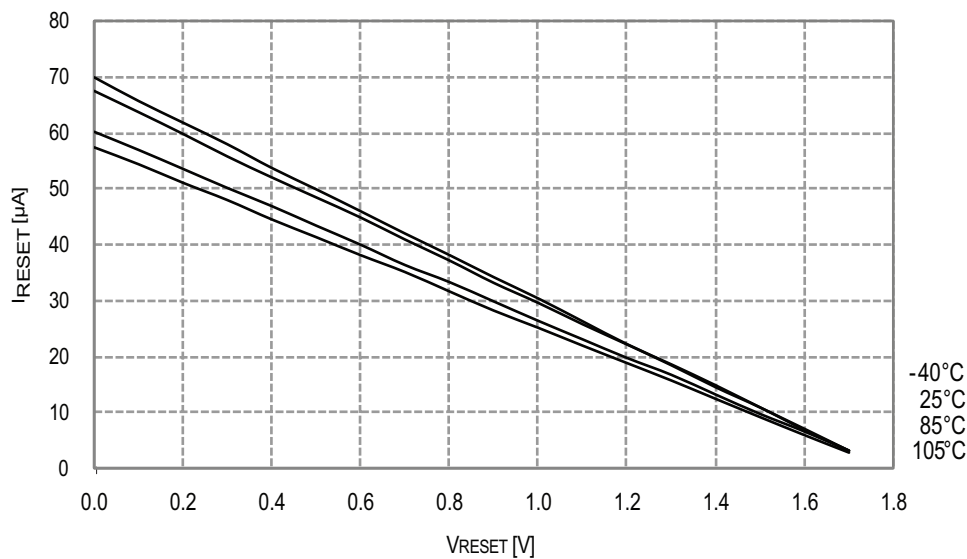
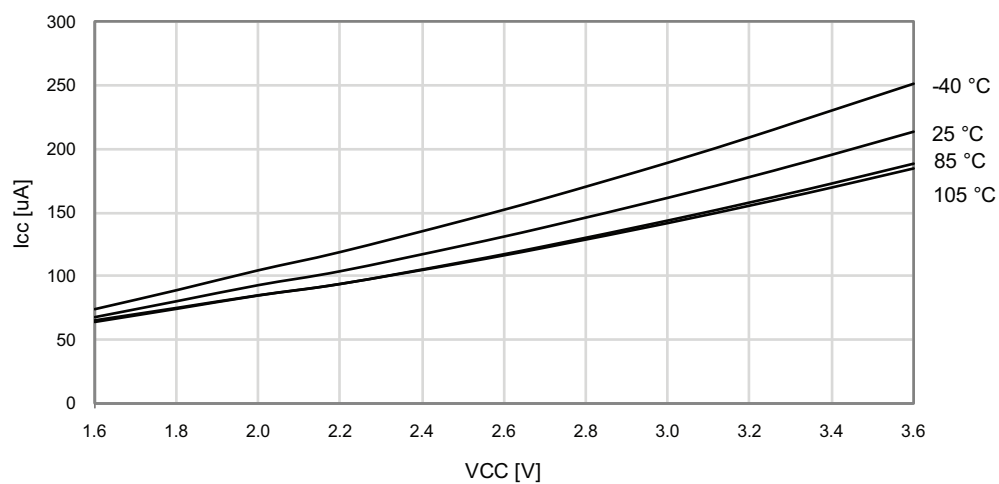


Figure 33-121. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage  
 $V_{CC} = 1.8V$



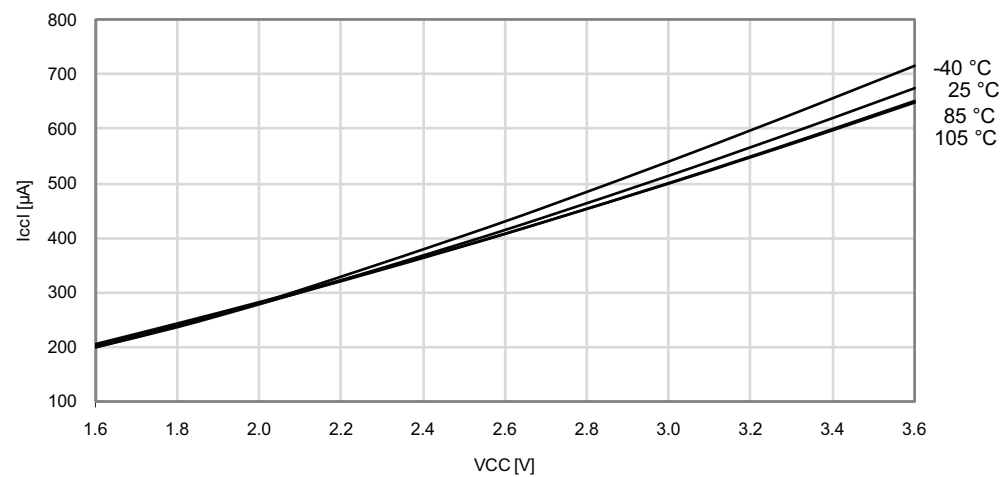
**Figure 33-145. Active Mode Supply Current vs.  $V_{CC}$**

$f_{SYS} = 32.768\text{kHz}$  internal oscillator

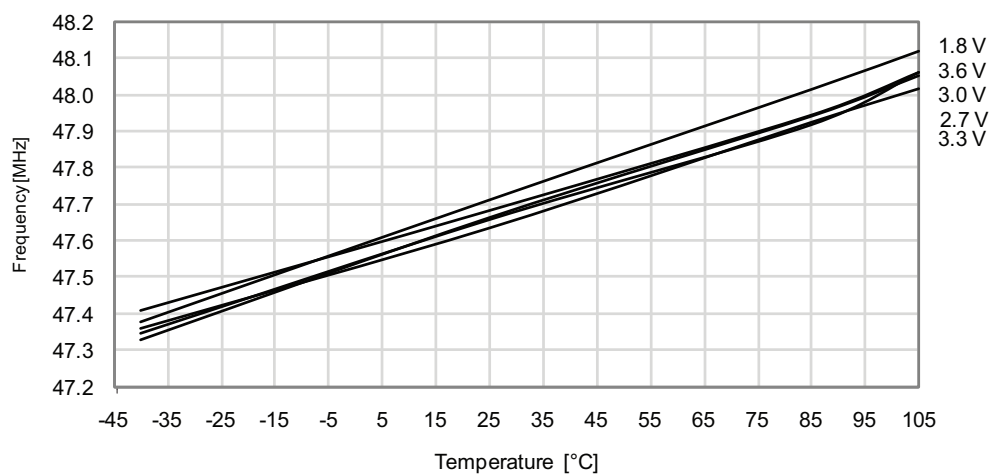


**Figure 33-146. Active Mode Supply Current vs.  $V_{CC}$**

$f_{SYS} = 1\text{MHz}$  external clock

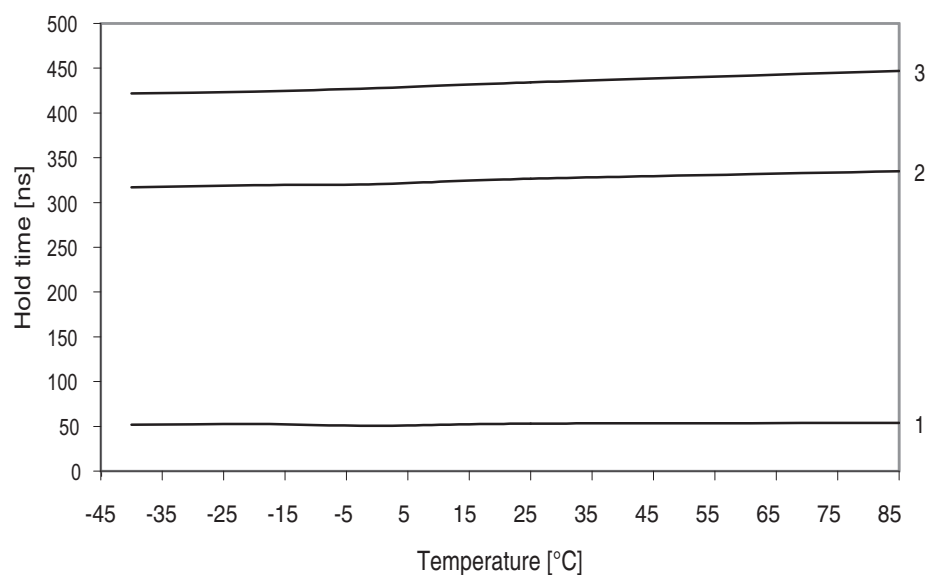


**Figure 33-209. 48MHz Internal Oscillator Frequency vs. Temperature**  
*DPLL enabled, from the 32.768kHz internal oscillator*



### 33.3.9 Two-Wire Interface Characteristics

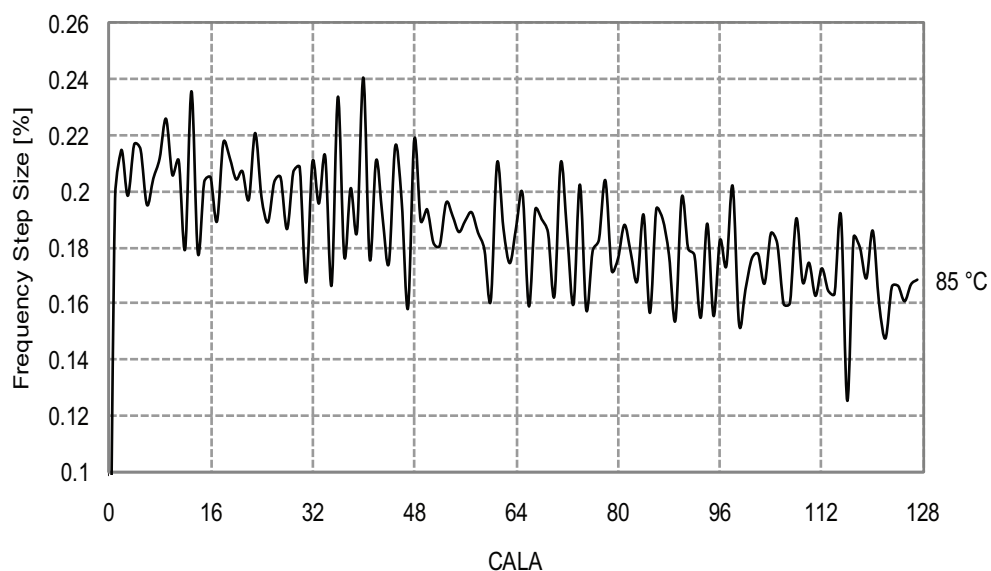
**Figure 33-210. SDA Hold Time vs. Temperature**





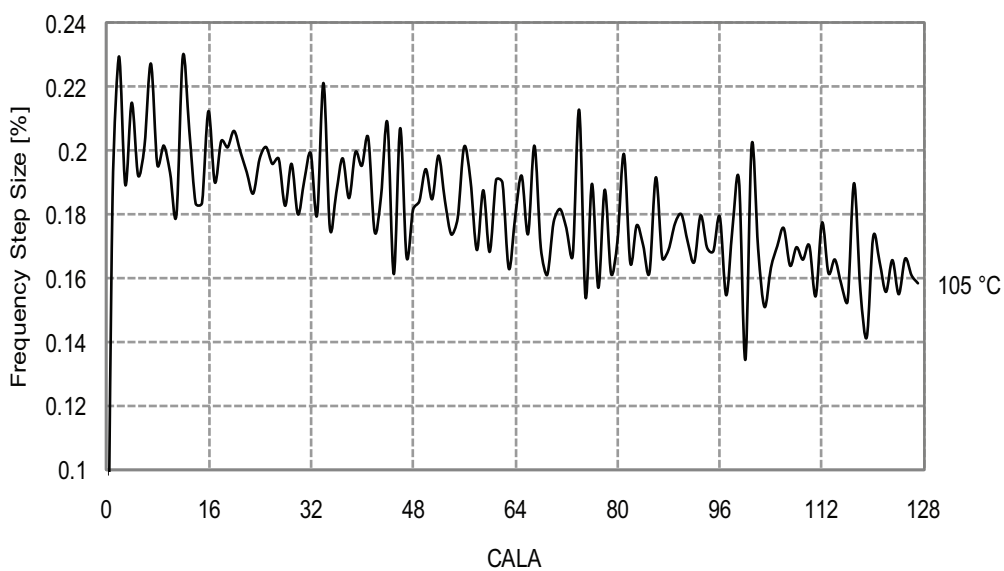
**Figure 33-345. 32MHz Internal Oscillator CALA Calibration Step Size**

$T = 85^{\circ}\text{C}$ ,  $V_{CC} = 3.0\text{V}$



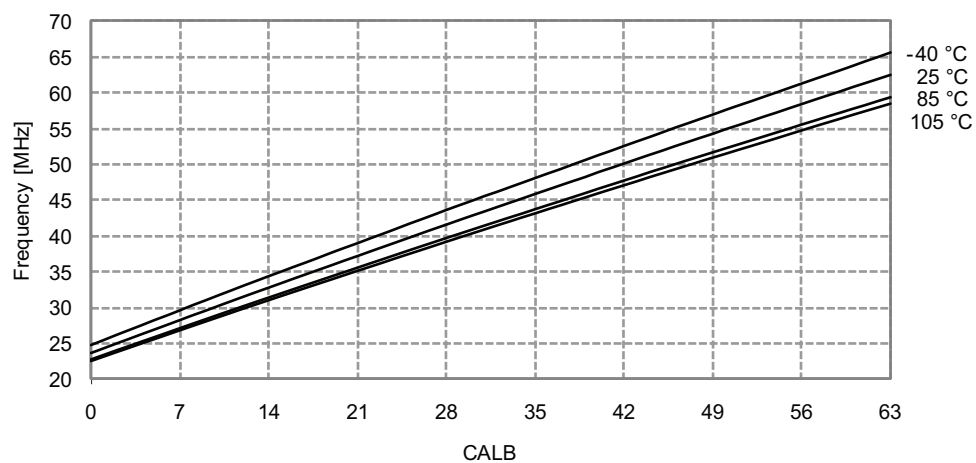
**Figure 33-346. 32MHz Internal Oscillator CALA Calibration Step Size**

$T = 105^{\circ}\text{C}$ ,  $V_{CC} = 3.0\text{V}$



**Figure 33-347. 32MHz Internal Oscillator Frequency vs. CALB Calibration Value**

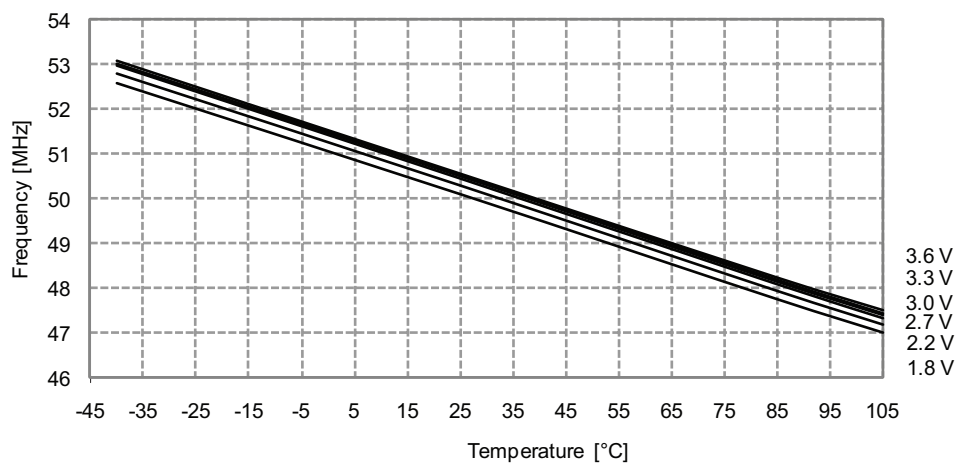
$V_{CC} = 3.0V$



### 33.5.8.5 32MHz Internal Oscillator Calibrated to 48MHz

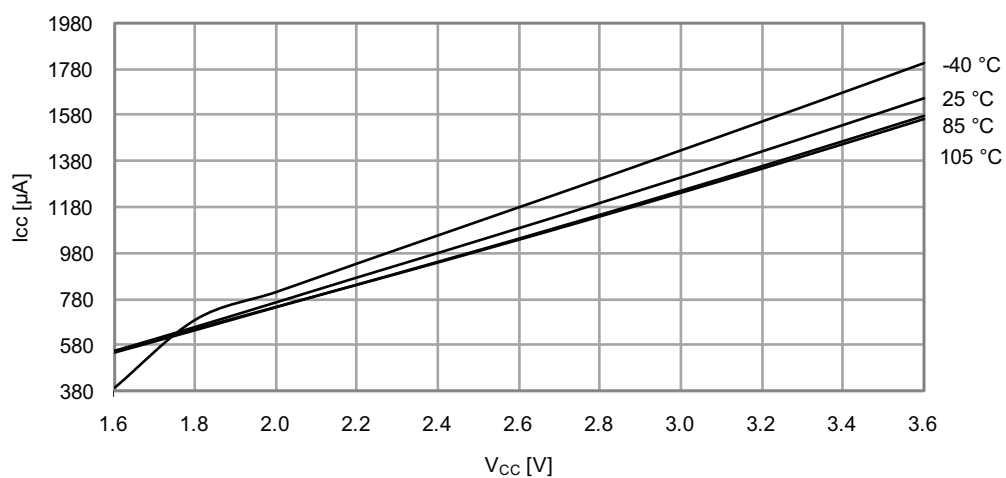
**Figure 33-348. 48MHz Internal Oscillator Frequency vs. Temperature**

*DFLL disabled*



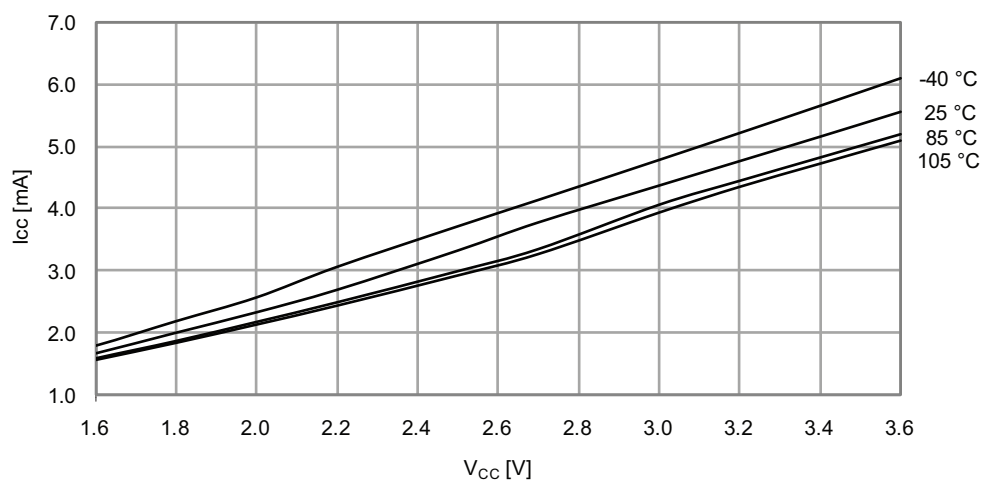
**Figure 33-357. Active Mode Supply Current vs.  $V_{CC}$**

$f_{SYS} = 2\text{MHz}$  internal oscillator



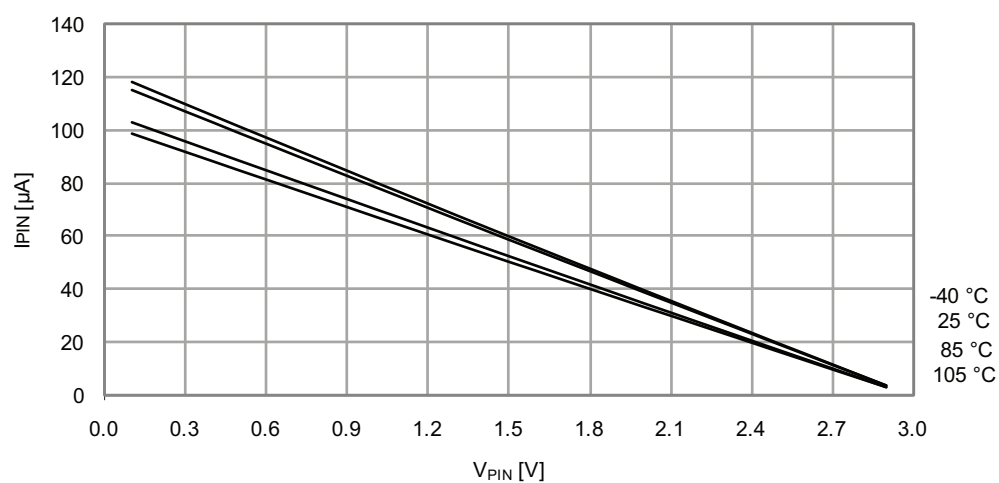
**Figure 33-358. Active Mode Supply Current vs.  $V_{CC}$**

$f_{SYS} = 32\text{MHz}$  internal oscillator prescaled to 8MHz



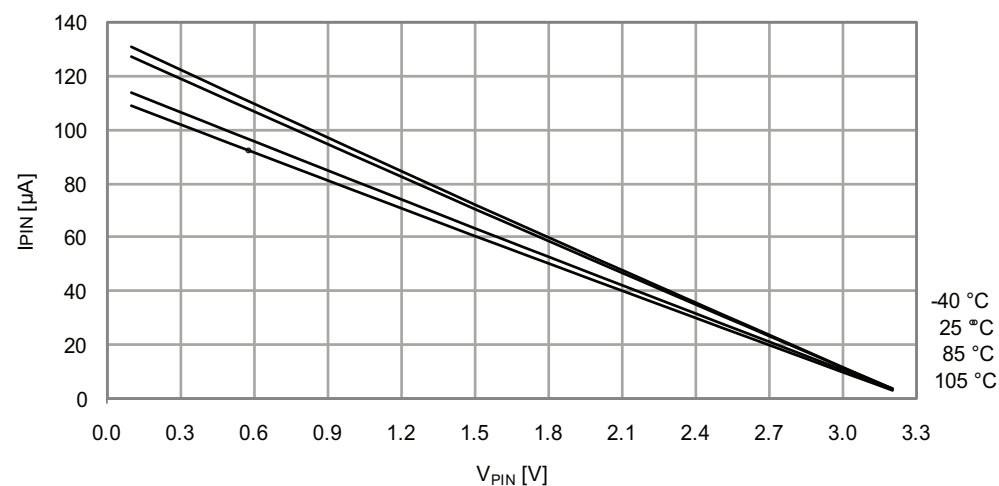
**Figure 33-371. I/O Pin Pull-up Resistor Current vs. Input Voltage**

$V_{CC} = 3.0V$



**Figure 33-372. I/O Pin Pull-up Resistor Current vs. Input Voltage**

$V_{CC} = 3.3V$



## Problem fix/workaround

Table 34-1. Configure PWM and CWCM According to this Table:

| PGM | CWCM | Description           |
|-----|------|-----------------------|
| 0   | 0    | PGM and CWCM disabled |
| 0   | 1    | PGM enabled           |
| 1   | 0    | PGM and CWCM enabled  |
| 1   | 1    | PGM enabled           |

### 11. PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

#### Problem fix/workaround

Do a write to any AWeX I/O register to re-enable the output.

### 12. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the  $V_{CC}$  voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until  $V_{CC}$  is above the programmed BOD level even if the BOD is disabled.

#### Problem fix/workaround

Do not set the BOD level higher than  $V_{CC}$  even if the BOD is not used.

### 13. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

#### Problem fix/workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELoad) is set. Do not write NVM DATA0 when EELoad is set.

### 14. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

#### Problem fix/workaround

None.

### 15. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

#### Problem fix/workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (that is, connect positive input to the negative AC input and vice versa), or use an external inverter to change polarity of Analog Comparator output.

|   |     |       |     |    |
|---|-----|-------|-----|----|
| — | 1×  | gain: | 2.4 | V  |
| — | 2×  | gain: | 1.2 | V  |
| — | 4×  | gain: | 0.6 | V  |
| — | 8×  | gain: | 300 | mV |
| — | 16× | gain: | 150 | mV |
| — | 32× | gain: | 75  | mV |
| — | 64× | gain: | 38  | mV |

#### **Problem fix/workaround**

Keep the amplified voltage output from the ADC gain stage below 2.4V in order to get a correct result, or keep ADC voltage reference below 2.4V.

### **6. ADC Event on compare match non-functional**

ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

#### **Problem fix/workaround**

Enable and use interrupt on compare match when using the compare function.

### **7. ADC propagation delay is not correct when 8× – 64× gain is used**

The propagation delay will increase by only one ADC clock cycle for all gain settings.

#### **Problem fix/workaround**

None.

### **8. Bandgap measurement with the ADC is non-functional when $V_{CC}$ is below 2.7V**

The ADC can not be used to do bandgap measurements when  $V_{CC}$  is below 2.7V.

#### **Problem fix/workaround**

None.

### **9. Accuracy lost on first three samples after switching input to ADC gain stage**

Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

#### **Problem fix/workaround**

Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

### **10. Configuration of PGM and CWCM not as described in XMEGA D Manual**

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

## Problem fix/workaround

**Table 34-6. Configure PWM and CWCM According to this Table:**

| PGM | CWCM | Description           |
|-----|------|-----------------------|
| 0   | 0    | PGM and CWCM disabled |
| 0   | 1    | PGM enabled           |
| 1   | 0    | PGM and CWCM enabled  |
| 1   | 1    | PGM enabled           |

### 11. PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

#### Problem fix/workaround

Do a write to any AWeX I/O register to re-enable the output.

### 12. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the  $V_{CC}$  voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until  $V_{CC}$  is above the programmed BOD level even if the BOD is disabled.

#### Problem fix/workaround

Do not set the BOD level higher than  $V_{CC}$  even if the BOD is not used.

### 13. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

#### Problem fix/workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELoad) is set. Do not write NVM DATA0 when EELoad is set.

### 14. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

#### Problem fix/workaround

None.

### 15. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

#### Problem fix/workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (that is, connect positive input to the negative AC input and vice versa), or use an external inverter to change polarity of Analog Comparator output.

## 25. Non available functions and options

The below function and options are not available. Writing to any registers or fuse to try and enable or configure these functions or options will have no effect, and will be as writing to a reserved address location.

- TWIE, the TWI module on PORTE
- TWI SDAHOLD option in the TWI CTRL register is one bit
- CRC generator module
- ADC 1/2× gain option, and this configuration option in the GAIN bits in the ADC Channel CTRL register
- ADC VCC/2 reference option and this configuration option in the REFSEL bits on the ADC REFCTRL register
- ADC option to use internal Gnd as negative input in differential measurements and this configuration option in the MUXNEG bits in the ADC Channel MUXCTRL register
- ADC channel scan and the ADC SCAN register
- ADC current limitation option, and the CURRLIMIT bits in the ADC CTRLB register
- ADC impedance mode selection for the gain stage, and the IMPMODE bit in the ADC CTRLB register
- Timer/Counter 2 and the SPLITMODE configuration option in the BYTEM bits in the Timer/Counter 0 CTRL register
- Analog Comparator (AC) current output option, and the AC CURRCTRL and CURRCALIB registers
- PORT remap functions with alternate pin locations for Timer/Counter output compare channels, USART0 and SPI, and the PORT REMAP register
- PORT RTC clock output option and the RTCOUT bit in the PORT CLKEVOUT register
- PORT remap functions with alternate pin locations for the clock and event output, and the CLKEVPIN bit in the PORT CLKEVOUT register
- TOSC alternate pin locations, and TOSCSEL bit in FUSEBYTE2
- Real Time Counter clock source options of external clock from TOSC1, and 32.768kHz from TOSC, and 32.768kHz from the 32.768kHz internal oscillator, and these configuration options in the RTCSRC bits in the Clock RTCTRL register
- PLL divide by two option, and the PLLDIV bit in the Clock PLLCTRL register
- PLL lock detection failure function and the PLLDIF and PLLFDEN bits in the Clock XOSCFAIL register
- The high drive option for external crystal and the XOSCPWR bit on the Oscillator XOSCCTRL register
- The option to enable sequential startup of the analog modules and the ANAINIT register in MCU Control memory

### Problem fix/workaround

None.

## 26. Sampled BOD in Active mode will cause noise when bandgap is used as reference

Using the BOD in sampled mode when the device is running in Active or Idle mode will add noise on the bandgap reference for ADC, DAC and Analog Comparator.

### Problem fix/workaround

If the bandgap is used as reference for either the ADC, DAC and Analog Comparator, the BOD must not be set in sampled mode.

## 27. Temperature sensor not calibrated

Temperature sensor factory calibration not implemented.

### Problem fix/workaround

None.



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