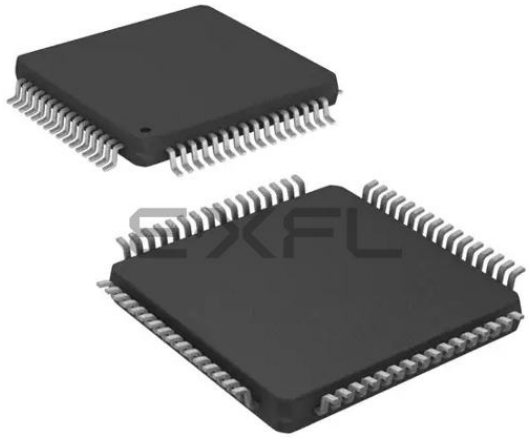

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32d3-anr

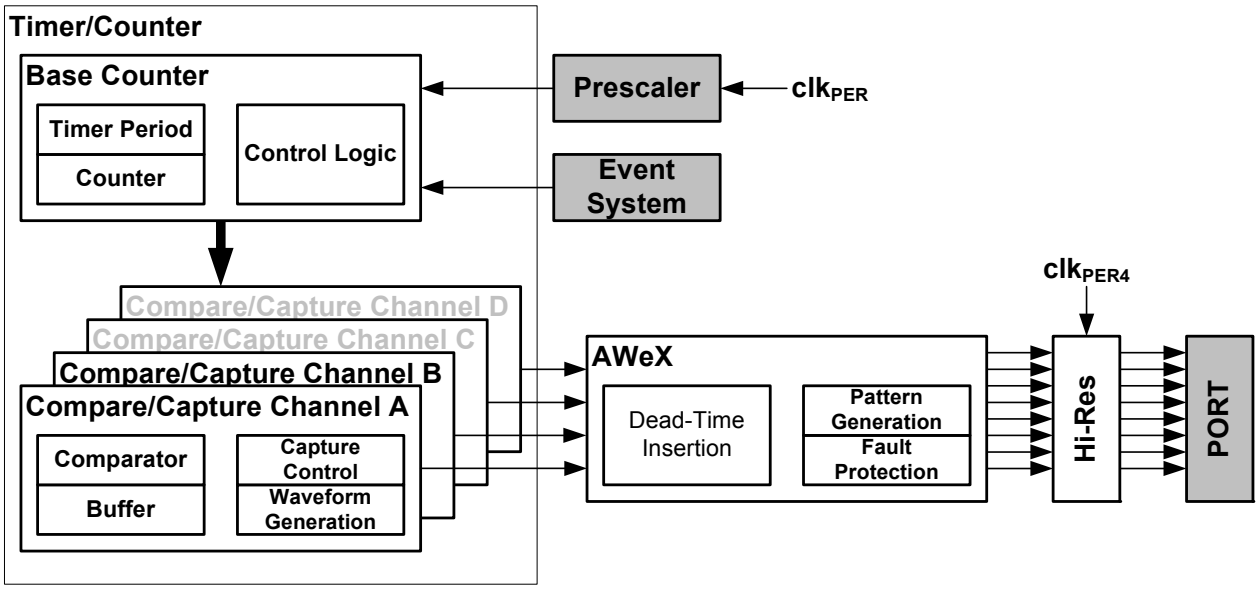
There are two differences between timer/counter type 0 and type 1. Timer/counter 0 has four CC channels, and timer/counter 1 has two CC channels. All information related to CC channels 3 and 4 is valid only for timer/counter 0. Only Timer/Counter 0 has the split mode feature that split it into two 8-bit Timer/Counters with four compare channels each.

Some timer/counters have extensions to enable more specialized waveform and frequency generation. The advanced waveform extension (AWeX) is intended for motor control and other power control applications. It enables low- and high-side output with dead-time insertion, as well as fault protection for disabling and shutting down external drivers. It can also generate a synchronized bit pattern across the port pins.

The advanced waveform extension can be enabled to provide extra and more advanced features for the Timer/Counter. This are only available for Timer/Counter 0. See “AWeX – Advanced Waveform Extension” on page 37 for more details.

The high-resolution (hi-res) extension can be used to increase the waveform output resolution by four or eight times by using an internal clock source running up to four times faster than the peripheral clock. See “Hi-Res – High Resolution Extension” on page 38 for more details.

Figure 15-1. Overview of a Timer/Counter and Closely Related Peripherals



PORTC has one Timer/Counter 0 and one Timer/Counter1. PORTD, PORTE and PORTF each has one Timer/Counter 0. Notation of these are TCC0 (Time/Counter C0), TCC1, TCD0, TCE0, and TCF0, respectively.

17. AWeX – Advanced Waveform Extension

17.1 Features

- Waveform output with complementary output from each compare channel
- Four dead-time insertion (DTI) units
  - 8-bit resolution
  - Separate high and low side dead-time setting
  - Double buffered dead time
  - Optionally halts timer during dead-time insertion
- Pattern generation unit creating synchronised bit pattern across the port pins
  - Double buffered pattern generation
  - Optional distribution of one compare channel output across the port pins
- Event controlled fault protection for instant and predictable fault triggering

17.2 Overview

The advanced waveform extension (AWeX) provides extra functions to the timer/counter in waveform generation (WG) modes. It is primarily intended for use with different types of motor control and other power control applications. It enables low- and high side output with dead-time insertion and fault protection for disabling and shutting down external drivers. It can also generate a synchronized bit pattern across the port pins.

Each of the waveform generator outputs from the timer/counter 0 are split into a complimentary pair of outputs when any AWeX features are enabled. These output pairs go through a dead-time insertion (DTI) unit that generates the non-inverted low side (LS) and inverted high side (HS) of the WG output with dead-time insertion between LS and HS switching. The DTI output will override the normal port value according to the port override setting.

The pattern generation unit can be used to generate a synchronized bit pattern on the port it is connected to. In addition, the WG output from compare channel A can be distributed to and override all the port pins. When the pattern generator unit is enabled, the DTI unit is bypassed.

The fault protection unit is connected to the event system, enabling any event to trigger a fault condition that will disable the AWeX output. The event system ensures predictable and instant fault reaction, and gives flexibility in the selection of fault triggers.

The AWeX is available for TCC0. The notation of this is AWEXC.

19. RTC – 16-bit Real-Time Counter

19.1 Features

- 16-bit resolution
- Selectable clock source
  - 32.768kHz external crystal
  - External clock
  - 32.768kHz internal oscillator
  - 32kHz internal ULP oscillator
- Programmable 10-bit clock prescaling
- One compare register
- One period register
- Clear counter on period overflow
- Optional interrupt/event on overflow and compare match

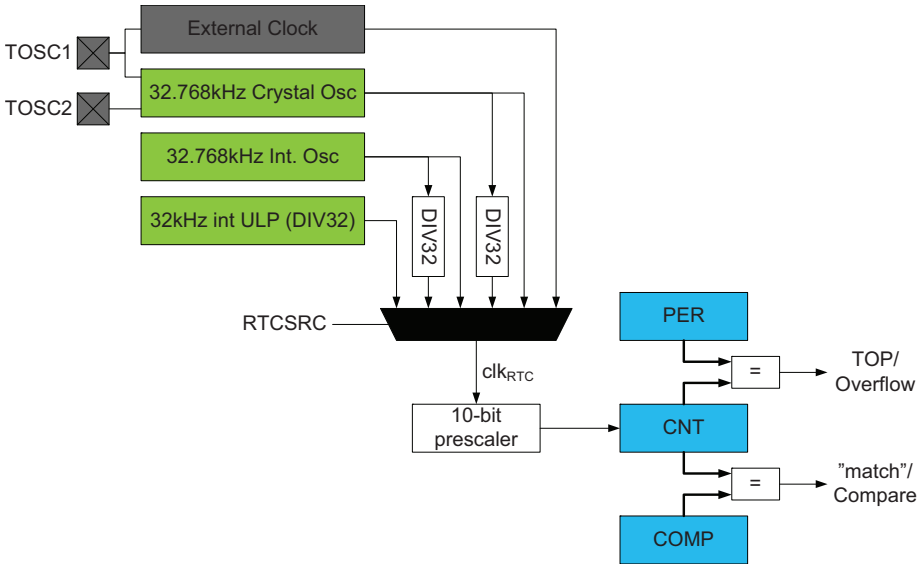
19.2 Overview

The 16-bit real-time counter (RTC) is a counter that typically runs continuously, including in low-power sleep modes, to keep track of time. It can wake up the device from sleep modes and/or interrupt the device at regular intervals.

The reference clock is typically the 1.024kHz output from a high-accuracy crystal of 32.768kHz, and this is the configuration most optimized for low power consumption. The faster 32.768kHz output can be selected if the RTC needs a resolution higher than 1ms. The RTC can also be clocked from an external clock signal, the 32.768kHz internal oscillator or the 32kHz internal ULP oscillator.

The RTC includes a 10-bit programmable prescaler that can scale down the reference clock before it reaches the counter. A wide range of resolutions and time-out periods can be configured. With a 32.768kHz clock source, the maximum resolution is 30.5µs, and time-out periods can range up to 2000 seconds. With a resolution of 1s, the maximum timeout period is more than18 hours (65536 seconds). The RTC can give a compare interrupt and/or event when the counter equals the compare register value, and an overflow interrupt and/or event when it equals the period register value.

Figure 19-1. Real-time Counter Overview



32.3.5 I/O Pin Characteristics

The I/O pins compiles with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits or exceeds this specification.

Table 32-65. I/O Pin Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} (1)/ I_{OL} (2)	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage	V_{CC} = 2.4 - 3.6V		0.7 * V_{CC}		V_{CC} + 0.5	V
		V_{CC} = 1.6 - 2.4V		0.8 * V_{CC}		V_{CC} + 0.5	
V_{IL}	Low level input voltage	V_{CC} = 2.4 - 3.6V		-0.5		0.3 * V_{CC}	
		V_{CC} = 1.6 - 2.4V		-0.5		0.2 * V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.6		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current I/O pin	T = 25°C			<0.01	1.0	µA
R_P	Pull/buss keeper resistor				25		kΩ

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
   The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
   The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance [1]	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		44k		Ω
			1MHz resonator, CL=20pF		67k		
			2MHz resonator, CL=20pF		67k		
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal		82k		
			8MHz crystal		1500		
			9MHz crystal		1500		
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal		2700		
			9MHz crystal		2700		
			12MHz crystal		1000		
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal		3600		
			12MHz crystal		1300		
			16MHz crystal		590		
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal		390		
			12MHz crystal		50		
			16MHz crystal		10		
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal		1500		
			12MHz crystal		650		
			16MHz crystal		270		
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal		1000		
			16MHz crystal		440		
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal		1300		
			16MHz crystal		590		
	ESR	SF = safety factor				$min(R_Q)/SF$	kΩ
	Start-up time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		1.0		ms
		XOSCPWR=0, FRQRANGE=1	2MHz crystal, CL=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz crystal, CL=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz crystal, CL=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz crystal, CL=20pF		1.4		

32.4.14 SPI Characteristics

Figure 32-26. SPI Timing Requirements in Master Mode

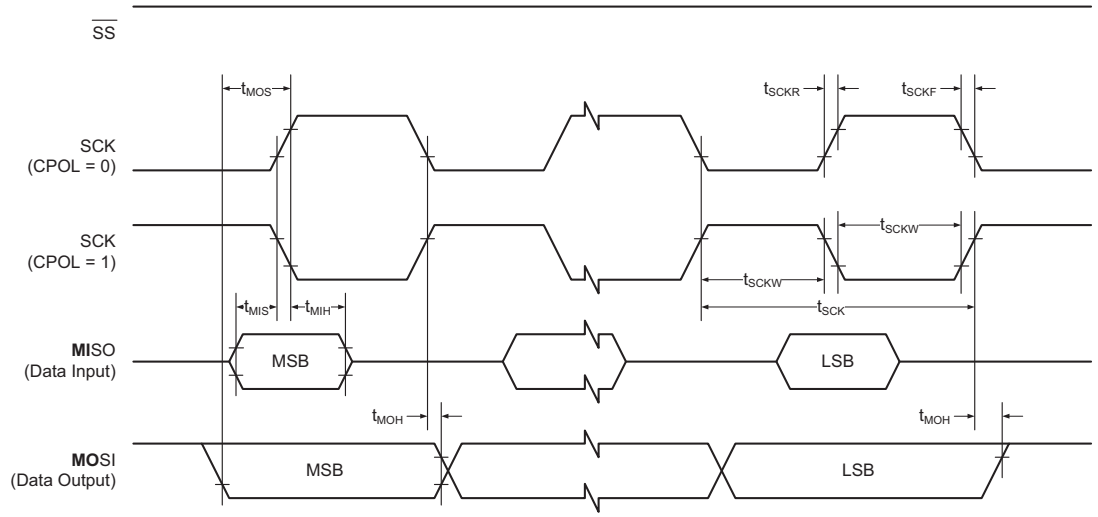
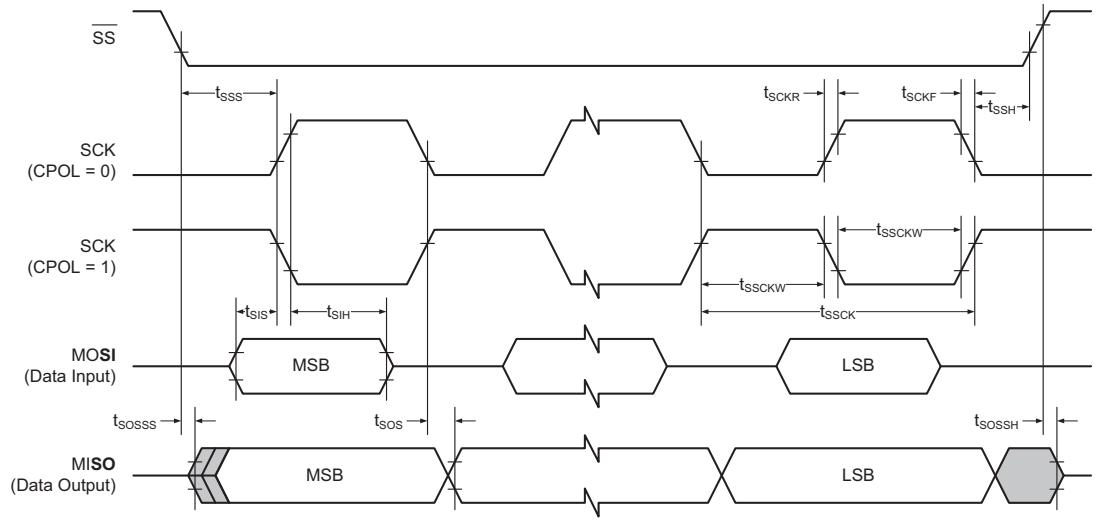


Figure 32-27.SPI Timing Requirements in Slave Mode



33.1.3 ADC Characteristics

Figure 33-31. INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

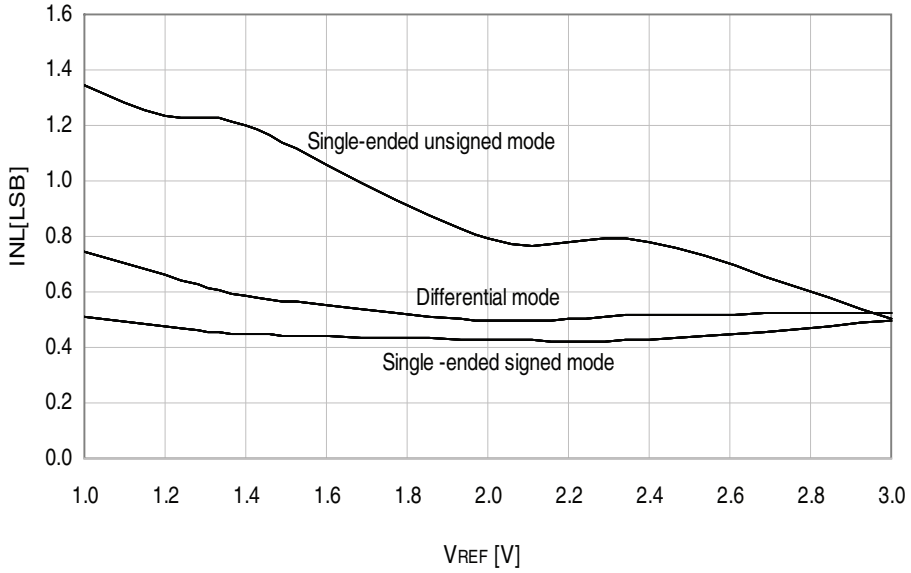


Figure 33-32. INL Error vs. Sample Rate

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external

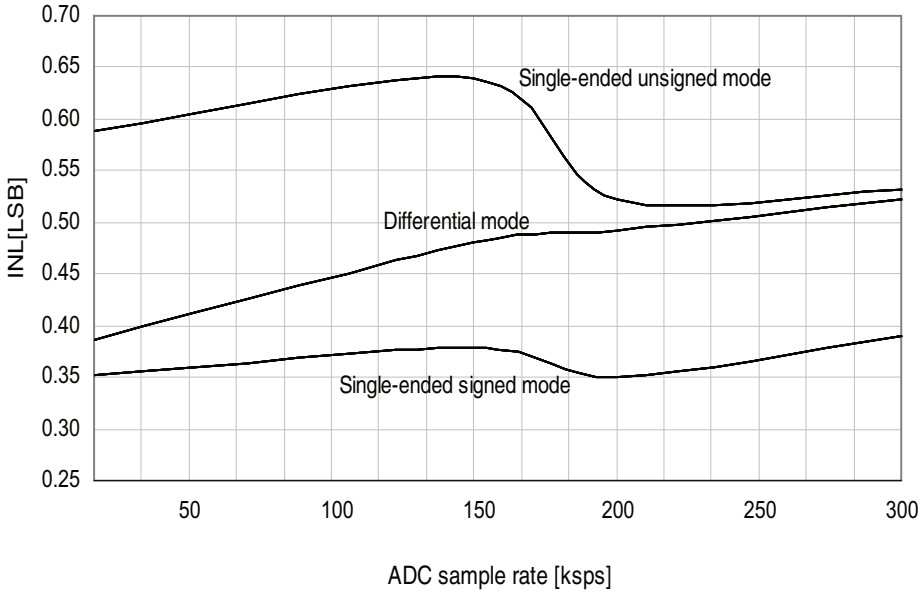
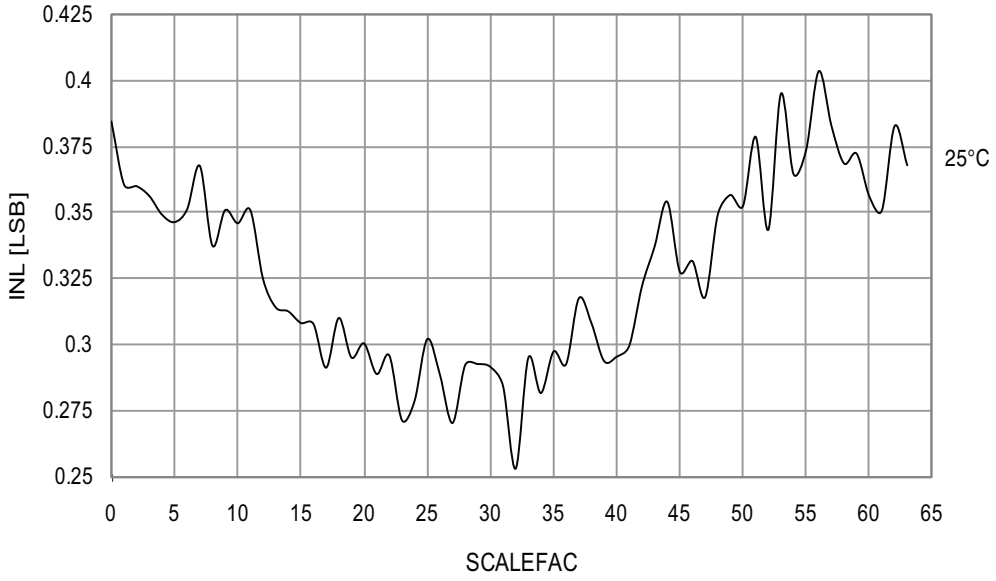


Figure 33-45. Voltage Scaler INL vs. SCALEFAC

T = 25°C, V_{CC} = 3.0V



33.1.5 Internal 1.0V Reference Characteristics

Figure 33-46. ADC Internal 1.0V Reference vs. Temperature

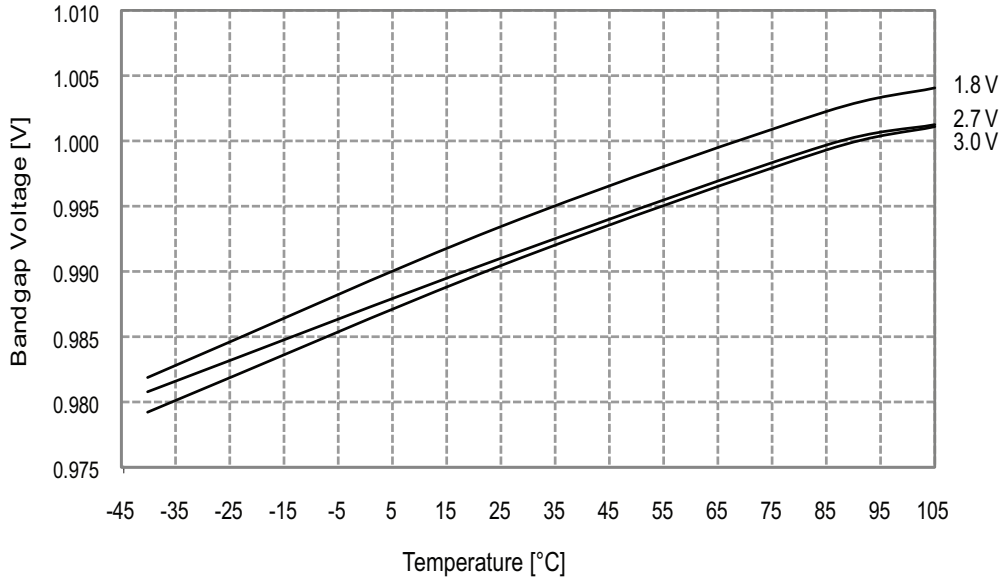
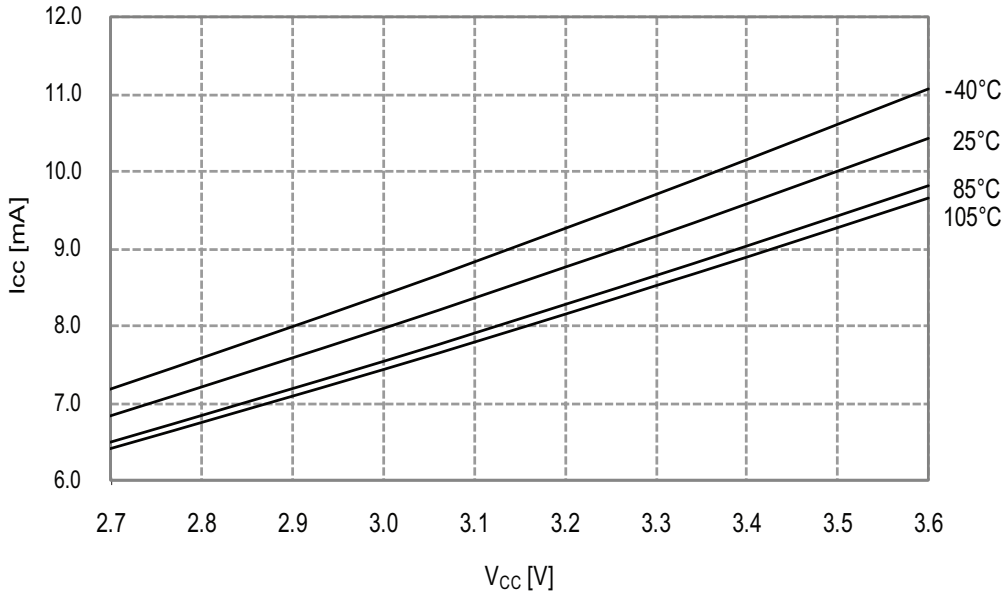


Figure 33-78.Active Mode Supply Current vs. V_{CC}

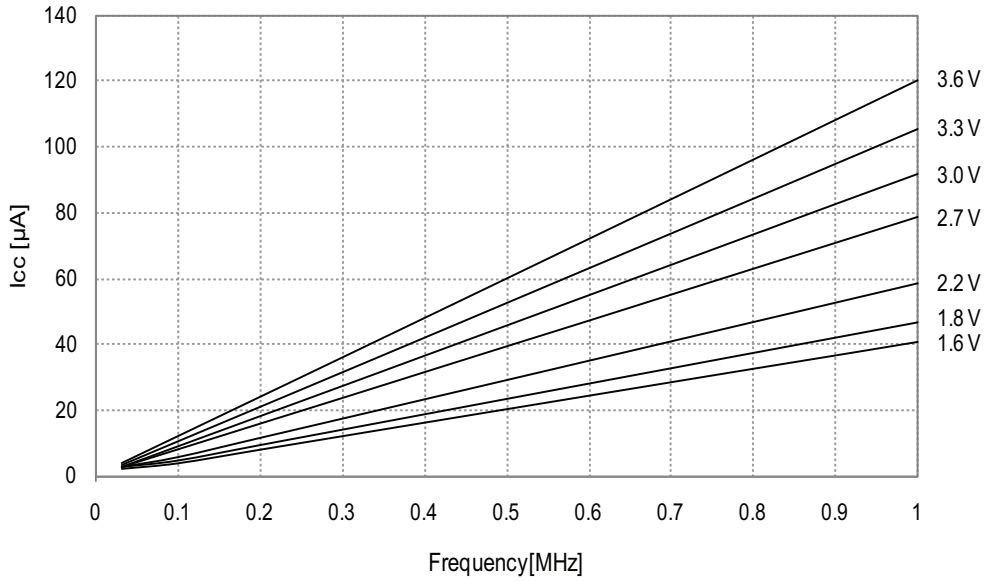
f_{SYS} = 32MHz internal oscillator



33.2.1.2 Idle Mode Supply Current

Figure 33-79.Idle Mode Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C



33.2.2 I/O Pin Characteristics

33.2.2.1 Pull-up

Figure 33-90. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = 1.8V

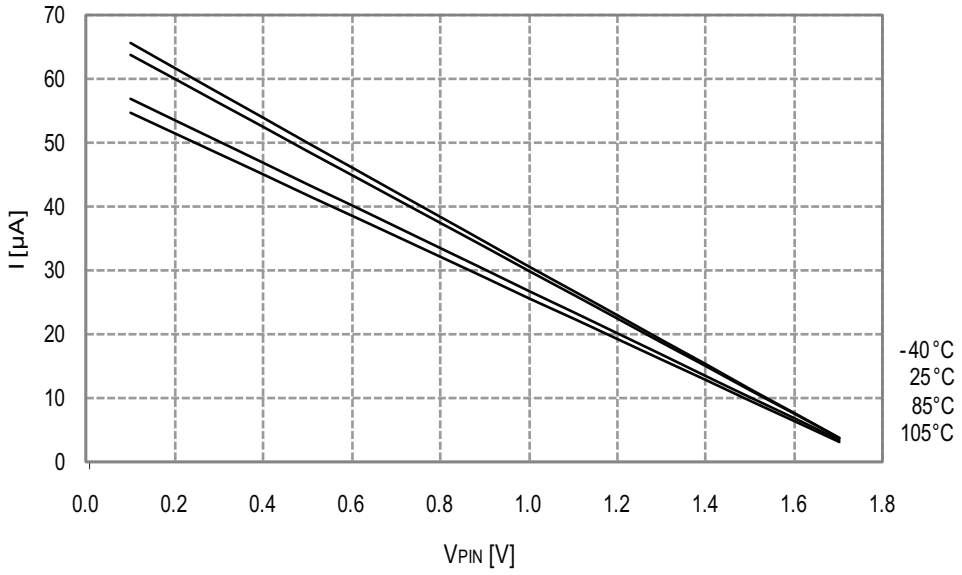


Figure 33-91. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = 3.0V

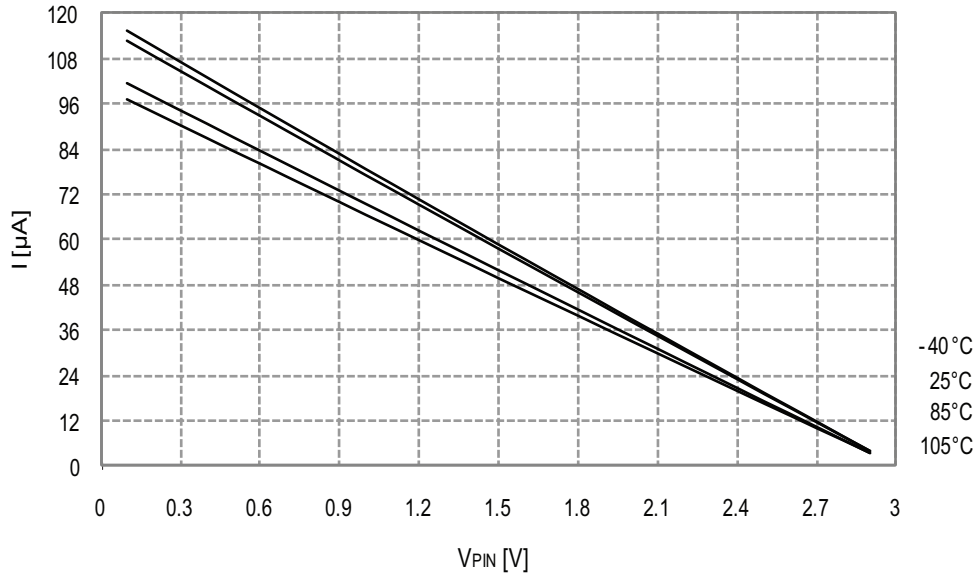
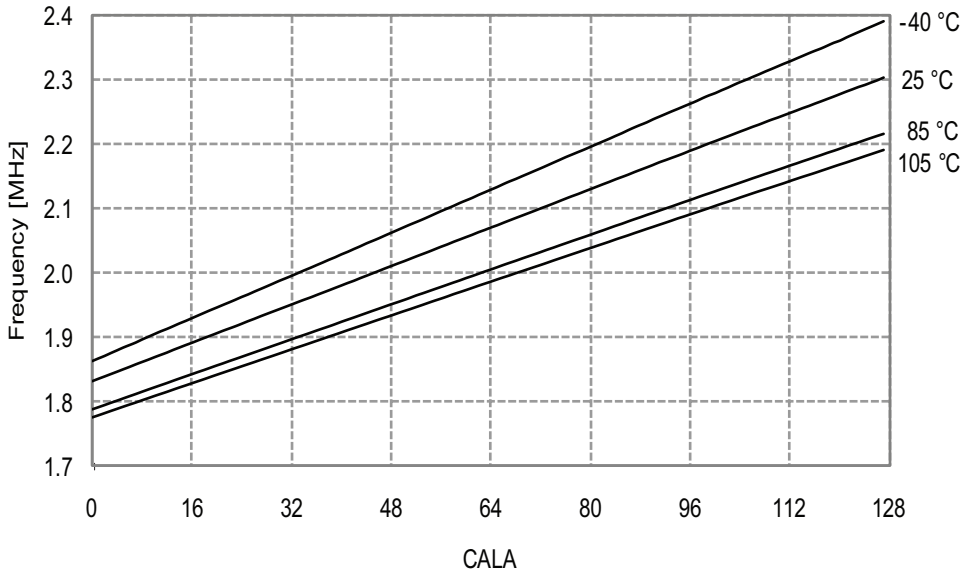


Figure 33-130. 2MHz Internal Oscillator Frequency vs. CALA Calibration Value

V_{CC} = 3V



33.2.8.4 32MHz Internal Oscillator

Figure 33-131. 32MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled

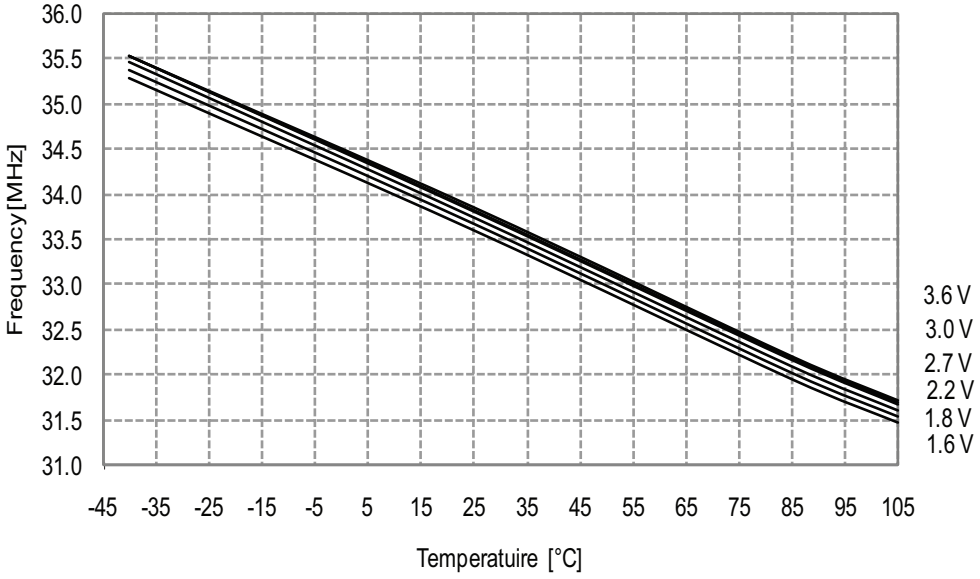


Figure 33-177. DNL Error vs. Input Code

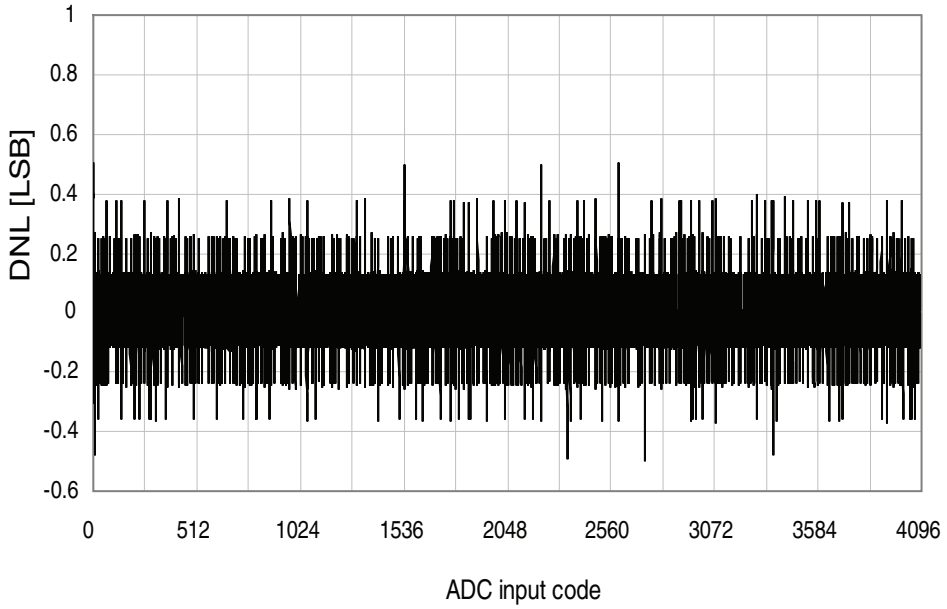
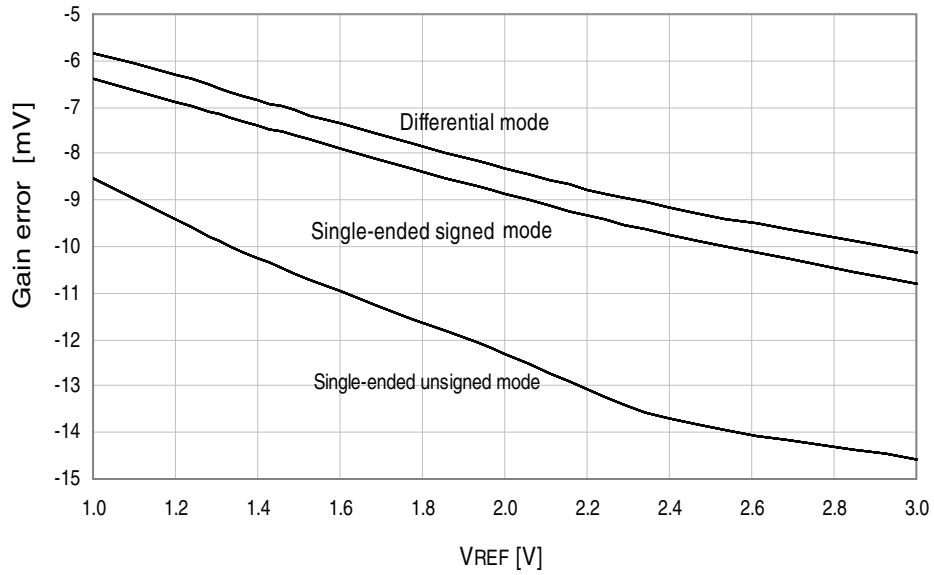


Figure 33-178. Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps



33.4 Atmel ATxmega192D3

33.4.1 Current Consumption

33.4.1.1 Active Mode Supply Current

Figure 33-213.Active Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C

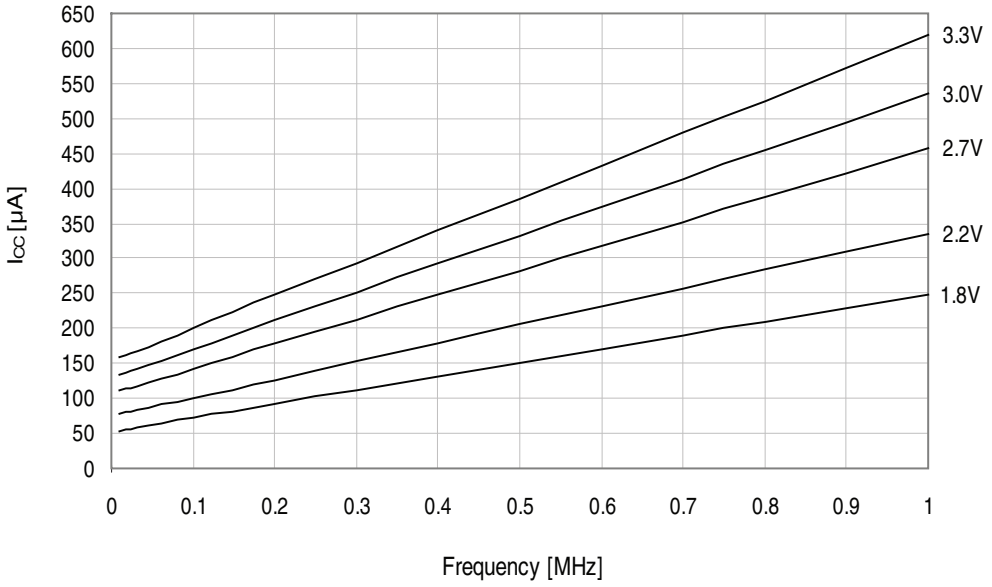


Figure 33-214.Active Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C

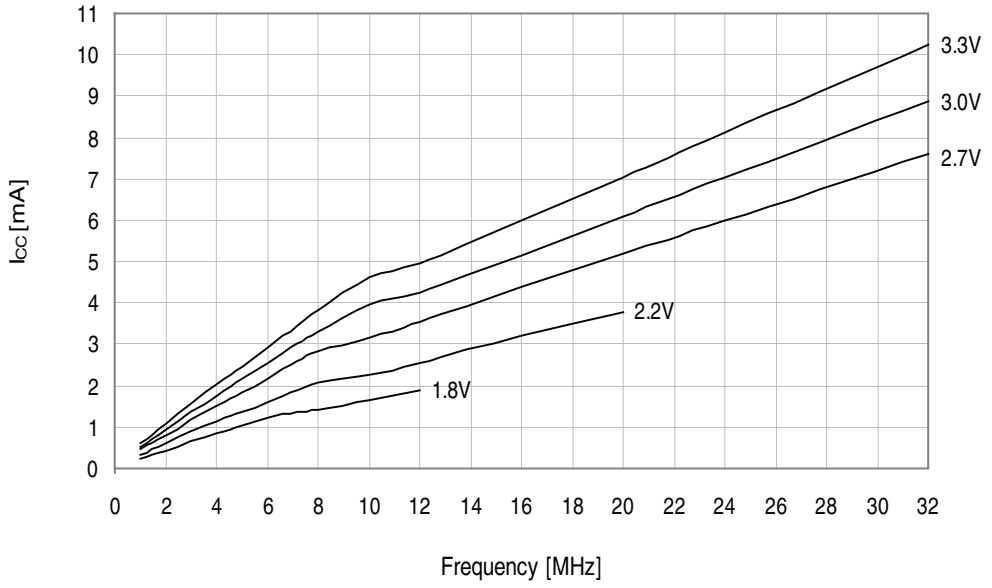


Figure 33-287.Active Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator

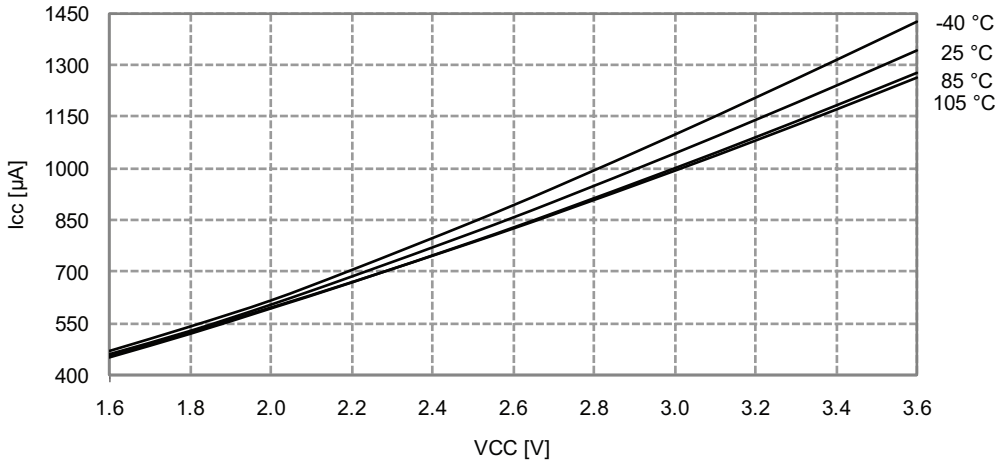
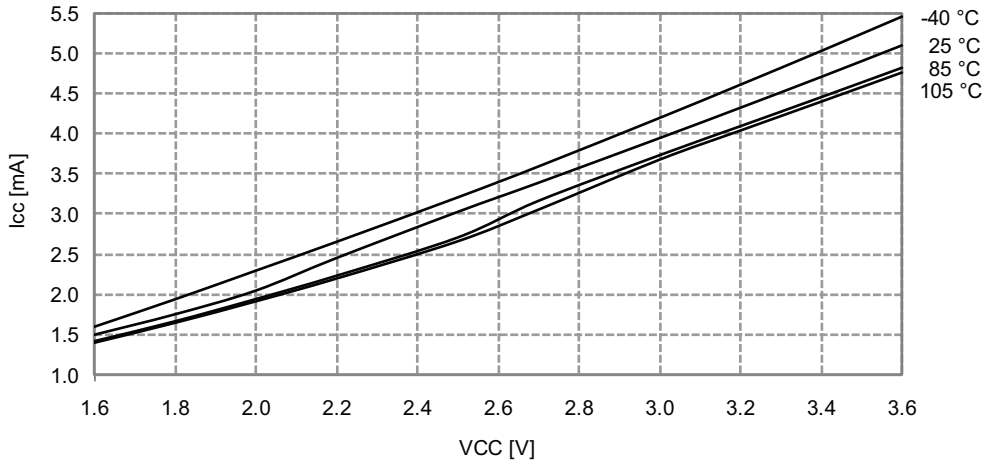


Figure 33-288.Active Mode Supply Current vs. V_{CC}

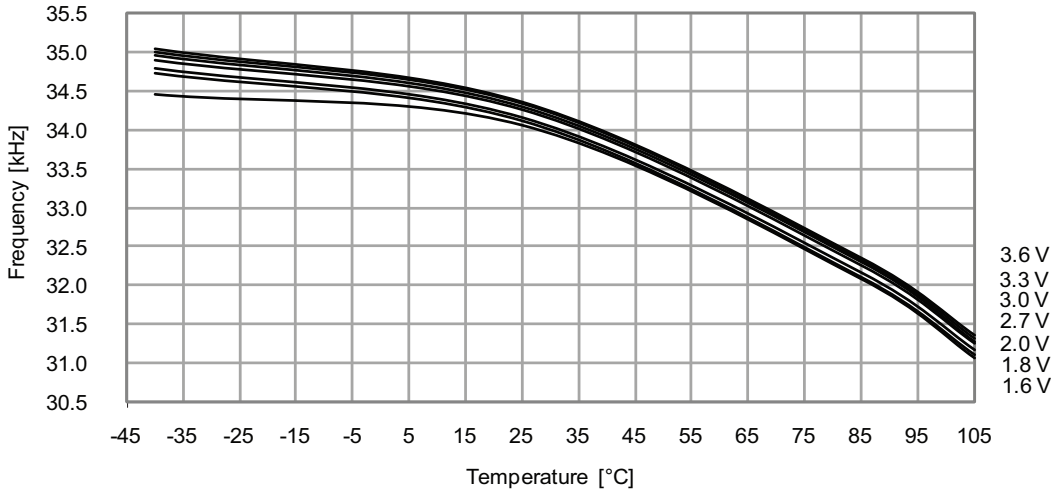
f_{SYS} = 32MHz internal oscillator prescaled to 8MHz



33.5.8 Oscillator Characteristics

33.5.8.1 Ultra Low-Power Internal Oscillator

Figure 33-335. Ultra Low-Power Internal Oscillator Frequency vs. Temperature



33.5.8.2 32.768kHz Internal Oscillator

Figure 33-336. 32.768kHz Internal Oscillator Frequency vs. Temperature

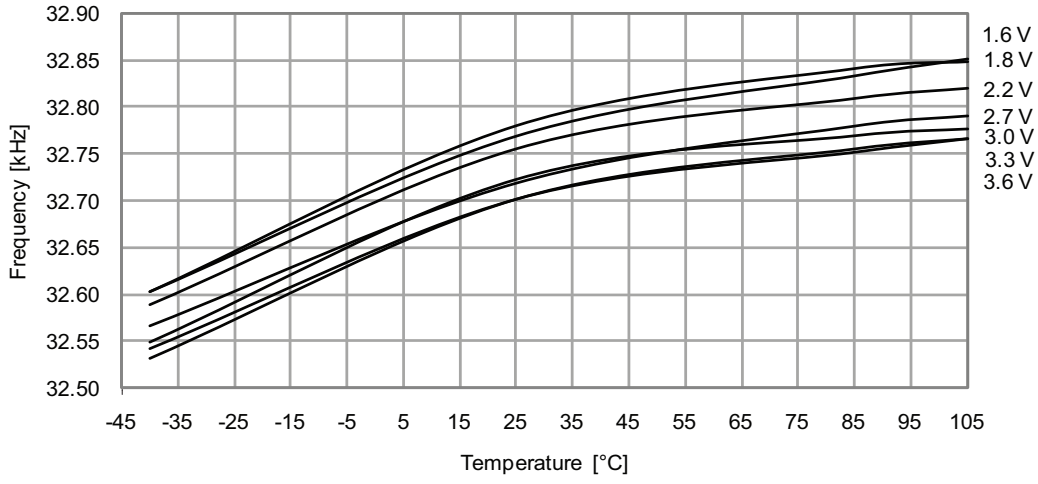


Figure 33-343. 32MHz Internal Oscillator CALA Calibration Step Size

T = -40°C, V_{CC} = 3.0V

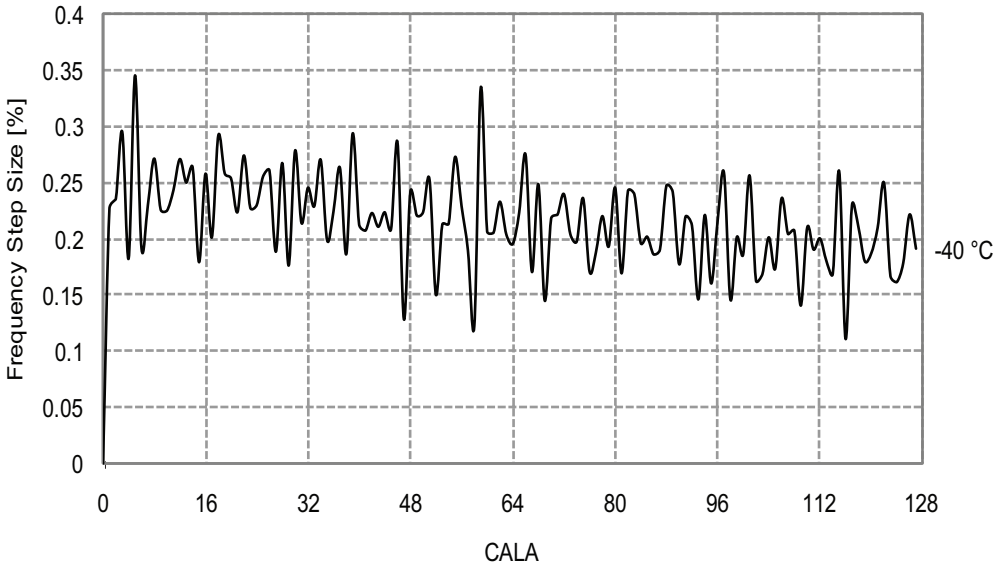
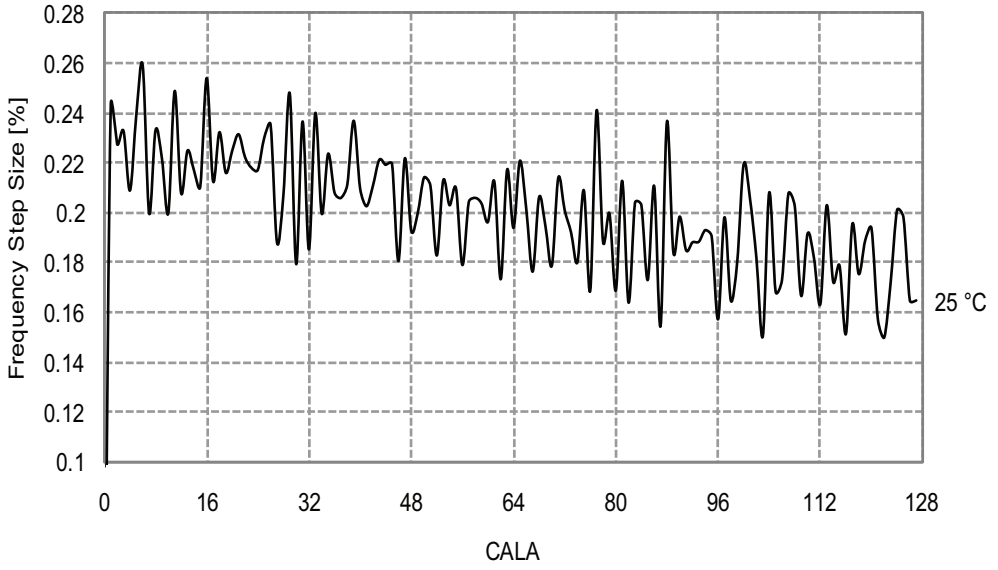


Figure 33-344. 32MHz Internal Oscillator CALA Calibration Step Size

T = 25°C, V_{CC} = 3.0V



33.6.2.2 Output Voltage vs. Sink/Source Current

Figure 33-373.I/O Pin Output Voltage vs. Source Current

V_{CC} = *1.8V*

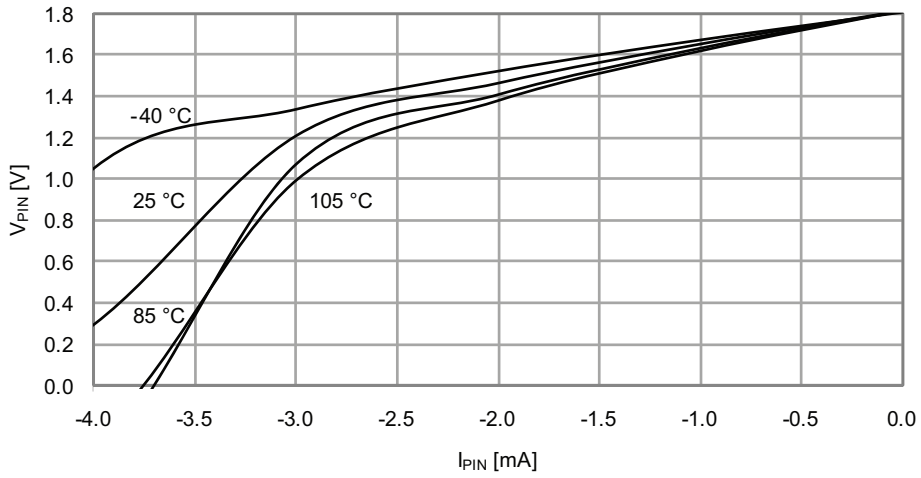


Figure 33-374.I/O Pin Output Voltage vs. Source Current

V_{CC} = *3.0V*

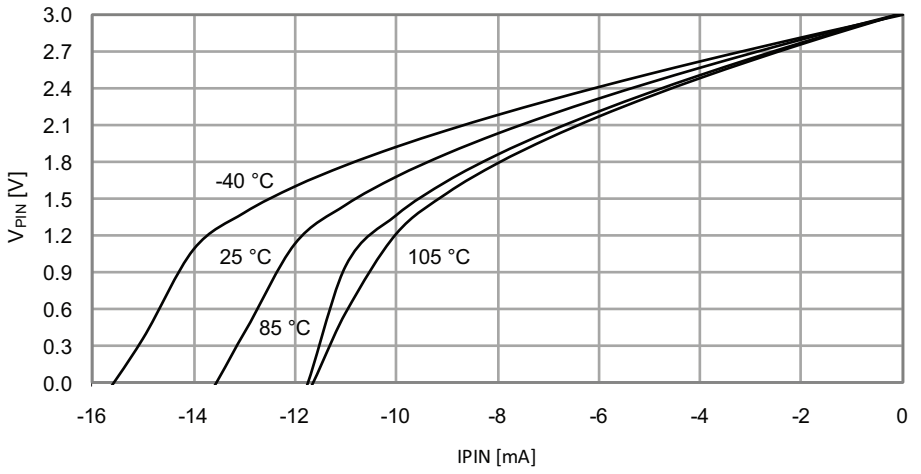
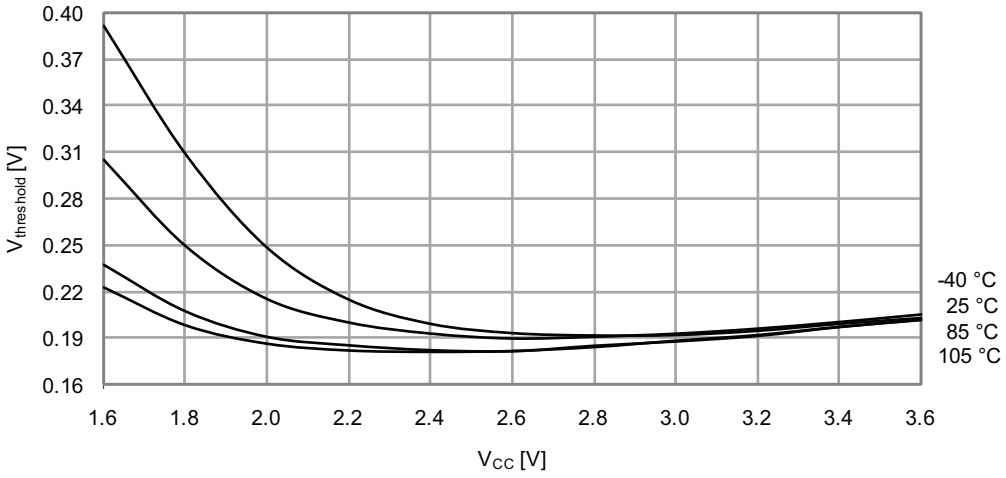


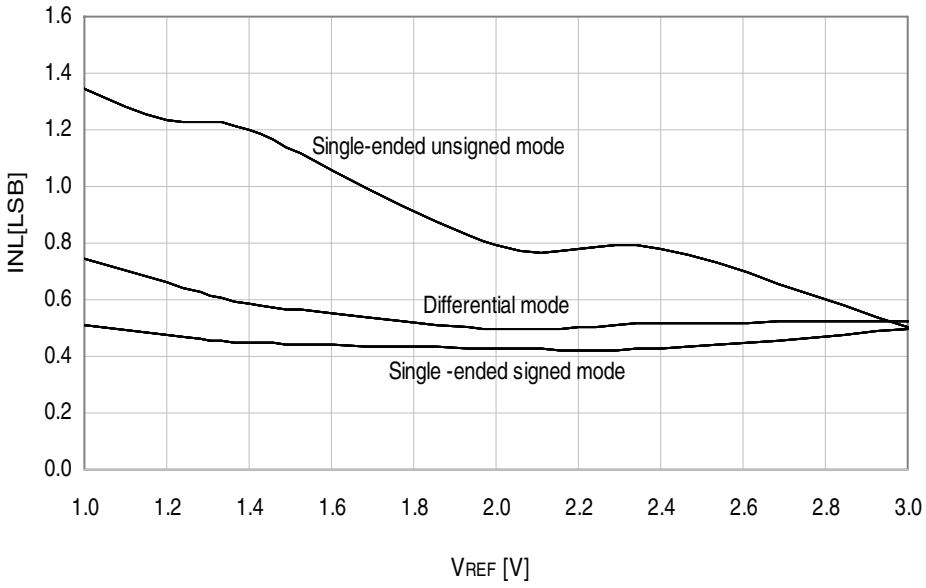
Figure 33-381.I/O Pin Input Hysteresis vs. V_{CC}



33.6.3 ADC Characteristics

Figure 33-382. INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference



- 1× gain: 2.4 V
- 2× gain: 1.2 V
- 4× gain: 0.6 V
- 8× gain: 300 mV
- 16× gain: 150 mV
- 32× gain: 75 mV
- 64× gain: 38 mV

Problem fix/workaround

Keep the amplified voltage output from the ADC gain stage below 2.4V in order to get a correct result, or keep ADC voltage reference below 2.4V.

6. ADC Event on compare match non-functional

ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

Problem fix/workaround

Enable and use interrupt on compare match when using the compare function.

7. ADC propagation delay is not correct when 8× – 64× gain is used

The propagation delay will increase by only one ADC clock cycle for all gain settings.

Problem fix/workaround

None.

8. Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V

The ADC can not be used to do bandgap measurements when V_{CC} is below 2.7V.

Problem fix/workaround

None.

9. Accuracy lost on first three samples after switching input to ADC gain stage

Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

Problem fix/workaround

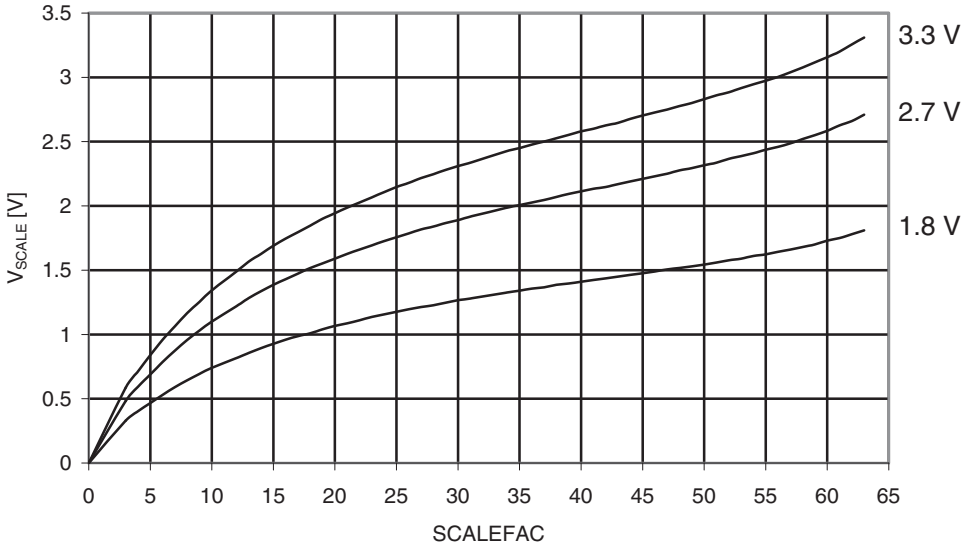
Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

10. Configuration of PGM and CWCM not as described in XMEGA D Manual

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

Figure 34-6. Analog Comparator Voltage Scaler vs. Scalefac
T = 25°C



Problem fix/workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed.

3. ADC gain stage cannot be used for single conversion

The ADC gain stage will not output correct result for single conversion that is triggered and started from software or event system.

Problem fix/workaround

When the gain stage is used, the ADC must be set in free running mode for correct results.

4. ADC has increased INL error for some operating conditions

Some ADC configurations or operating condition will result in increased INL error.

In signed mode INL is increased to:

6LSB for sample rates above 130ksps, and up to 8LSB for 200ksps sample rate.

6LSB for reference voltage below 1.1V when V_{CC} is above 3.0V.

20LSB for ambient temperature below 0°C and reference voltage below 1.3V.

In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

Problem fix/workaround

None, avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

5. ADC gain stage output range is limited to 2.4V

The amplified output of the ADC gain stage will never go above 2.4V, hence the differential input will only give correct output when below 2.4V/gain. For the available gain settings, this gives a differential input range of: