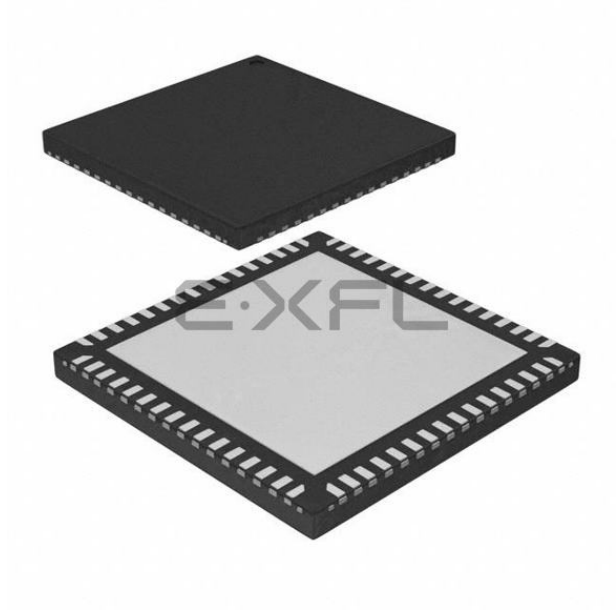

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32d3-mn

12. WDT – Watchdog Timer

12.1 Features

- Issues a device reset if the timer is not reset before its timeout period
- Asynchronous operation from dedicated oscillator
- 1kHz output of the 32kHz ultra low power oscillator
- 11 selectable timeout periods, from 8ms to 8s
- Two operation modes:
  - Normal mode
  - Window mode
- Configuration lock to prevent unwanted changes

12.2 Overview

The watchdog timer (WDT) is a system function for monitoring correct program operation. It makes it possible to recover from error situations such as runaway or deadlocked code. The WDT is a timer, configured to a predefined timeout period, and is constantly running when enabled. If the WDT is not reset within the timeout period, it will issue a microcontroller reset. The WDT is reset by executing the WDR (watchdog timer reset) instruction from the application code.

The window mode makes it possible to define a time slot or window inside the total timeout period during which WDT must be reset. If the WDT is reset outside this window, either too early or too late, a system reset will be issued. Compared to the normal mode, this can also catch situations where a code error causes constant WDR execution.

The WDT will run in active mode and all sleep modes, if enabled. It is asynchronous, runs from a CPU-independent clock source, and will continue to operate to issue a system reset even if the main clocks fail.

The configuration change protection mechanism ensures that the WDT settings cannot be changed by accident. For increased safety, a fuse for locking the WDT settings is also available.

13. Interrupts and Programmable Multilevel Interrupt Controller

13.1 Features

- Short and predictable interrupt response time
- Separate interrupt configuration and vector address for each interrupt
- Programmable multilevel interrupt controller
  - Interrupt prioritizing according to level and vector address
  - Three selectable interrupt levels for all interrupts: low, medium, and high
  - Selectable, round-robin priority scheme within low-level interrupts
  - Non-maskable interrupts for critical functions
- Interrupt vectors optionally placed in the application section or the boot loader section

13.2 Overview

Interrupts signal a change of state in peripherals, and this can be used to alter program execution. Peripherals can have one or more interrupts, and all are individually enabled and configured. When an interrupt is enabled and configured, it will generate an interrupt request when the interrupt condition is present. The programmable multilevel interrupt controller (PMIC) controls the handling and prioritizing of interrupt requests. When an interrupt request is acknowledged by the PMIC, the program counter is set to point to the interrupt vector, and the interrupt handler can be executed.

All peripherals can select between three different priority levels for their interrupts: low, medium, and high. Interrupts are prioritized according to their level and their interrupt vector address. Medium-level interrupts will interrupt low-level interrupt handlers. High-level interrupts will interrupt both medium- and low-level interrupt handlers. Within each level, the interrupt priority is decided from the interrupt vector address, where the lowest interrupt vector address has the highest interrupt priority. Low-level interrupts have an optional round-robin scheduling scheme to ensure that all interrupts are serviced within a certain amount of time.

Non-maskable interrupts (NMI) are also supported, and can be used for system critical functions.

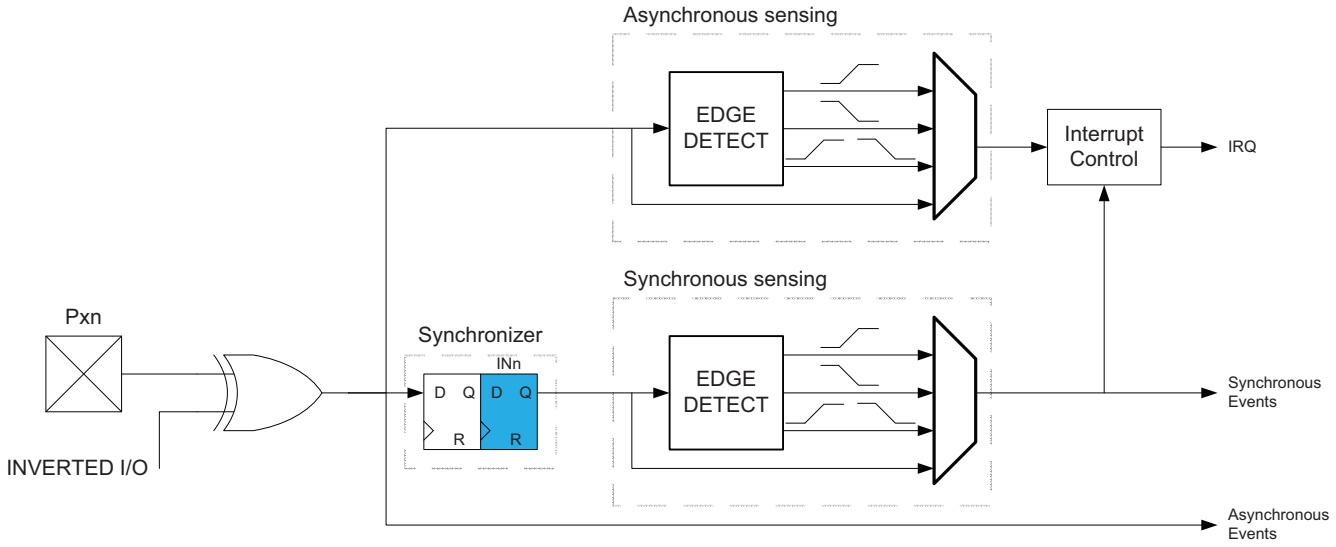
13.3 Interrupt Vectors

The interrupt vector is the sum of the peripheral's base interrupt address and the offset address for specific interrupts in each peripheral. The base addresses for the Atmel AVR XMEGA D3 devices are shown in Table 13-1 on page 29. Offset addresses for each interrupt available in the peripheral are described for each peripheral in the XMEGA D manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in Table 13-1 on page 29. The program address is the word address.

14.4 Input Sensing

Input sensing is synchronous or asynchronous depending on the enabled clock for the ports, and the configuration is shown in Figure 14-7.

Figure 14-7. Input Sensing System Overview



When a pin is configured with inverted I/O, the pin value is inverted before the input sensing.

14.5 Alternate Port Functions

Most port pins have alternate pin functions in addition to being a general purpose I/O pin. When an alternate function is enabled, it might override the normal port pin function or pin value. This happens when other peripherals that require pins are enabled or configured to use pins. If and how a peripheral will override and use pins is described in the section for that peripheral. “Pinout and Pin Functions” on page 50 shows which modules on peripherals that enable alternate functions on a pin, and which alternate functions that are available on a pin.

32.3.6 ADC Characteristics

Table 32-66. Power Supply, Reference, and Input Range

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC} - 0.3		V_{CC} + 0.3	V
V_{REF}	Reference voltage		1		AV_{CC} - 0.6	
R_{in}	Input resistance	Switched			4.5	kΩ
C_{in}	Input capacitance	Switched			5	pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF
V_{in}	Input range		0		V_{REF}	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	
	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF} - ΔV	
ΔV	Fixed offset voltage			200		lsb

Table 32-67. Clock and Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC clock frequency	Maximum is 1/4 of peripheral clock frequency	100		1800	kHz
		Measuring internal signals	100		125	
f_{ClkADC}	Sample rate		16		300	ksps
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	16		300	ksps
		CURRLIMIT = LOW	16		250	
		CURRLIMIT = MEDIUM	16		150	
		CURRLIMIT = HIGH	16		50	
	Sampling time	1/2 Clk_{ADC} cycle	0.28		320	µs
	Conversion time (latency)	(RES+2)/2 + GAIN RES (Resolution) = 8 or 12, GAIN = 0 to 3	5.5		10	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	
	ADC settling time	After changing reference or input mode		7	7	

32.3.8 Bandgap and Internal 1.0V Reference Characteristics

Table 32-71. Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC		1 Clk_{PER} + 2.5µs		µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T = 85°C, after calibration	0.99	1.0	1.01	
	Variation over voltage and temperature	Calibrated at T = 85°C		1		%

32.3.9 Brownout Detection Characteristics

Table 32-72. Brownout Detection Characteristics (1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.40	1.60	1.70	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.0		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

32.3.10 External Reset Characteristics

Table 32-73. External Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width		1000	100		ns
V_{RST}	Reset threshold voltage	V_{CC} = 2.7 - 3.6V		0.45 * V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.45 * V_{CC}		
R_{RST}	Reset pin pull-up resistor			27		kΩ

Table 32-121. Current Consumption for Modules and Peripherals

Symbol	Parameter	Condition [1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				0.9		µA
	32.768kHz int. oscillator				25		
	2MHz int. oscillator				78		
		DFLL enabled with 32.768kHz int. osc. as reference			110		
	32MHz int. oscillator				250		
		DFLL enabled with 32.768kHz int. osc. as reference			440		
	PLL	20× multiplication factor, 32MHz int. osc. DIV4 as reference			310		
	Watchdog timer				1.0		
	BOD	Continuous mode			132		
		Sampled mode, includes ULP oscillator			1.4		
	Internal 1.0V reference				185		
	Temperature sensor				182		
	ADC	16ksps V_{REF} = Ext. ref.			1.12		mA
			CURRLIMIT = LOW		1.01		
			CURRLIMIT = MEDIUM		0.9		
			CURRLIMIT = HIGH		0.8		
		75ksps V_{REF} = Ext. ref.	CURRLIMIT = LOW		1.7		
		300ksps V_{REF} = Ext. ref.			3.1		
	USART	Rx and Tx enabled, 9600 BAUD			9.5		µA
	Flash memory and EEPROM programming				10		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

33.1.10 PDI Characteristics

Figure 33-71. Maximum PDI Frequency vs. V_{CC}

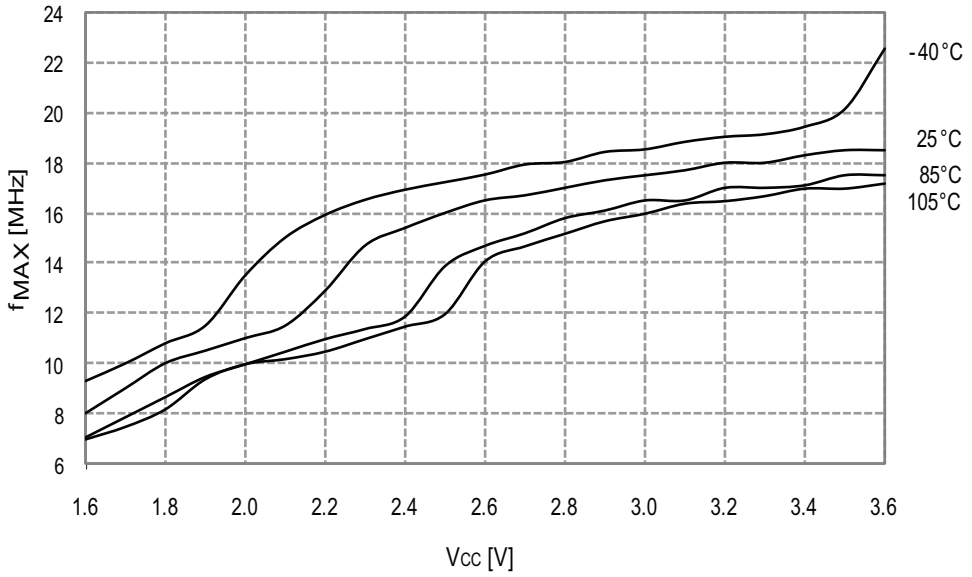


Figure 33-76. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator

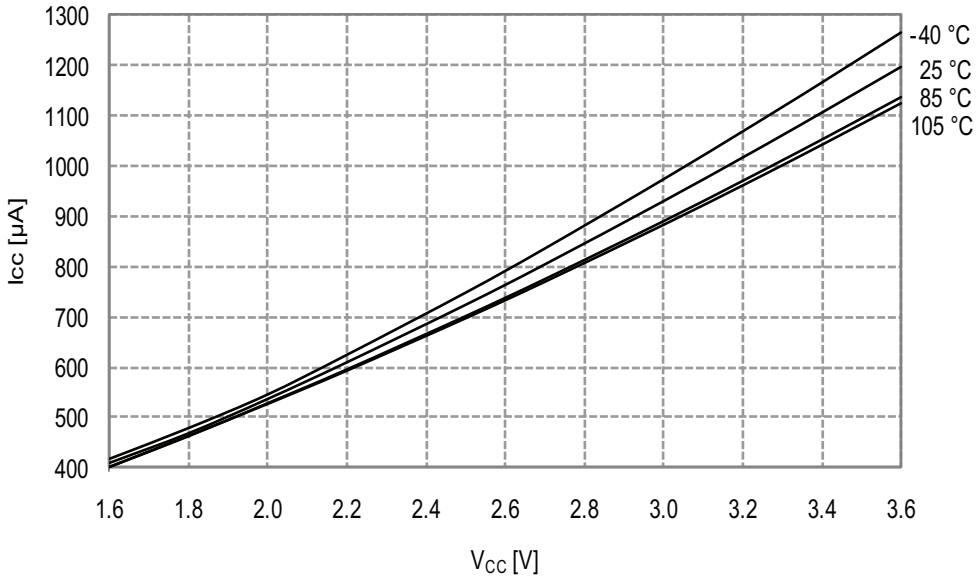


Figure 33-77. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz

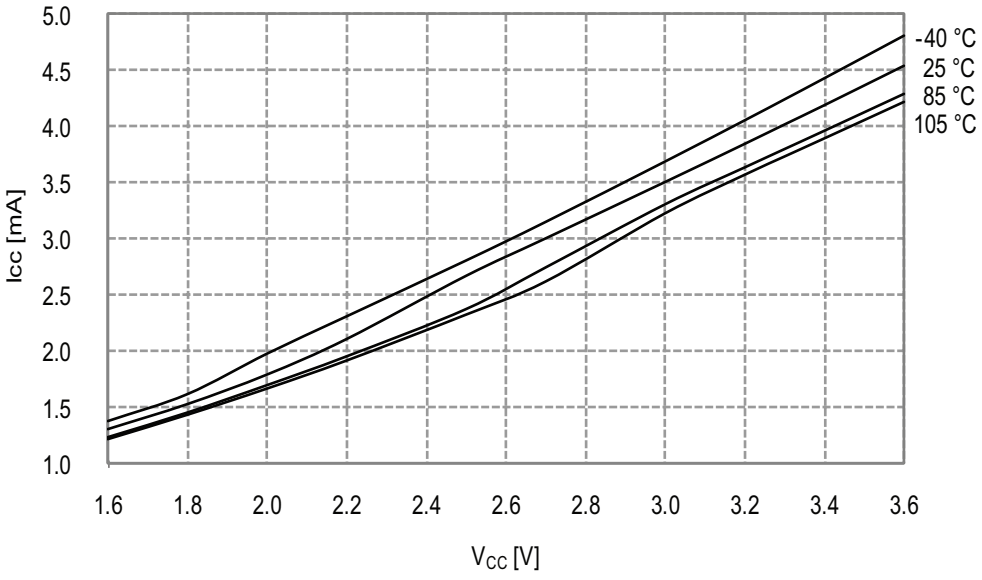
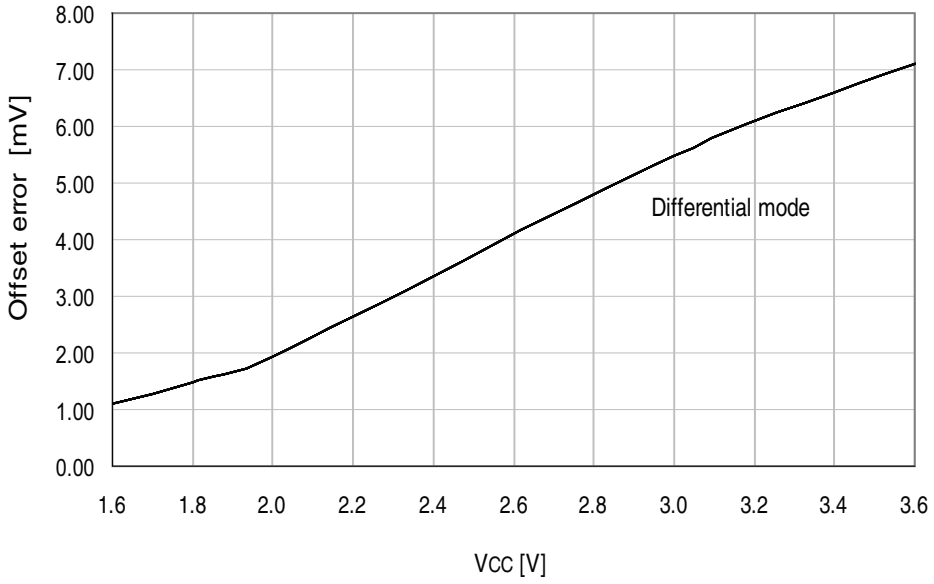


Figure 33-112. Offset Error vs. V_{CC}

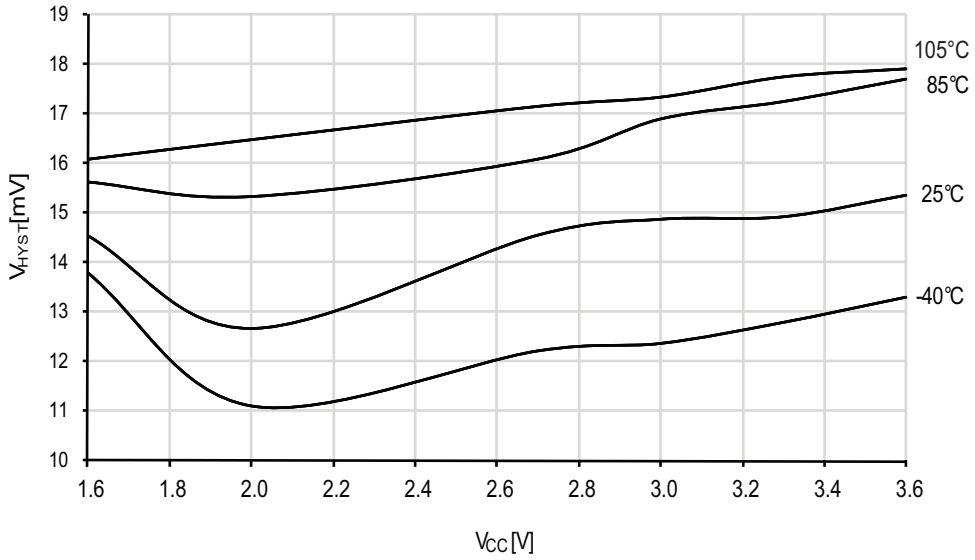
T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps



33.2.4 Analog Comparator Characteristics

Figure 33-113. Analog Comparator Hysteresis vs. V_{CC}

Small hysteresis



33.2.9 Two-Wire Interface Characteristics

Figure 33-140. SDA Hold Time vs. Temperature

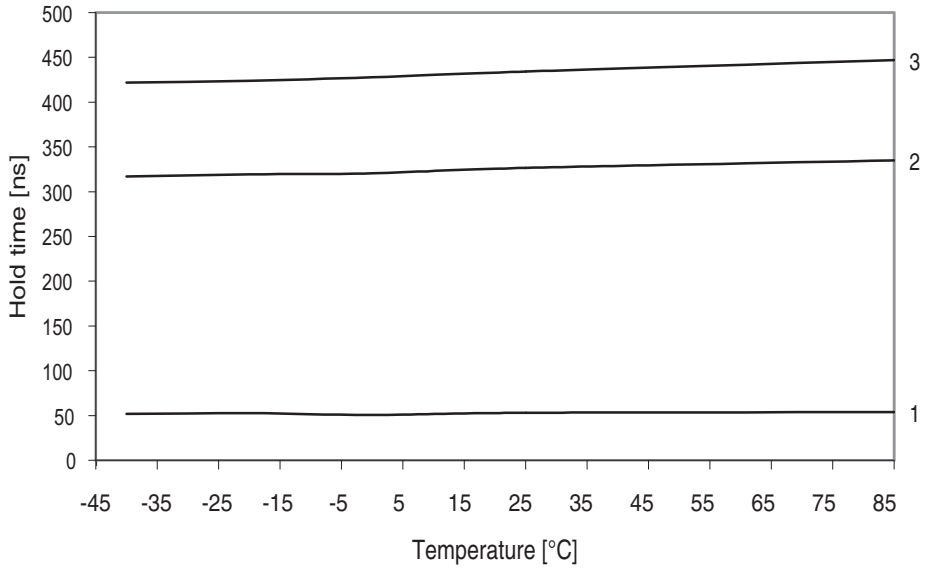


Figure 33-141. SDA Hold Time vs. Supply Voltage

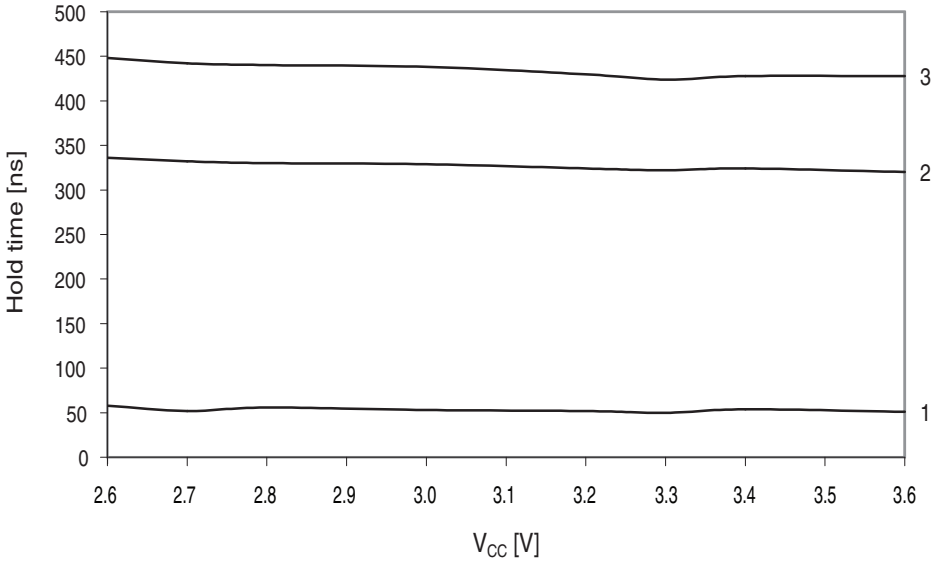


Figure 33-153. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

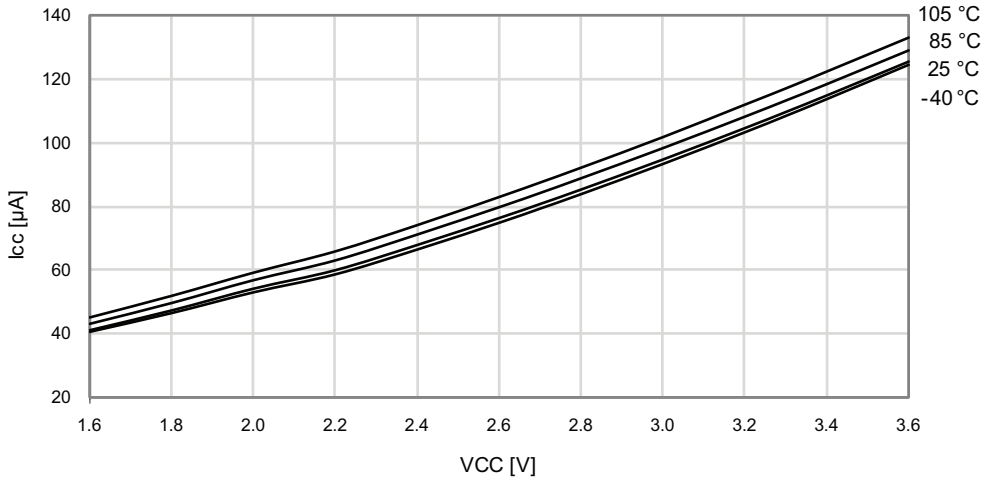


Figure 33-154. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator

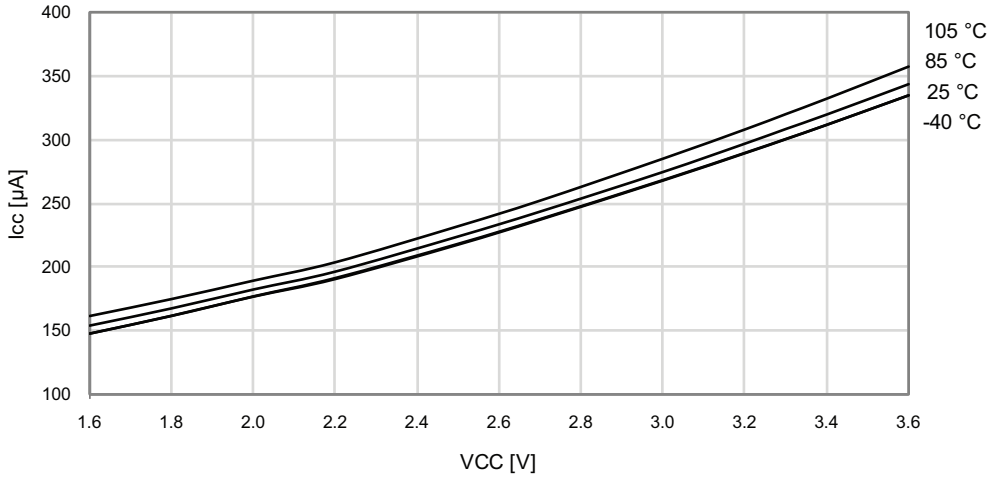


Figure 33-179. Gain Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps

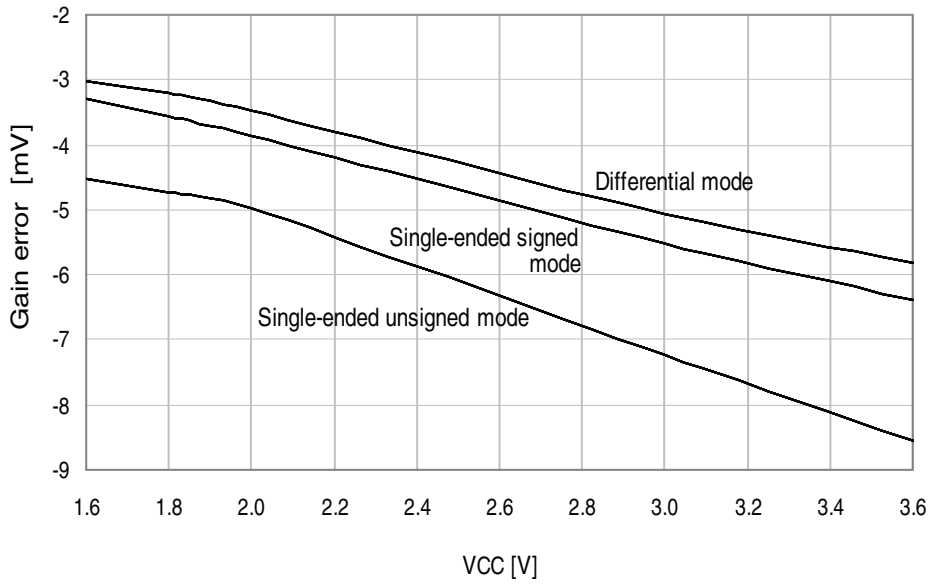


Figure 33-180. Offset Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

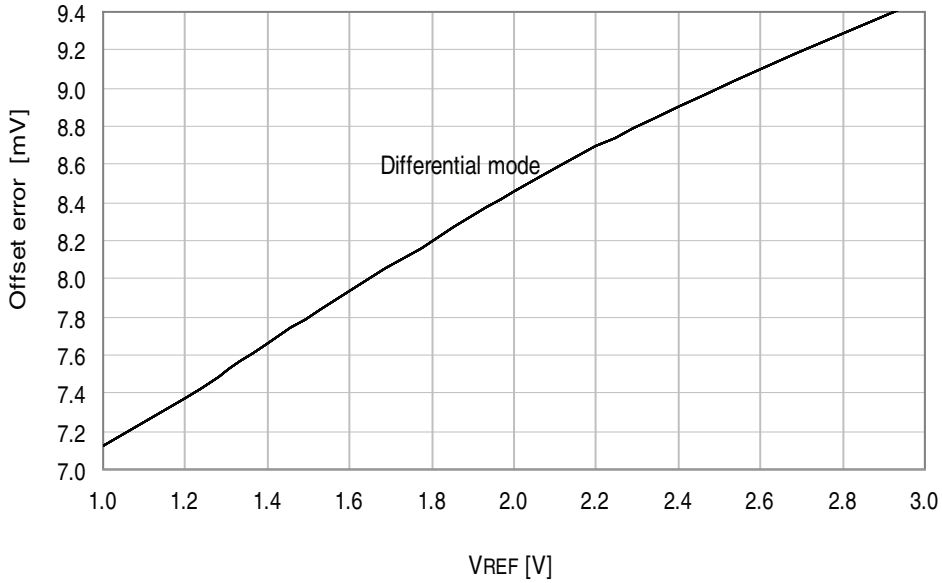
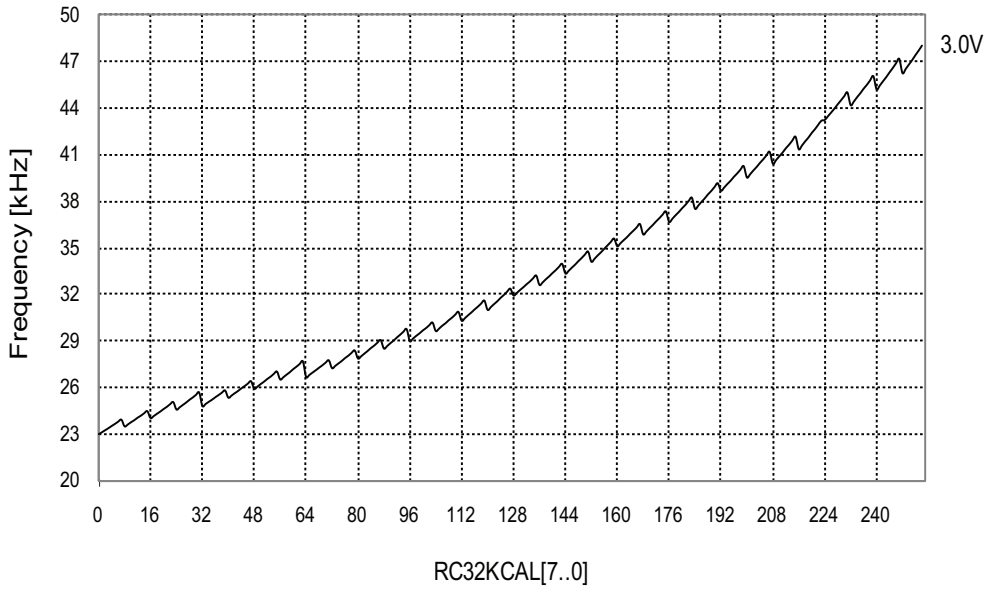


Figure 33-197. 32.768kHz Internal Oscillator Frequency vs. Calibration Value

V_{CC} = 3.0V, T = 25°C



33.3.8.3 2MHz Internal Oscillator

Figure 33-198. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled

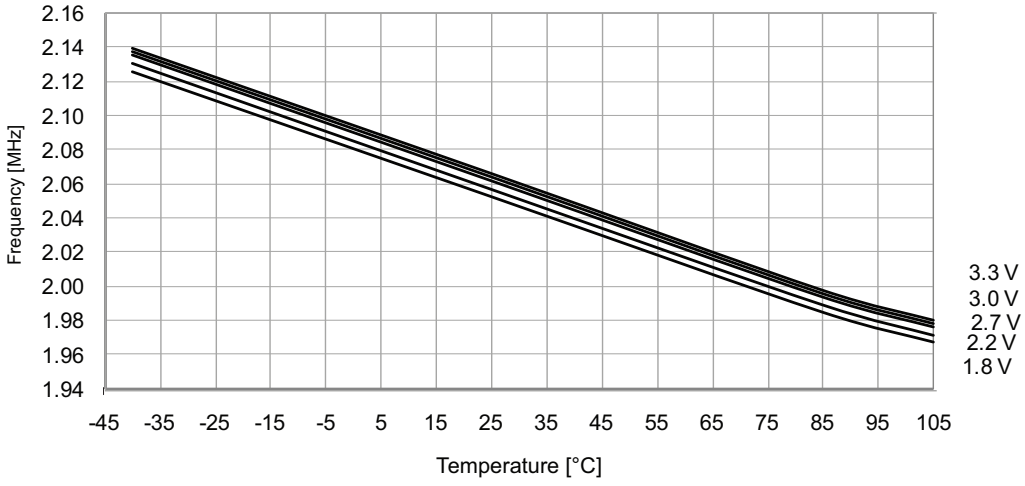


Figure 33-235.I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.3V

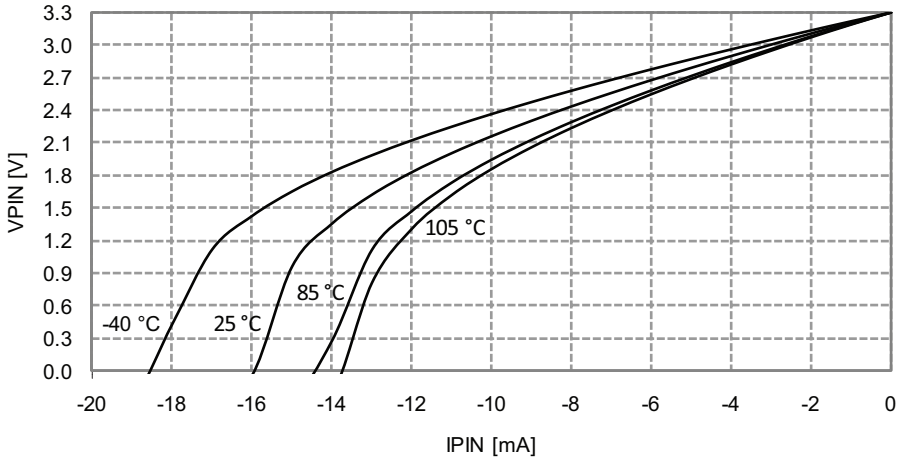


Figure 33-236.I/O Pin Output Voltage vs. Sink Current

V_{CC} = 1.8V

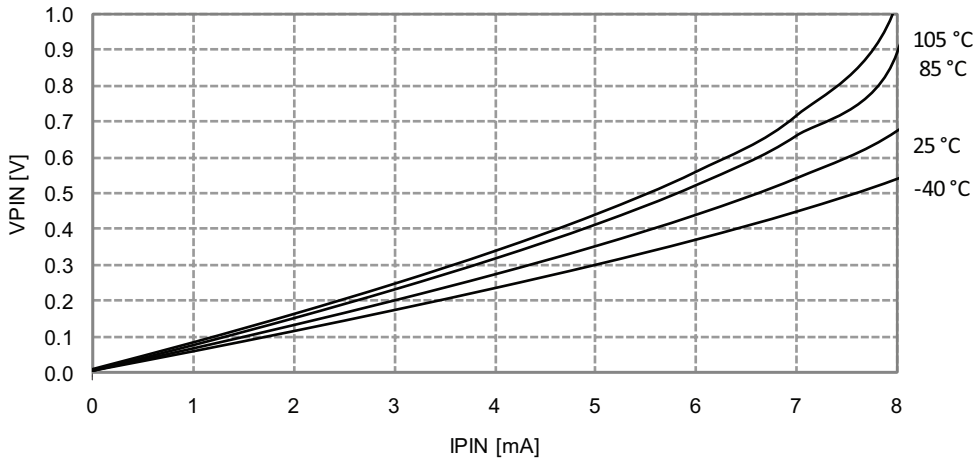


Figure 33-249.Gain Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps

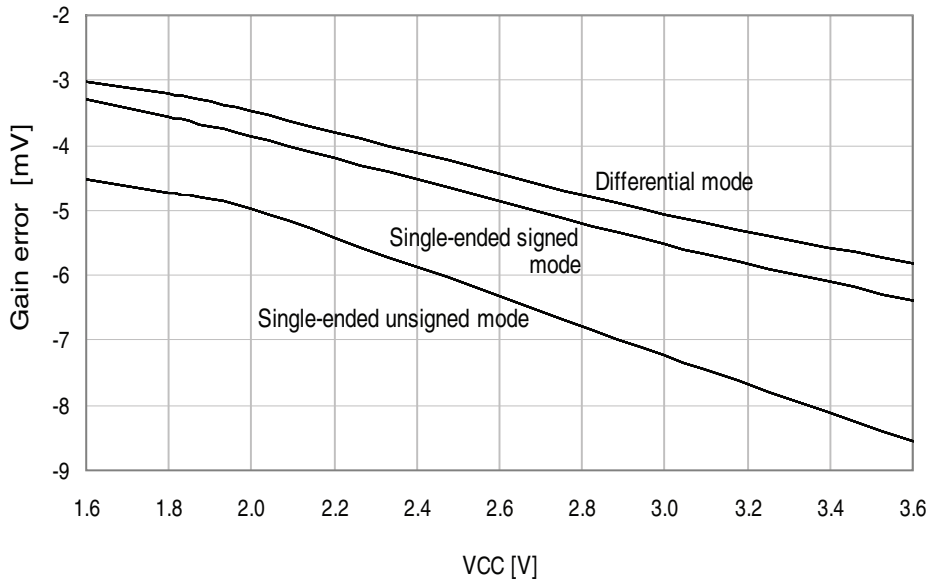


Figure 33-250.Offset Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

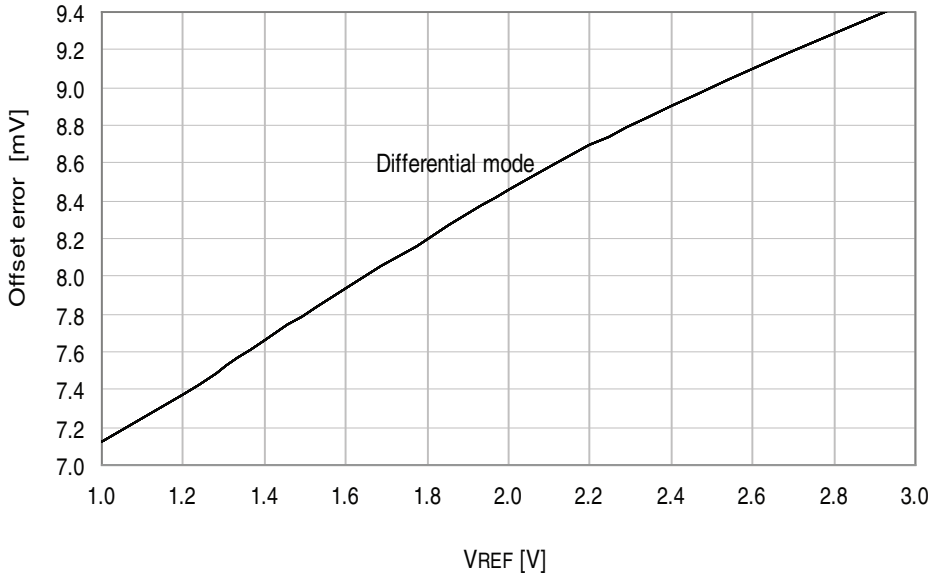


Figure 33-305.I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.3V

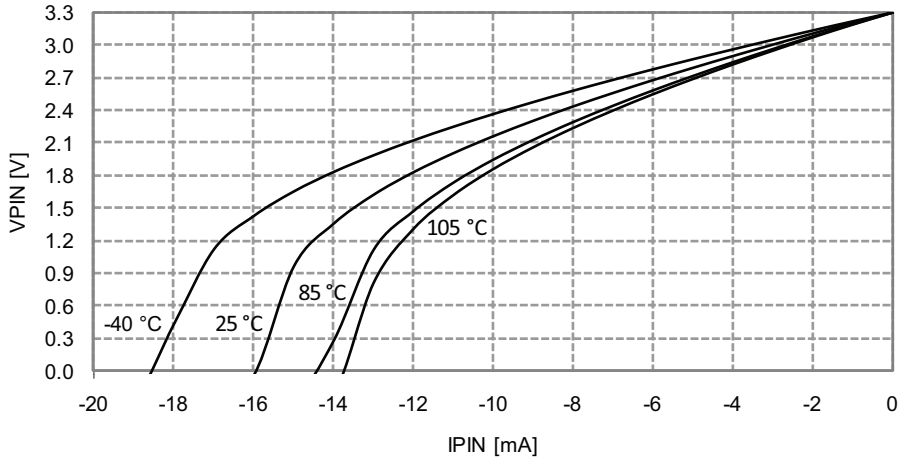
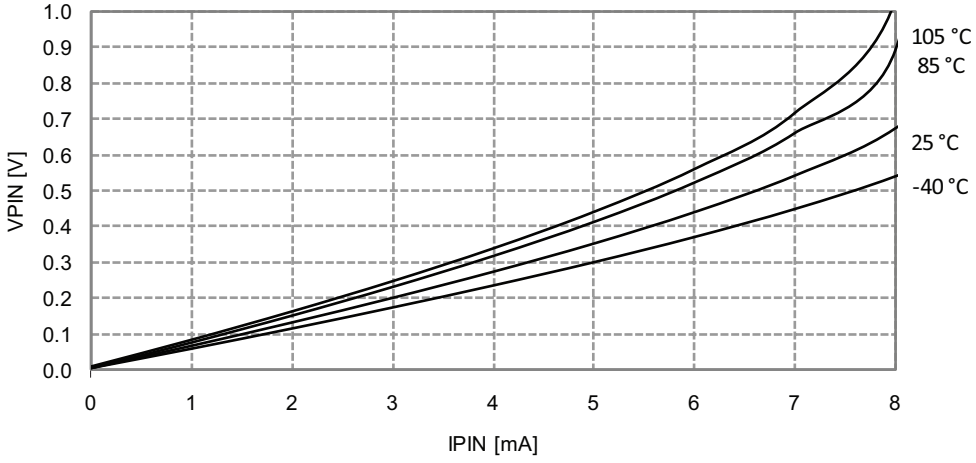


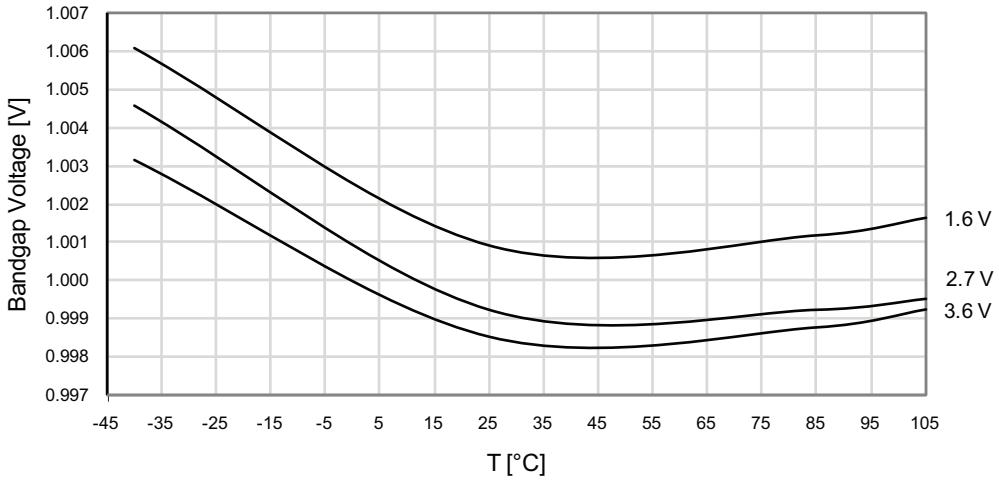
Figure 33-306.I/O Pin Output Voltage vs. Sink Current

V_{CC} = 1.8V



33.5.5 Internal 1.0V Reference Characteristics

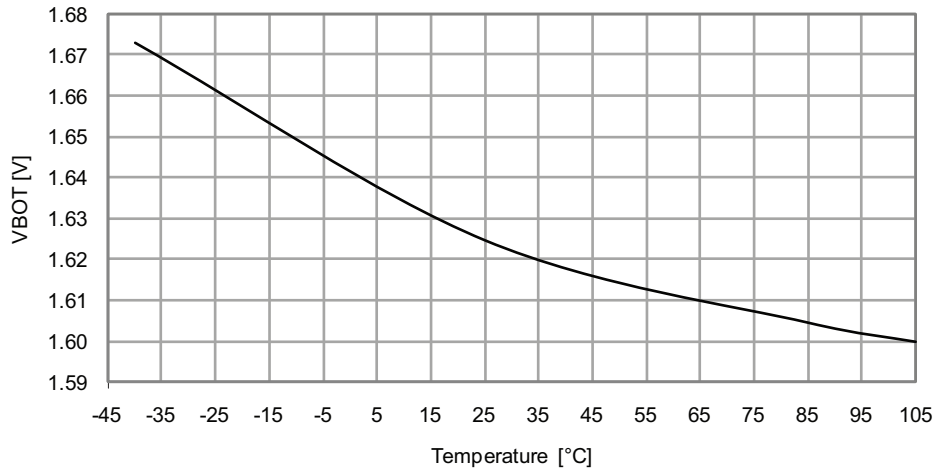
Figure 33-327. ADC Internal 1.0V Reference vs. Temperature



33.5.6 BOD Characteristics

Figure 33-328. BOD Thresholds vs. Temperature

BOD level = 1.6V



- CRC generator module
- ADC 1/2× gain option, and this configuration option in the GAIN bits in the ADC Channel CTRL register
- ADC VCC/2 reference option and this configuration option in the REFSEL bits on the ADC REFCTRL register
- ADC option to use internal Gnd as negative input in differential measurements and this configuration option in the MUXNEG bits in the ADC Channel MUXCTRL register
- ADC channel scan and the ADC SCAN register
- ADC current limitation option, and the CURRLIMIT bits in the ADC CTRLB register
- ADC impedance mode selection for the gain stage, and the IMPMODE bit in the ADC CTRLB register
- Timer/Counter 2 and the SPLITMODE configuration option in the BYTEM bits in the Timer/Counter 0 CTRLE register
- Analog Comparator (AC) current output option, and the AC CURRCTRL and CURRCALIB registers
- PORT remap functions with alternate pin locations for Timer/Counter output compare channels, USART0 and SPI, and the PORT REMAP register
- PORT RTC clock output option and the RTCOUT bit in the PORT CLKEVOUT register
- PORT remap functions with alternate pin locations for the clock and event output, and the CLKEVPIN bit in the PORT CLKEVOUT register
- TOSC alternate pin locations, and TOSCSEL bit in FUSEBYTE2
- Real Time Counter clock source options of external clock from TOSC1, and 32.768kHz from TOSC, and 32.768kHz from the 32.768kHz internal oscillator, and these configuration options in the RTCSRC bits in the Clock RTCTRL register
- PLL divide by two option, and the PLLDIV bit in the Clock PLLCTRL register
- PLL lock detection failure function and the PLLDIF and PLLFDEN bits in the Clock XOSCFAIL register
- The high drive option for external crystal and the XOSCPWR bit on the Oscillator XOSCCTRL register
- The option to enable sequential startup of the analog modules and the ANAINIT register in MCU Control memory

Problem fix/workaround

None.

26. Sampled BOD in Active mode will cause noise when bandgap is used as reference

Using the BOD in sampled mode when the device is running in Active or Idle mode will add noise on the bandgap reference for ADC, DAC and Analog Comparator.

Problem fix/workaround

If the bandgap is used as reference for either the ADC, DAC and Analog Comparator, the BOD must not be set in sampled mode.

27. Temperature sensor not calibrated

Temperature sensor factory calibration not implemented.

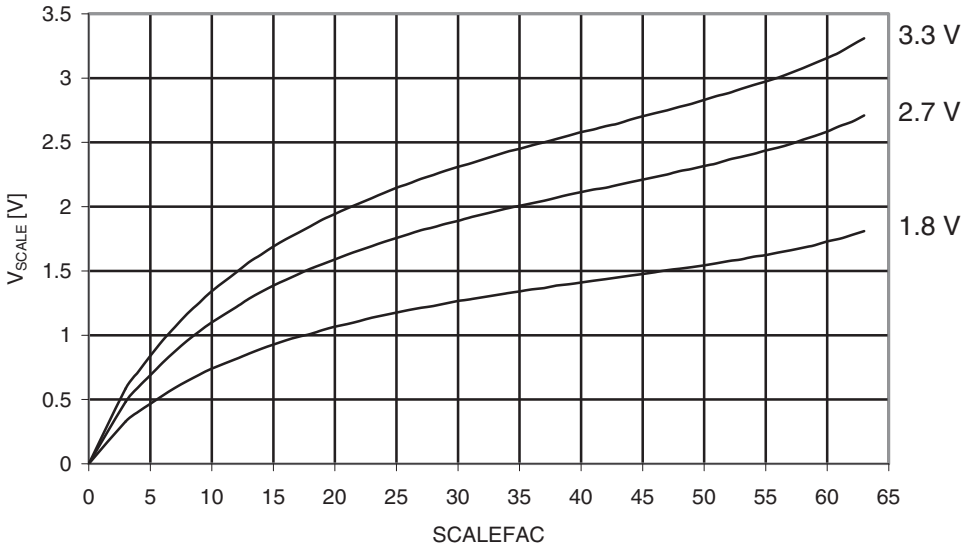
Problem fix/workaround

None.

28. Disabling of USART transmitter does not automatically set the TxD pin direction to input

If the USART transmitter is idle with no frames to transmit, setting TXEN to zero will not automatically set the TxD pin direction to input.

Figure 34-8. Analog Comparator Voltage Scaler vs. Scalefac
T = 25°C



Problem fix/workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed.

3. ADC gain stage cannot be used for single conversion

The ADC gain stage will not output correct result for single conversion that is triggered and started from software or event system.

Problem fix/workaround

When the gain stage is used, the ADC must be set in free running mode for correct results.

4. ADC has increased INL error for some operating conditions

Some ADC configurations or operating condition will result in increased INL error.

In signed mode INL is increased to:

6LSB for sample rates above 130ksps, and up to 8LSB for 200ksps sample rate.

6LSB for reference voltage below 1.1V when V_{CC} is above 3.0V.

20LSB for ambient temperature below 0°C and reference voltage below 1.3V.

In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

Problem fix/workaround

None, avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

5. ADC gain stage output range is limited to 2.4V

The amplified output of the ADC gain stage will never go above 2.4V, hence the differential input will only give correct output when below 2.4V/gain. For the available gain settings, this gives a differential input range of:

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