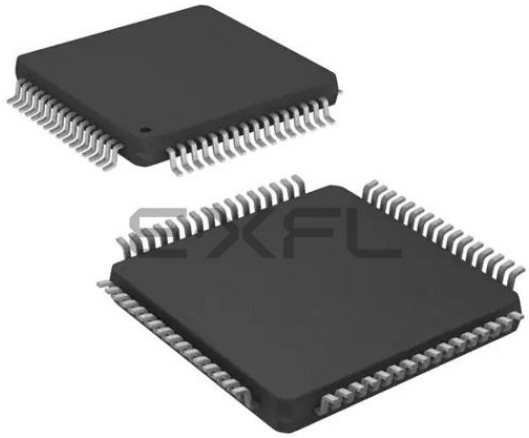

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega384d3-an

device-dependent. These two sections have separate lock bits, and can have different levels of protection. The store program memory (SPM) instruction, which is used to write to the flash from the application software, will only operate when executed from the boot loader section.

The application section contains an application table section with separate lock settings. This enables safe storage of nonvolatile data in the program memory.

Figure 7-1. Flash Program Memory (hexadecimal address)

	Word address					
ATxmega	**32D3**	**64D3**	**128D3**	**192D3**	**256D3**	**384D3**
Application section (32K/64K/128K/192K/256K/384K)	0	0	0	0	0	0
...						
	37FF	77FF	EFFF	16FFF	1EFFF	2EFFF
Application table section (4K/4K/8K/8K/8K/8K)	3800	7800	F000	17000	1F000	2F000
	3FFF	7FFF	FFFF	17FFF	1FFFF	2FFFF
Boot section (4K/4K/8K/8K/8K/8K)	4000	8000	10000	18000	20000	30000
	47FF	87FF	10FFF	18FFF	20FFF	30FFF

7.3.1 Application Section

The application section is the section of the flash that is used for storing the executable application code. The protection level for the application section can be selected by the boot lock bits for this section. The application section can not store any boot loader code since the SPM instruction cannot be executed from the application section.

7.3.2 Application Table Section

The application table section is a part of the application section of the flash memory that can be used for storing data. The size is identical to the boot loader section. The protection level for the application table section can be selected by the boot lock bits for this section. The possibilities for different protection levels on the application section and the application table section enable safe parameter storage in the program memory. If this section is not used for data, application code can reside here.

7.3.3 Boot Loader Section

While the application section is used for storing the application code, the boot loader software must be located in the boot loader section because the SPM instruction can only initiate programming when executing from this section. The SPM instruction can access the entire flash, including the boot loader section itself. The protection level for the boot loader section can be selected by the boot loader lock bits. If this section is not used for boot loader software, the application code can be stored here.

7.3.4 Production Signature Row

The production signature row is a separate memory section for factory programmed data. It contains calibration data for functions such as oscillators and analog modules. Some of the calibration values will be automatically loaded to the corresponding module or peripheral unit during reset. Other values must be loaded from the signature row and written to the corresponding peripheral registers from software. For details on calibration conditions, refer to “Electrical Characteristics” on page 63.

The production signature row also contains an ID that identifies each microcontroller device type and a serial number for each manufactured device. The serial number consists of the production lot number, wafer number, and wafer coordinates for the device. The device ID for the available devices is shown in Table 7-1 on page 15.

10. Power Management and Sleep Modes

10.1 Features

- Power management for adjusting power consumption and functions
- Five sleep modes
  - Idle
  - Power down
  - Power save
  - Standby
  - Extended standby
- Power reduction register to disable clock and turn off unused peripherals in active and idle modes

10.2 Overview

Various sleep modes and clock gating are provided in order to tailor power consumption to application requirements. This enables the Atmel AVR XMEGA microcontroller to stop unused modules to save power.

All sleep modes are available and can be entered from active mode. In active mode, the CPU is executing application code. When the device enters sleep mode, program execution is stopped and interrupts or a reset is used to wake the device again. The application code decides which sleep mode to enter and when. Interrupts from enabled peripherals and all enabled reset sources can restore the microcontroller from sleep to active mode.

In addition, power reduction registers provide a method to stop the clock to individual peripherals from software. When this is done, the current state of the peripheral is frozen, and there is no power consumption from that peripheral. This reduces the power consumption in active mode and idle sleep modes and enables much more fine-tuned power management than sleep modes alone.

10.3 Sleep Modes

Sleep modes are used to shut down modules and clock domains in the microcontroller in order to save power. XMEGA microcontrollers have five different sleep modes tuned to match the typical functional stages during application execution. A dedicated sleep instruction (SLEEP) is available to enter sleep mode. Interrupts are used to wake the device from sleep, and the available interrupt wake-up sources are dependent on the configured sleep mode. When an enabled interrupt occurs, the device will wake up and execute the interrupt service routine before continuing normal program execution from the first instruction after the SLEEP instruction. If other, higher priority interrupts are pending when the wake-up occurs, their interrupt service routines will be executed according to their priority before the interrupt service routine for the wake-up interrupt is executed. After wake-up, the CPU is halted for four cycles before execution starts.

The content of the register file, SRAM and registers are kept during sleep. If a reset occurs during sleep, the device will reset, start up, and execute from the reset vector.

10.3.1 Idle Mode

In idle mode the CPU and nonvolatile memory are stopped (note that any ongoing programming will be completed), but all peripherals, including the interrupt controller and event system are kept running. Any enabled interrupt will wake the device.

10.3.2 Power-down Mode

In power-down mode, all clocks, including the real-time counter clock source, are stopped. This allows operation only of asynchronous modules that do not require a running clock. The only interrupts that can wake up the MCU are the two-wire interface address match interrupt and asynchronous port interrupts.

28. Pinout and Pin Functions

The device pinout is shown in “Pinout/block Diagram” on page 5. In addition to general purpose I/O functionality, each pin can have several alternate functions. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the pin functions can be used at time.

28.1 Alternate Pin Function Description

The tables below show the notation for all pin functions available and describe its function.

28.1.1 Operation/power Supply

V_{CC}	Digital supply voltage
AV_{CC}	Analog supply voltage
GND	Ground

28.1.2 Port Interrupt Functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

28.1.3 Analog Functions

ACn	Analog comparator input pin n
ACnOUT	Analog comparator n output
ADCn	Analog to digital converter input pin n
A_{REF}	Analog reference input pin

28.1.4 Timer/counter and AWEX Functions

OCnxLS	Output compare channel x low side for Timer/Counter n
OCnxHS	Output compare channel x high side for Timer/Counter n

Table 32-40. Gain Stage Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode		4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode		4.4		pF
	Signal range	Gain stage output	0		AV_{CC} - 0.6	V
	Propagation delay	ADC conversion rate	1/2	1	3	Clk_{ADC} cycles
	Clock frequency	Same as ADC	100		1800	kHz
	Gain error	0.5× gain, normal mode		-1		%
		1× gain, normal mode		-1		
		8× gain, normal mode		-1		
		64× gain, normal mode		5		
	Offset error, input referred	0.5× gain, normal mode		10		mV
		1× gain, normal mode		5		
		8× gain, normal mode		-20		
		64× gain, normal mode		-126		

32.2.7 Analog Comparator Characteristics

Table 32-41. Analog Comparator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage			10		mV
I_{lk}	Input leakage current			<10	50	nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			50		µs
V_{hys1}	Hysteresis, none	V_{CC} = 1.6V - 3.6V		0		mV
V_{hys2}	Hysteresis, small	V_{CC} = 1.6V - 3.6V		15		
V_{hys3}	Hysteresis, large	V_{CC} = 1.6V - 3.6V		30		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T = 85°C		20	40	ns
		V_{CC} = 3.0V		17		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb
	Current source accuracy after calibration			5		%
	Current source calibration range	Single mode	4		6	µA

Table 32-58. Two-wire Interface Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7V_{CC}$		V_{CC} + 0.5	V
V_{IL}	Input low voltage		-0.5		$0.3V_{CC}$	
V_{hys}	Hysteresis of Schmitt trigger inputs		$0.05V_{CC}$ (1)			
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		$20 + 0.1C_b$ (1)(2)		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	10pF < C_b < 400pF (2)	$20 + 0.1C_b$ (1)(2)		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER} (3) > max(10f_{SCL}, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq$ 100kHz	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		f_{SCL} > 100kHz			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold time (repeated) START condition	$f_{SCL} \leq$ 100kHz	4.0			µs
		f_{SCL} > 100kHz	0.6			
t_{LOW}	Low period of SCL clock	$f_{SCL} \leq$ 100kHz	4.7			
		f_{SCL} > 100kHz	1.3			
t_{HIGH}	High period of SCL clock	$f_{SCL} \leq$ 100kHz	4.0			
		f_{SCL} > 100kHz	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq$ 100kHz	4.7			
		f_{SCL} > 100kHz	0.6			
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq$ 100kHz	0		3.45	µs
		f_{SCL} > 100kHz	0		0.9	
$t_{SU;DAT}$	Data setup time	$f_{SCL} \leq$ 100kHz	250			
		f_{SCL} > 100kHz	100			
$t_{SU;STO}$	Setup time for STOP condition	$f_{SCL} \leq$ 100kHz	4.0			
		f_{SCL} > 100kHz	0.6			
t_{BUF}	Bus free time between a STOP and START condition	$f_{SCL} \leq$ 100kHz	4.7			
		f_{SCL} > 100kHz	1.3			

Notes:
1. Required only for f_{SCL} > 100kHz.
2. C_b = Capacitance of one bus line in pF.
3. f_{PER} = Peripheral clock frequency.

Table 32-112.External Clock with Prescaler [1] for System Clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency [2]	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	4.5			
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes:
1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

32.4.13.7 External 16MHz Crystal Oscillator and XOSC Characteristics

Table 32-113. External 16MHz Crystal Oscillator and XOSC Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0		0		ns
			FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1			0		
	Long term jitter	XOSCPWR=0	FRQRANGE=0		0		
			FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1			0		
	Frequency error	XOSCPWR=0	FRQRANGE=0		0.03		%
			FRQRANGE=1		0.03		
			FRQRANGE=2 or 3		0.03		
		XOSCPWR=1			0.003		
	Duty cycle	XOSCPWR=0	FRQRANGE=0		50		
			FRQRANGE=1		50		
			FRQRANGE=2 or 3		50		
		XOSCPWR=1			50		

32.6.3 Current Consumption

Table 32-149. Current Consumption for Active Mode and Sleep Modes

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		150		µA
			V_{CC} = 3.0V		320		
		1MHz, Ext. Clk	V_{CC} = 1.8V		410		
			V_{CC} = 3.0V		830		
		2MHz, Ext. Clk	V_{CC} = 1.8V		660	800	
			V_{CC} = 3.0V		1.3	1.8	mA
		32MHz, Ext. Clk			10	15	
	Idle power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		4		µA
			V_{CC} = 3.0V		5		
		1MHz, Ext. Clk	V_{CC} = 1.8V		50		
			V_{CC} = 3.0V		100		
		2MHz, Ext. Clk	V_{CC} = 1.8V		100	350	
			V_{CC} = 3.0V		200	600	
		32MHz, Ext. Clk			3.3	7	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.2	1.0	µA
		T = 85°C			3.5	6.0	
		T = 105°C			15	20	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.5	2.0	
		WDT and sampled BOD enabled, T = 85°C			6.0	10	
		WDT and sampled BOD enabled, T= 105°C			16	27	
	Power-save power consumption (2)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.4		
			V_{CC} = 3.0V		1.5		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.7	2	
			V_{CC} = 3.0V		0.8	2	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.9	3	
			V_{CC} = 3.0V		1.1	3	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		300		

Notes: 1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

Figure 33-5. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator

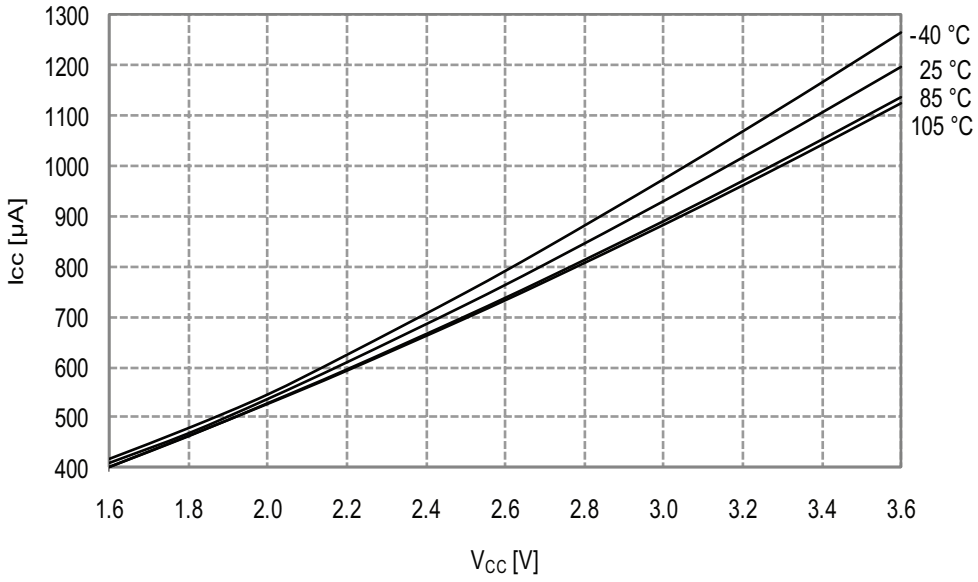


Figure 33-6. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz

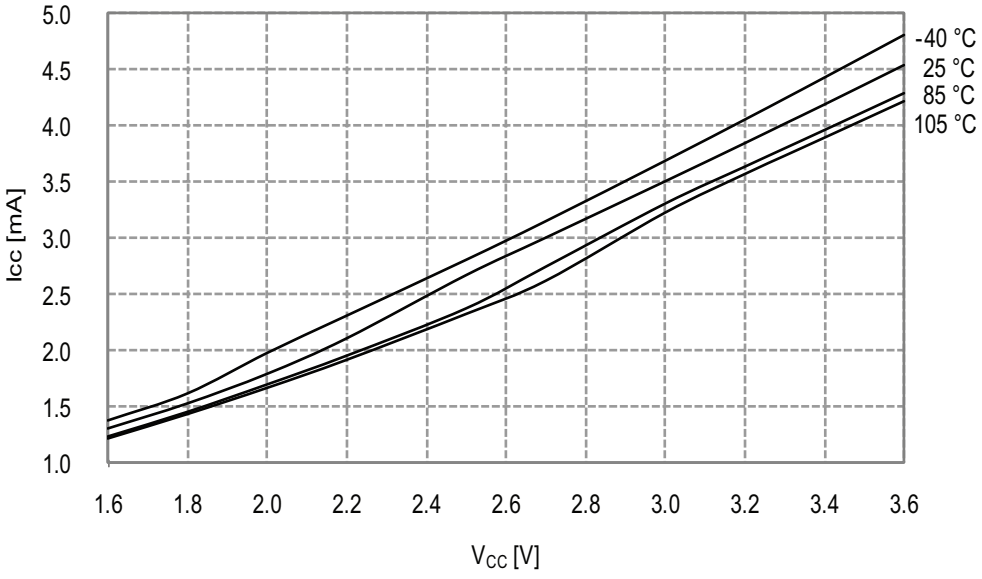
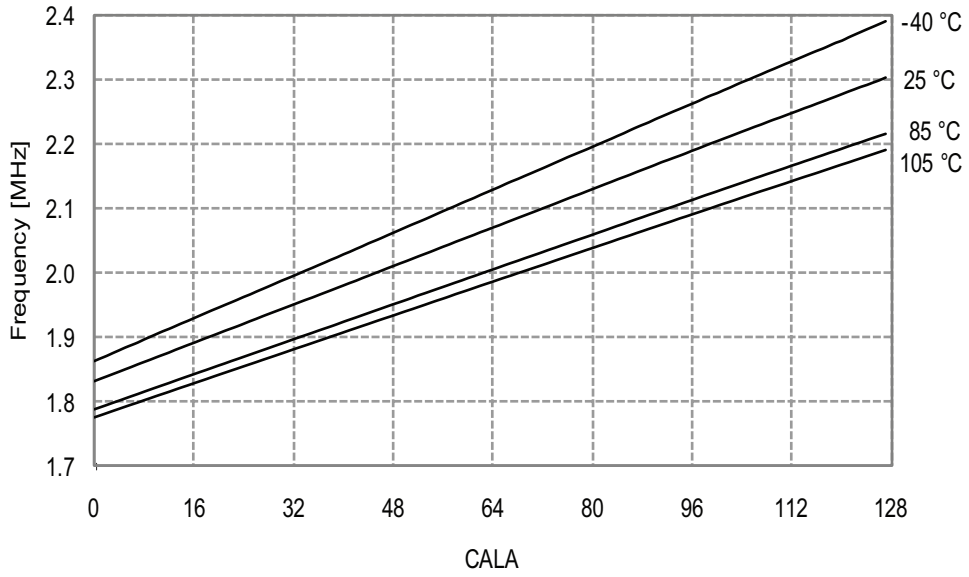


Figure 33-59. 2MHz Internal Oscillator Frequency vs. CALA Calibration Value

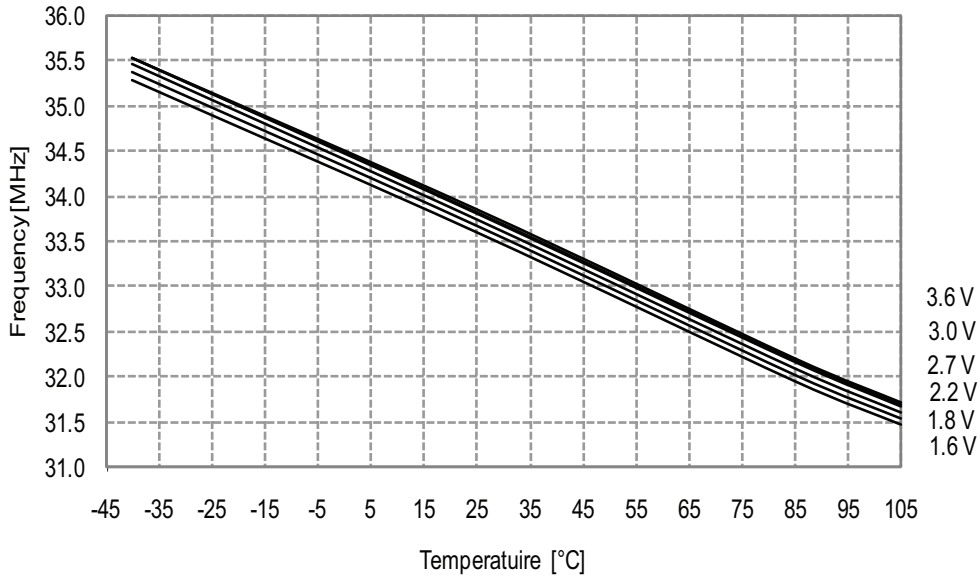
V_{CC} = 3V



33.1.8.4 32MHz Internal Oscillator

Figure 33-60. 32MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled



33.2.8.3 2MHz Internal Oscillator

Figure 33-128. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled

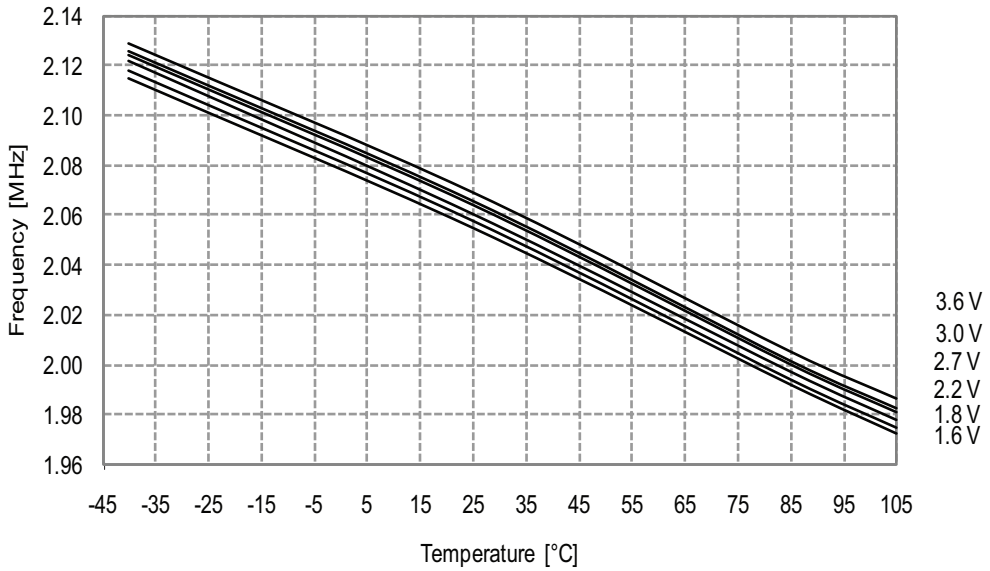


Figure 33-129. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator

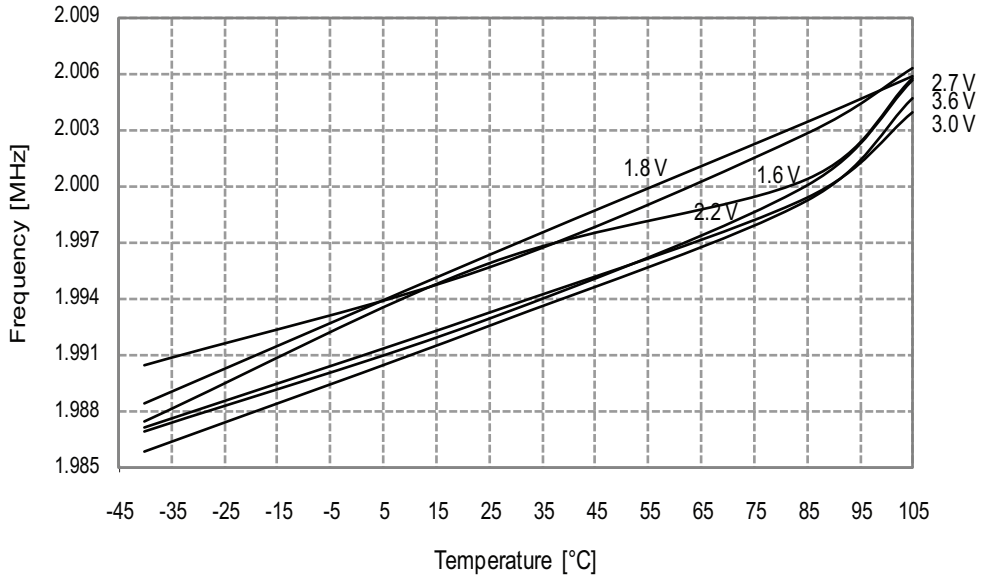
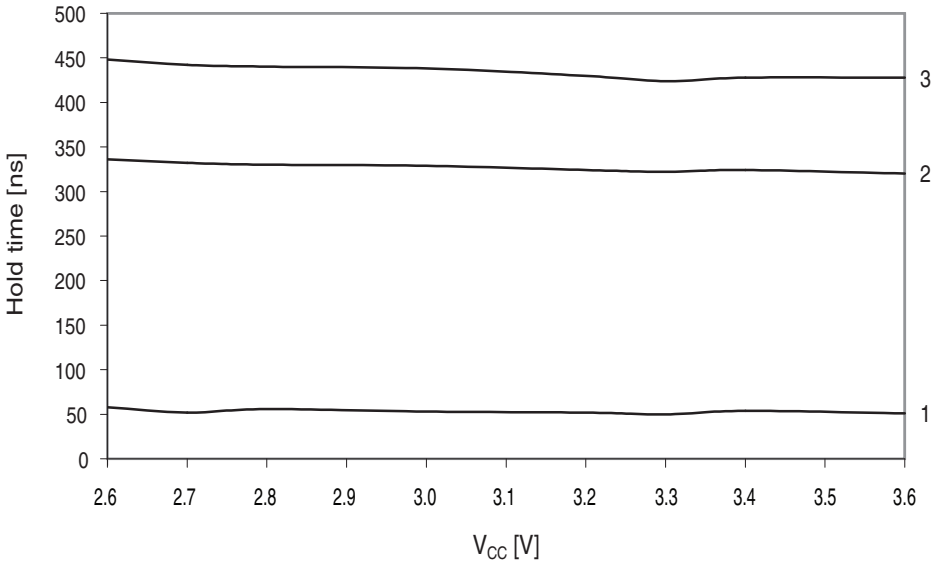
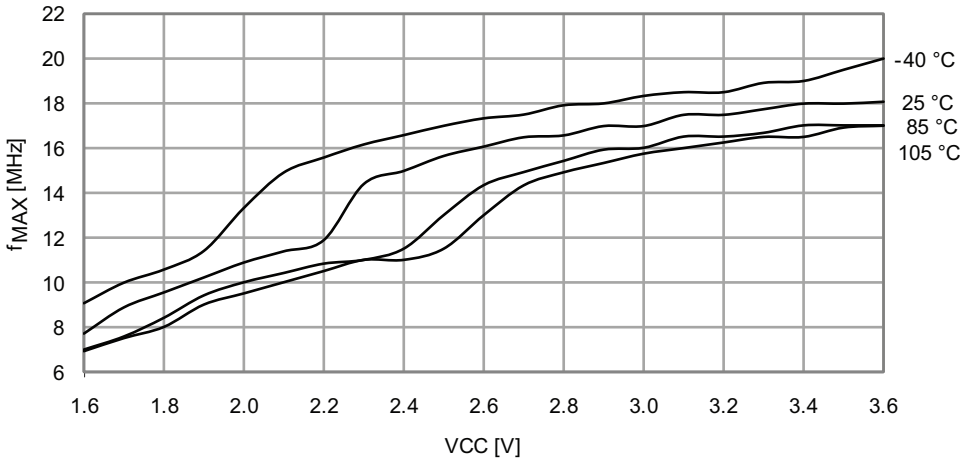


Figure 33-211. SDA Hold Time vs. Supply Voltage



33.3.10 PDI Characteristics

Figure 33-212. Maximum PDI Frequency vs. V_{CC}



33.4 Atmel ATxmega192D3

33.4.1 Current Consumption

33.4.1.1 Active Mode Supply Current

Figure 33-213.Active Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C

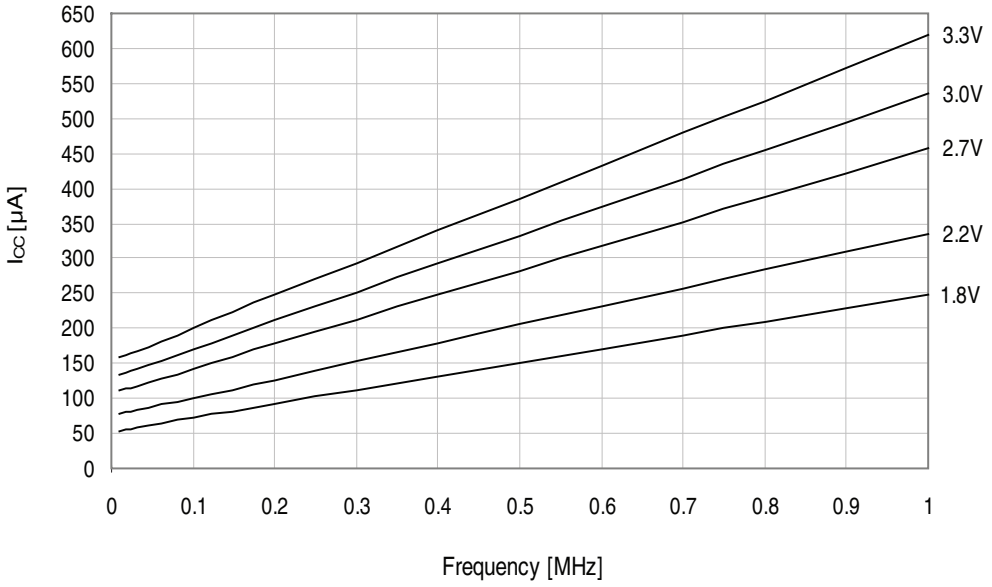


Figure 33-214.Active Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C

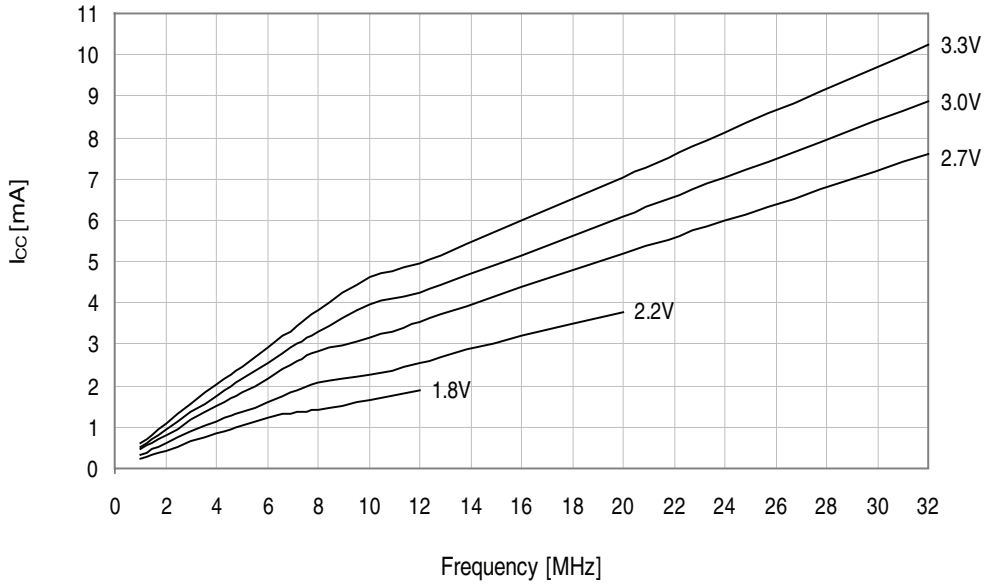
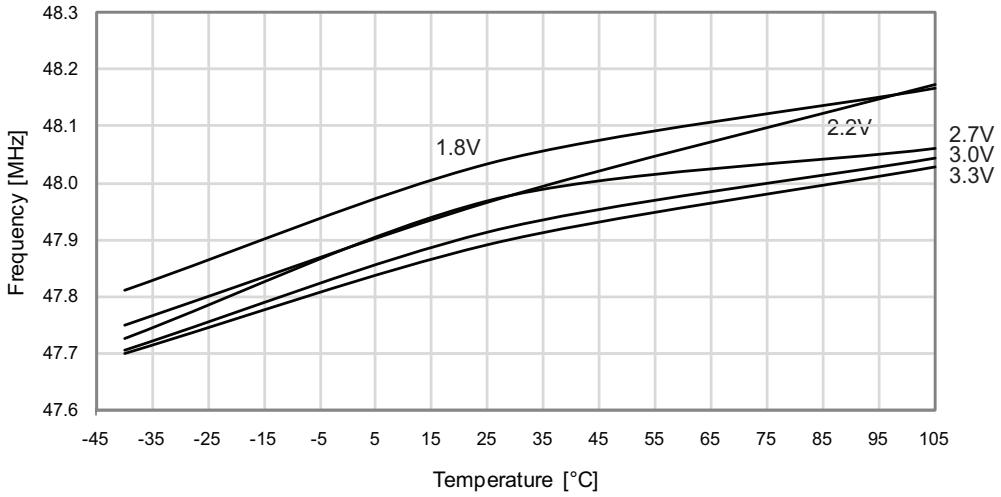


Figure 33-279. 48MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator



33.4.9 Two-Wire Interface Characteristics

Figure 33-280.SDA Hold Time vs. Temperature

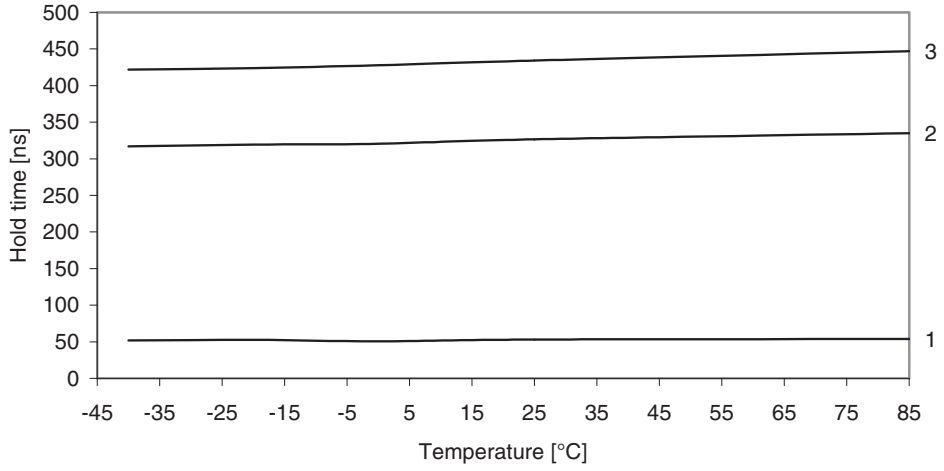


Figure 33-333. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 3.3V

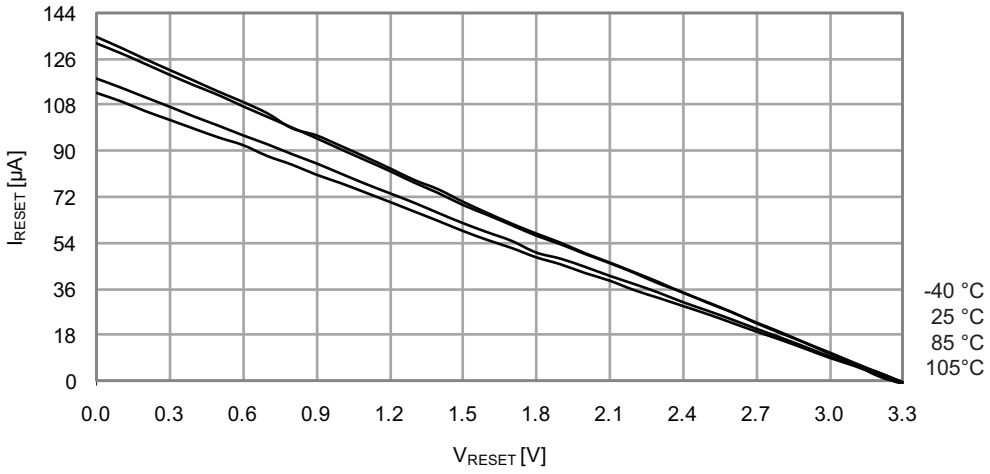


Figure 33-334. Reset Pin Input Threshold Voltage vs. V_{CC}

V_{IH} - Reset pin read as "1"

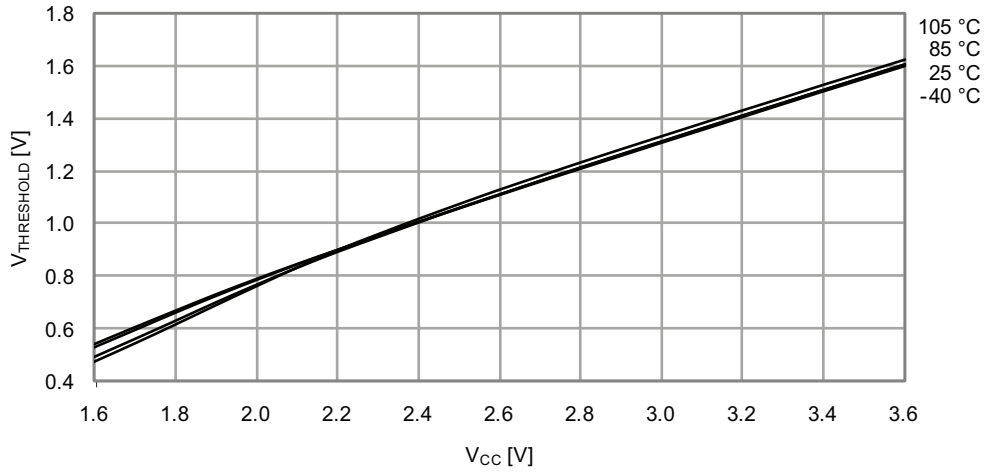


Figure 33-345. 32MHz Internal Oscillator CALA Calibration Step Size

T = 85°C, V_{CC} = 3.0V

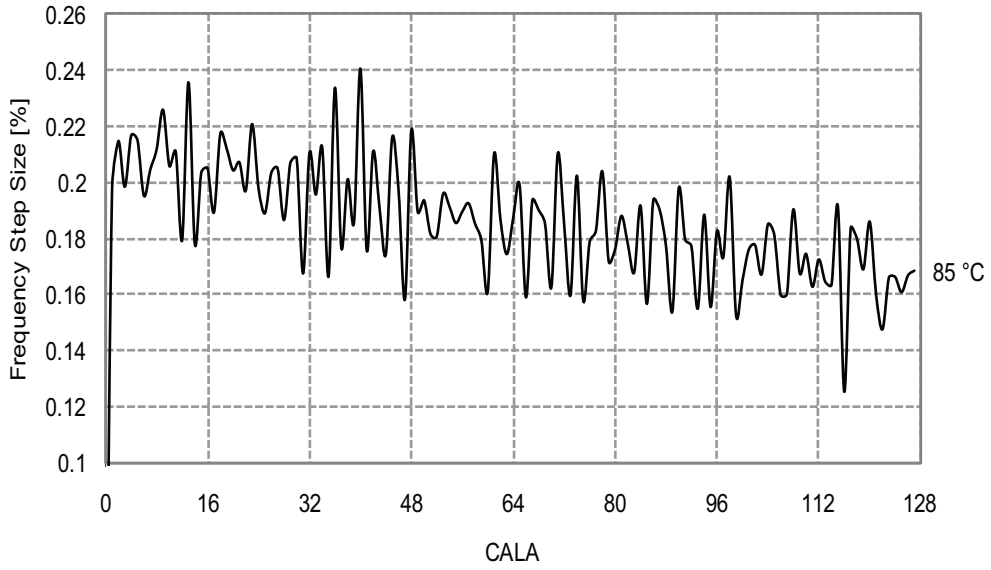


Figure 33-346. 32MHz Internal Oscillator CALA Calibration Step Size

T = 105°C, V_{CC} = 3.0V

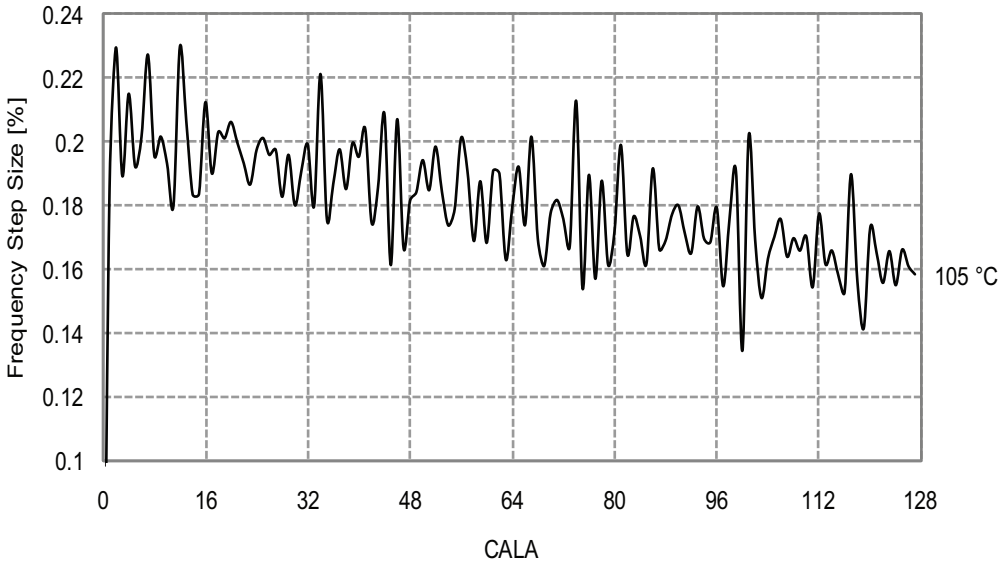


Figure 33-403. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 3.3V

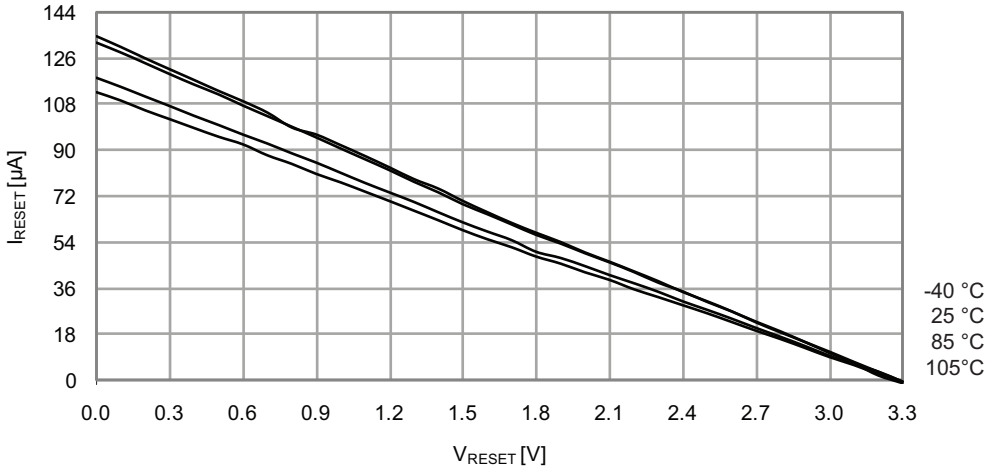
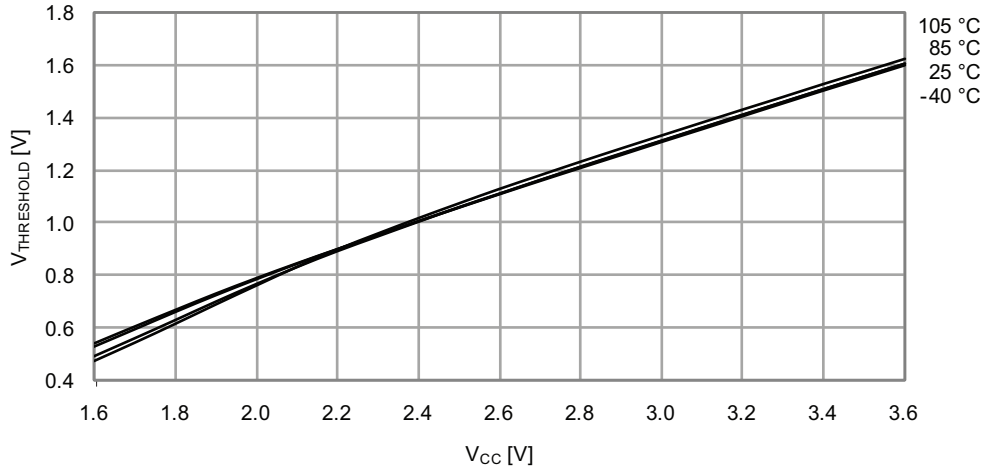


Figure 33-404. Reset Pin Input Threshold Voltage vs. V_{CC}

V_{IH} - Reset pin read as "1"



33.6.8.5 32MHz Internal Oscillator Calibrated to 48MHz

Figure 33-415. 48MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled

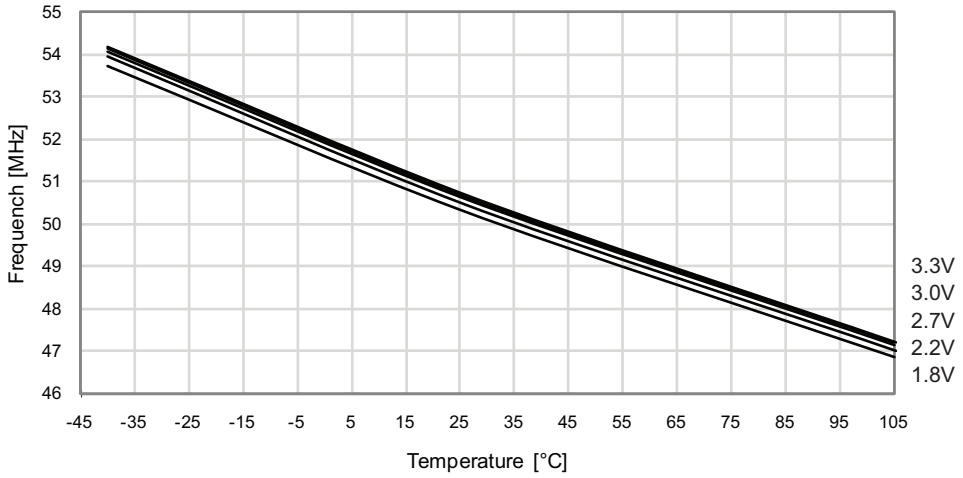
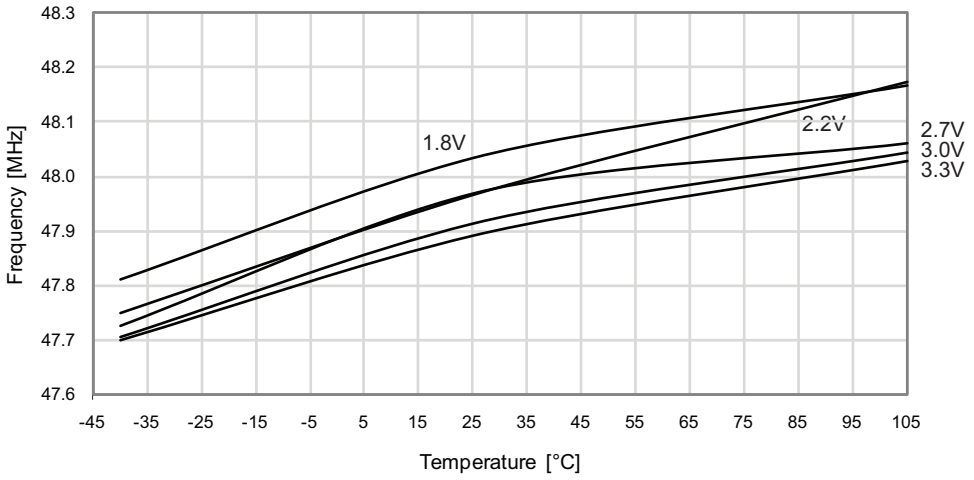


Figure 33-416. 48MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator



Problem fix/workaround

Table 34-3. Configure PWM and CWCM According to this Table:

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

11. PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

Problem fix/workaround

Do a write to any AWeX I/O register to re-enable the output.

12. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the V_{CC} voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until V_{CC} is above the programmed BOD level even if the BOD is disabled.

Problem fix/workaround

Do not set the BOD level higher than V_{CC} even if the BOD is not used.

13. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

14. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/workaround

None.

15. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

Problem fix/workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (that is, connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

16. NMI Flag for Crystal Oscillator Failure automatically cleared

NMI flag for Crystal Oscillator Failure (XOSCFDIF) will be automatically cleared when executing the NMI interrupt handler.

Problem fix/workaround

This device revision has only one NMI interrupt source, so checking the interrupt source in software is not required.

17. RTC Counter value not correctly read after sleep

If the RTC is set to wake up the device on RTC Overflow and bit 0 of RTC CNT is identical to bit 0 of RTC PER as the device is entering sleep, the value in the RTC count register can not be read correctly within the first prescaled RTC clock cycle after wake-up. The value read will be the same as the value in the register when entering sleep.

The same applies if RTC Compare Match is used as wake-up source.

Problem fix/workaround

Wait at least one prescaled RTC clock cycle before reading the RTC CNT value.

18. Pending asynchronous RTC-interrupts will not wake up device

Asynchronous Interrupts from the Real-Time-Counter that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again.

Problem fix/workaround

None.

19. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/workaround

Clear the flag in software after address interrupt.

20. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
       ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc)) &&
         /* SCL not held by slave: */
         !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
```

- 1× gain: 2.4 V
- 2× gain: 1.2 V
- 4× gain: 0.6 V
- 8× gain: 300 mV
- 16× gain: 150 mV
- 32× gain: 75 mV
- 64× gain: 38 mV

Problem fix/workaround

Keep the amplified voltage output from the ADC gain stage below 2.4V in order to get a correct result, or keep ADC voltage reference below 2.4V.

6. ADC Event on compare match non-functional

ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

Problem fix/workaround

Enable and use interrupt on compare match when using the compare function.

7. ADC propagation delay is not correct when 8× – 64× gain is used

The propagation delay will increase by only one ADC clock cycle for all gain settings.

Problem fix/workaround

None.

8. Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V

The ADC can not be used to do bandgap measurements when V_{CC} is below 2.7V.

Problem fix/workaround

None.

9. Accuracy lost on first three samples after switching input to ADC gain stage

Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

Problem fix/workaround

Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

10. Configuration of PGM and CWCM not as described in XMEGA D Manual

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.