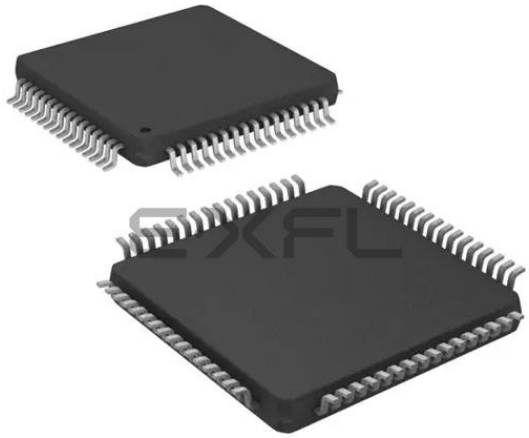

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64d3-anr

10.3.3 Power-save Mode

Power-save mode is identical to power down, with one exception. If the real-time counter (RTC) is enabled, it will keep running during sleep, and the device can also wake up from either an RTC overflow or compare match interrupt.

10.3.4 Standby Mode

Standby mode is identical to power down, with the exception that the enabled system clock sources are kept running while the CPU, peripheral, and RTC clocks are stopped. This reduces the wake-up time.

10.3.5 Extended Standby Mode

Extended standby mode is identical to power-save mode, with the exception that the enabled system clock sources are kept running while the CPU and peripheral clocks are stopped. This reduces the wake-up time.

24. CRC – Cyclic Redundancy Check generator

24.1 Features

- Cyclic redundancy check (CRC) generation and checking for
  - Communication data
  - Program or data in flash memory
  - Data in SRAM and I/O memory space
- Integrated with flash memory and CPU
  - Automatic CRC of the complete or a selectable range of the flash memory
  - CPU can load data to the CRC generator through the I/O interface
- CRC polynomial software selectable to
  - CRC-16 (CRC-CCITT)
  - CRC-32 (IEEE 802.3)
- Zero remainder detection

24.2 Overview

A cyclic redundancy check (CRC) is an error detection technique test algorithm used to find accidental errors in data, and it is commonly used to determine the correctness of a data transmission, and data present in the data and program memories. A CRC takes a data stream or a block of data as input and generates a 16- or 32-bit output that can be appended to the data and used as a checksum. When the same data are later received or read, the device or application repeats the calculation. If the new CRC result does not match the one calculated earlier, the block contains a data error. The application will then detect this and may take a corrective action, such as requesting the data to be sent again or simply not using the incorrect data.

Typically, an n-bit CRC applied to a data block of arbitrary length will detect any single error burst not longer than n bits (any single alteration that spans no more than n bits of the data), and will detect the fraction $1-2^{-n}$ of all longer error bursts. The CRC module in Atmel AVR XMEGA devices supports two commonly used CRC polynomials; CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3).

CRC-16:

Polynominal: $x^{16}+x^{12}+x^{5}+1$

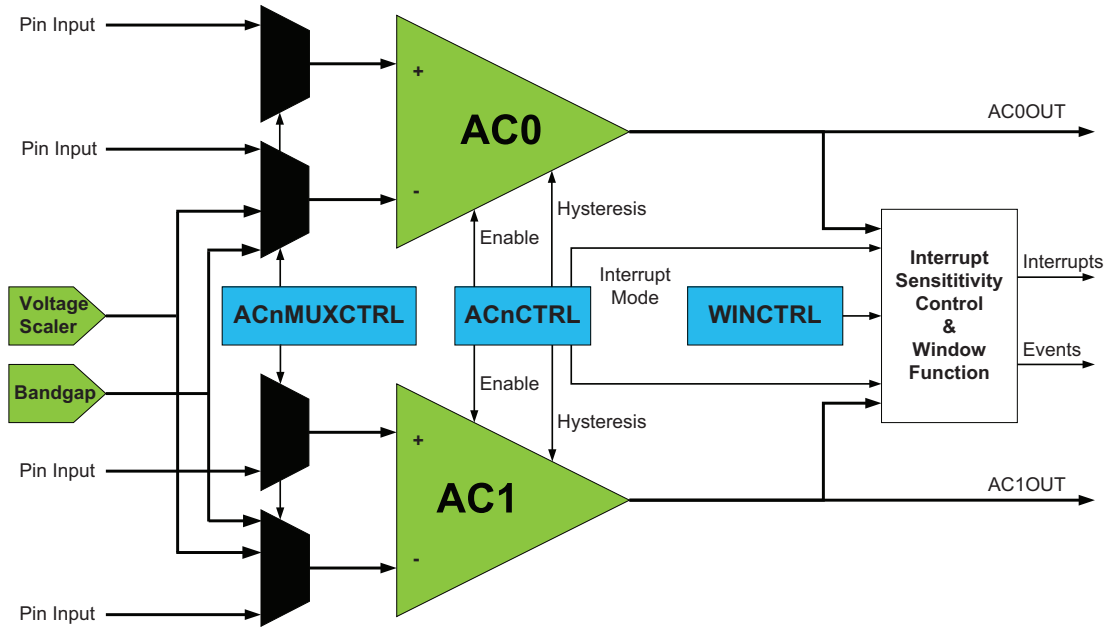
Hex value: 0x1021

CRC-32:

Polynominal: $x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+x+1$

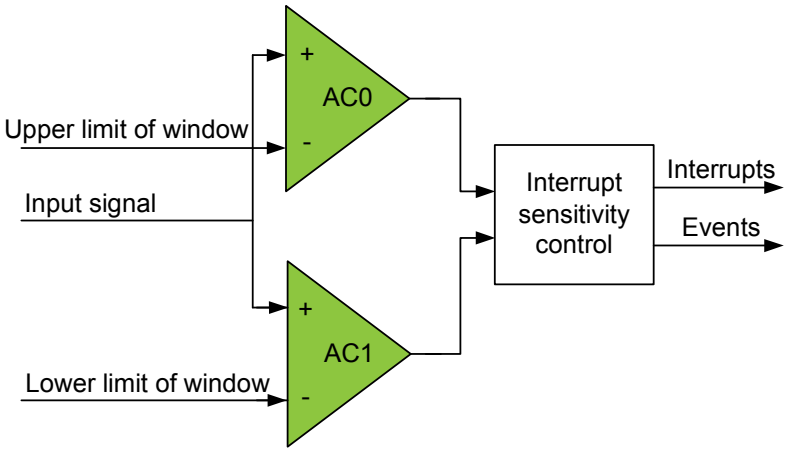
Hex value: 0x04C11DB7

Figure 26-1. Analog Comparator Overview



The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in Figure 26-2.

Figure 26-2. Analog Comparator Window Function



29. Peripheral Module Address Map

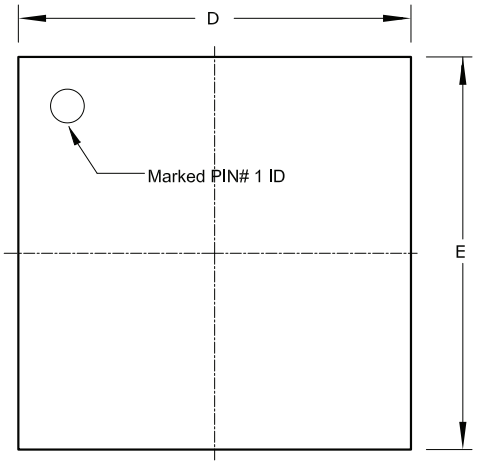
The address maps show the base address for each peripheral and module in Atmel AVR XMEGA D3. For complete register description and summary for each peripheral module, refer to the XMEGA D manual.

Table 29-1. Peripheral Module Address Map

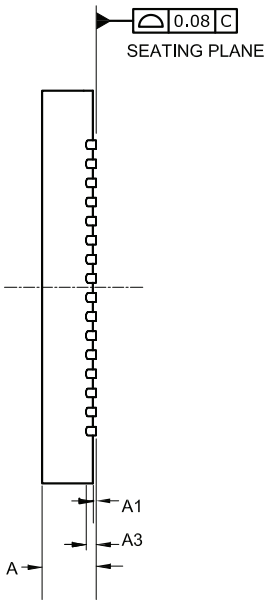
Base address	Name	Description
0x0000	GPIO	General Purpose IO Registers
0x0010	VPORT0	Virtual Port 0
0x0014	VPORT1	Virtual Port 1
0x0018	VPORT2	Virtual Port 2
0x001C	VPORT3	Virtual Port 2
0x0030	CPU	CPU
0x0040	CLK	Clock Control
0x0048	SLEEP	Sleep Controller
0x0050	OSC	Oscillator Control
0x0060	DFLLRC32M	DFLL for the 32MHz Internal Oscillator
0x0068	DFLLRC2M	DFLL for the 2MHz Internal Oscillator
0x0070	PR	Power Reduction
0x0078	RST	Reset Controller
0x0080	WDT	Watchdog Timer
0x0090	MCU	MCU Control
0x00A0	PMIC	Programmable Multilevel Interrupt Controller
0x00B0	PORTCFG	Port Configuration
0x0180	EVSYS	Event System
0x00D0	CRC	CRC Module
0x01C0	NVM	Non Volatile Memory (NVM) Controller
0x0200	ADCA	Analog to Digital Converter on port A
0x0380	ACA	Analog Comparator pair on port A
0x0400	RTC	Real-Time Counter
0x0480	TWIC	Two-Wire Interface on port C
0x04A0	TWIE	Two-Wire Interface on port E
0x0600	PORTA	Port A
0x0620	PORTB	Port B
0x0640	PORTC	Port C

31.2 64M

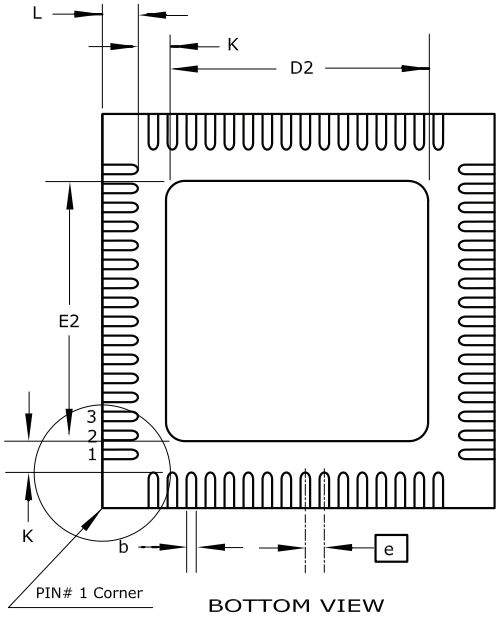
DRAWINGS NOT SCALED



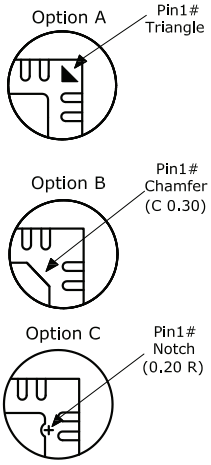
TOP VIEW



SIDE VIEW



BOTTOM VIEW



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	----	----	1.00	
A1	----	0.02	0.05	
A3		0.20 REF		
D/E	8.90	9.00	9.10	
D2/E2	7.50	7.65	7.80	
L	0.35	0.40	0.45	
K	0.20	0.27	0.40	
b	0.18	----	0.30	2
e		0.50 BSC		
n		64		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VMMD for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

12/18/2012

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact: packagedrawings@atmel.com**	PP, 64 Lds - 0.50mm Pitch, 9x9x1mm Body size Very Thin Quad Flat Package (VQFN) Sawn	ZFF	PP	A

32.3.3 Current Consumption

Table 32-62. Current Consumption for Active Mode and Sleep Modes

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		55		µA
			V_{CC} = 3.0V		135		
		1MHz, Ext. Clk	V_{CC} = 1.8V		237		
			V_{CC} = 3.0V		515		
		2MHz, Ext. Clk	V_{CC} = 1.8V		425	700	
			V_{CC} = 3.0V		0.9	1.5	mA
		32MHz, Ext. Clk			8.3	12	
	Idle power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		2.8		µA
			V_{CC} = 3.0V		3.1		
		1MHz, Ext. Clk	V_{CC} = 1.8V		47		
			V_{CC} = 3.0V		95		
		2MHz, Ext. Clk	V_{CC} = 1.8V		94	200	
			V_{CC} = 3.0V		190	400	
		32MHz, Ext. Clk			3.0	7.0	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			1.9	4.0	
		T = 105°C			4.0	8.0	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.5	2.0	
		WDT and sampled BOD enabled, T = 85°C			3.0	8.0	
		WDT and sampled BOD enabled, T= 105°C			5.0	10	
	Power-save power consumption (2)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.3		
			V_{CC} = 3.0V		1.4		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.7	2.0	
			V_{CC} = 3.0V		0.8	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.9	3.0	
			V_{CC} = 3.0V		1.1	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		145		

Notes: 1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

32.6.13 Clock and Oscillator Characteristics

32.6.13.1 Calibrated 32.768kHz Internal Oscillator Characteristics

Table 32-164. 32.768kHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

32.6.13.2 Calibrated 2MHz RC Internal Oscillator Characteristics

Table 32-165. 2MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8		2.2	MHz
	Factory calibrated frequency			2.0		
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration stepsize			0.23		

32.6.13.3 Calibrated 32MHz Internal Oscillator Characteristics

Table 32-166. 32MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30	32	35	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration step size			0.24		

32.6.13.4 32kHz Internal ULP Oscillator Characteristics

Table 32-167. 32kHz Internal ULP Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			26		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-12		12	%
	Accuracy		-30		30	

Figure 33-5. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator

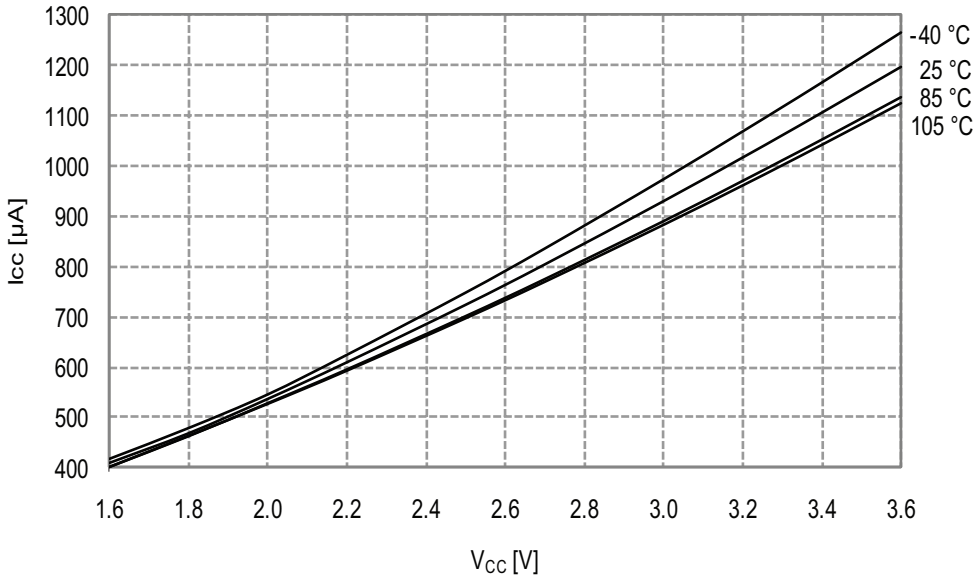


Figure 33-6. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz

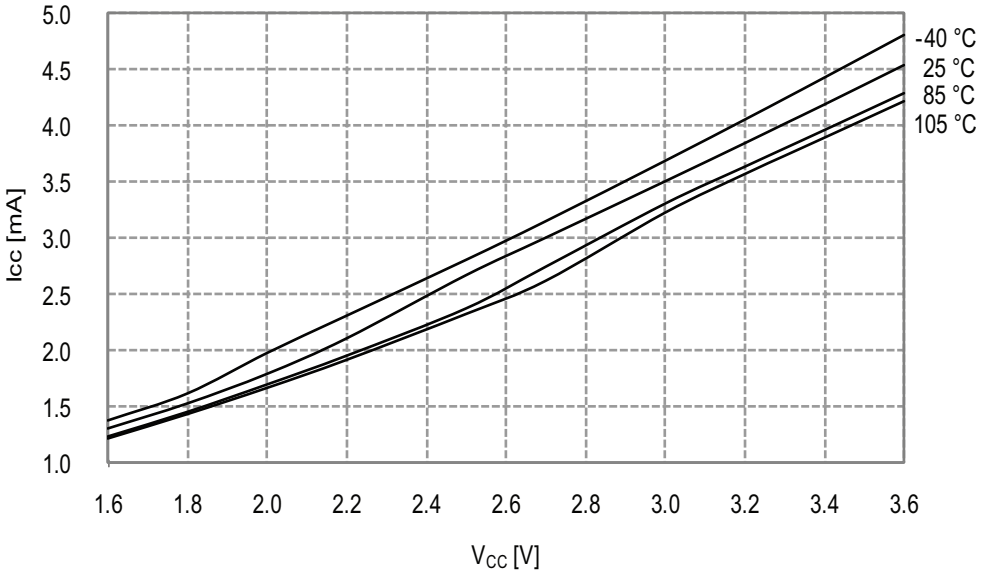


Figure 33-39. Offset error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps.

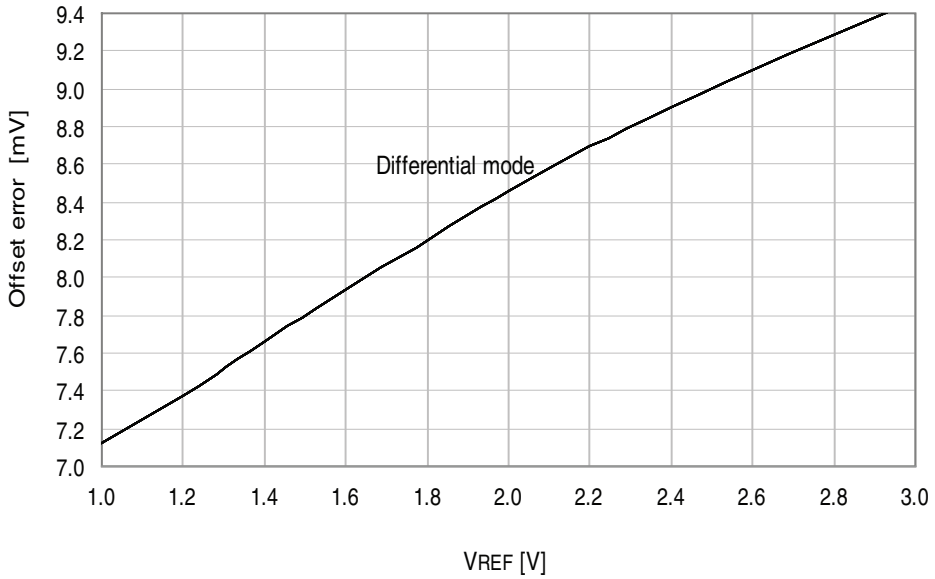


Figure 33-40. Gain Error vs. Temperature

V_{CC} = 3.0V, V_{REF} = external 2.0V

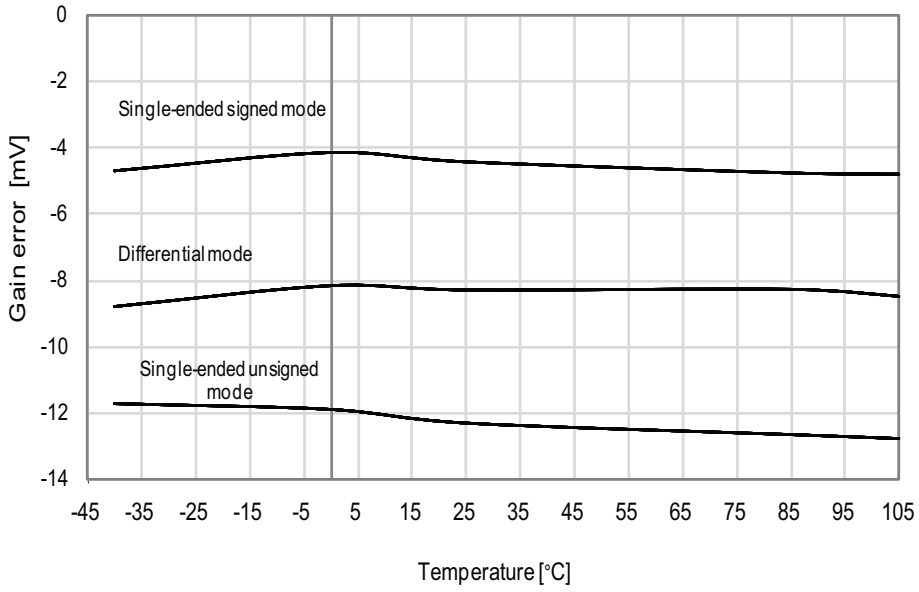


Figure 33-84. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz

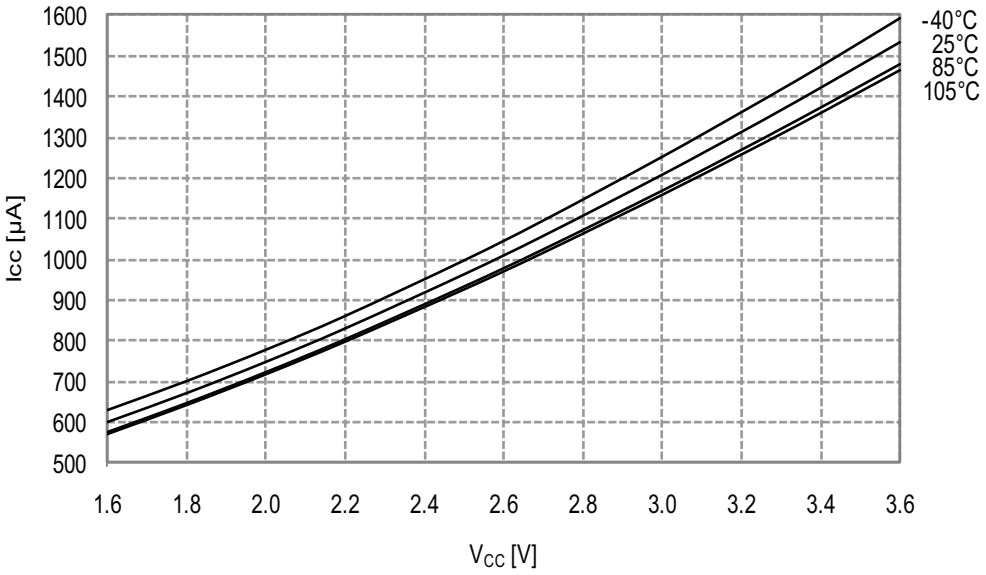


Figure 33-85. Idle Mode Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator

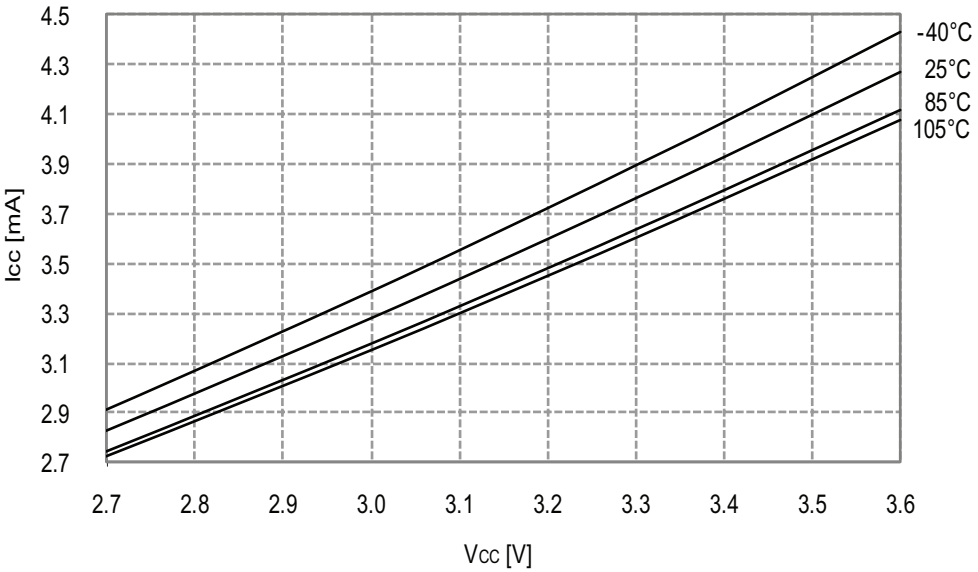


Figure 33-94. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.0V

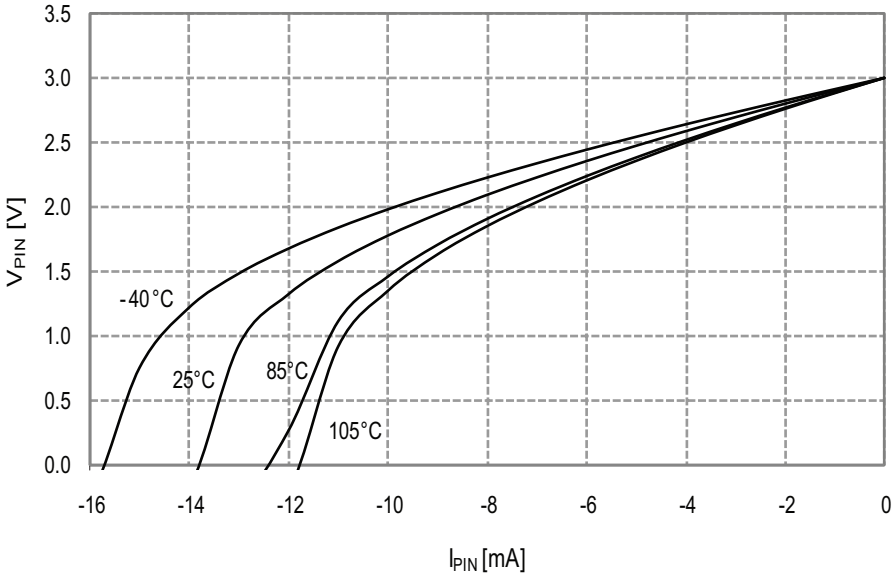


Figure 33-95. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.3V

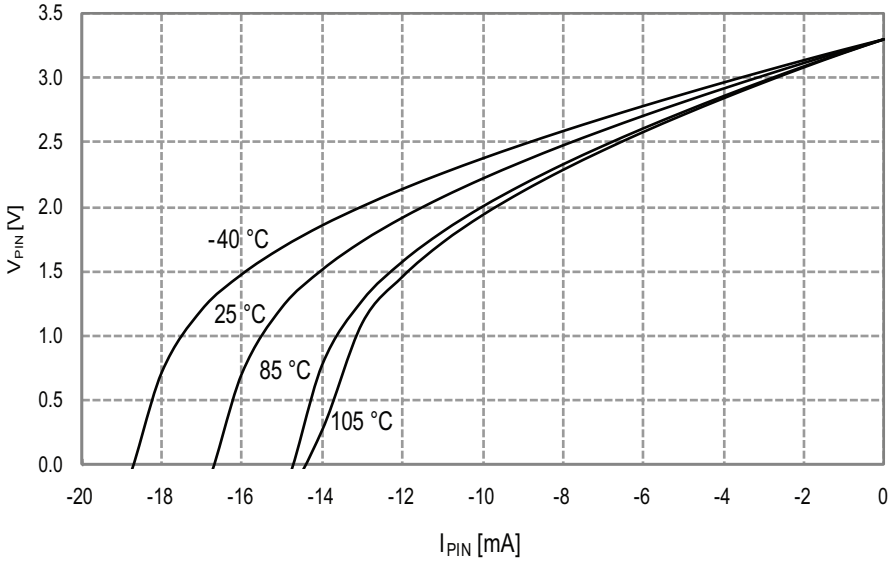
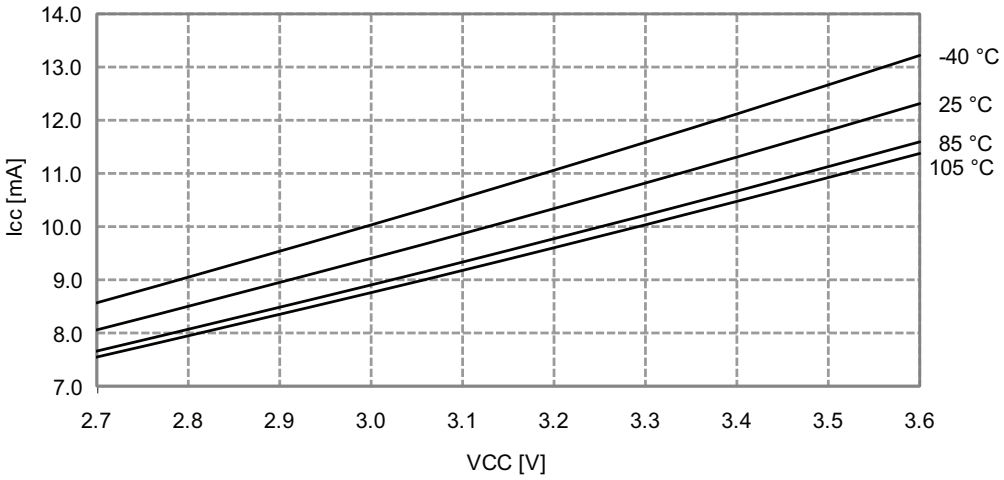


Figure 33-219.Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator



33.4.1.2 Idle Mode Supply Current

Figure 33-220.Idle Mode Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C

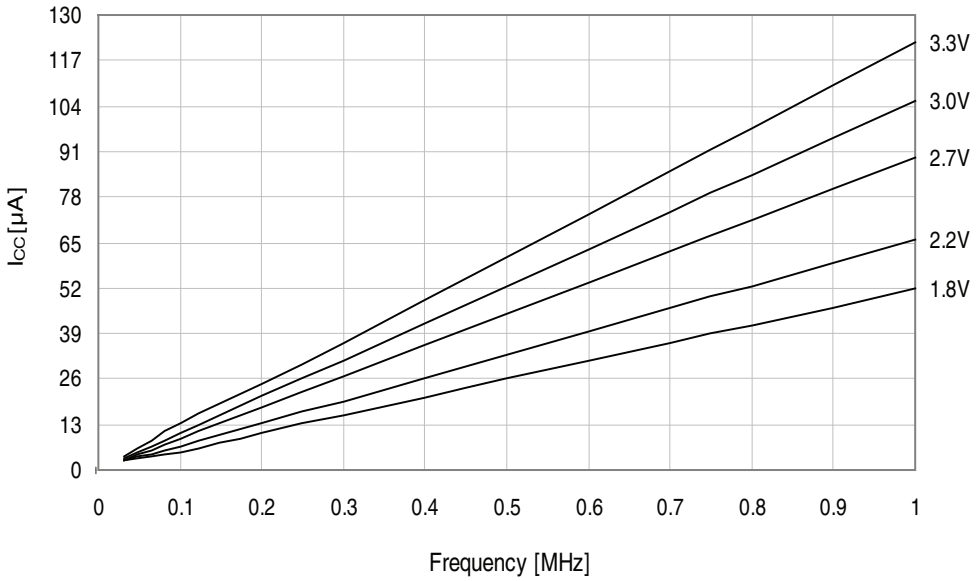


Figure 33-247.DNL Error vs. Input Code

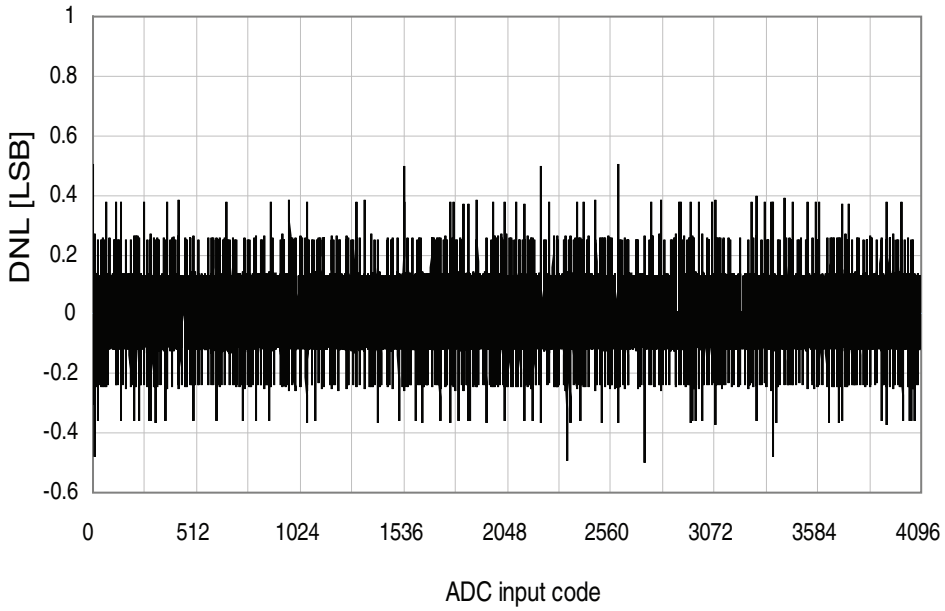


Figure 33-248.Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

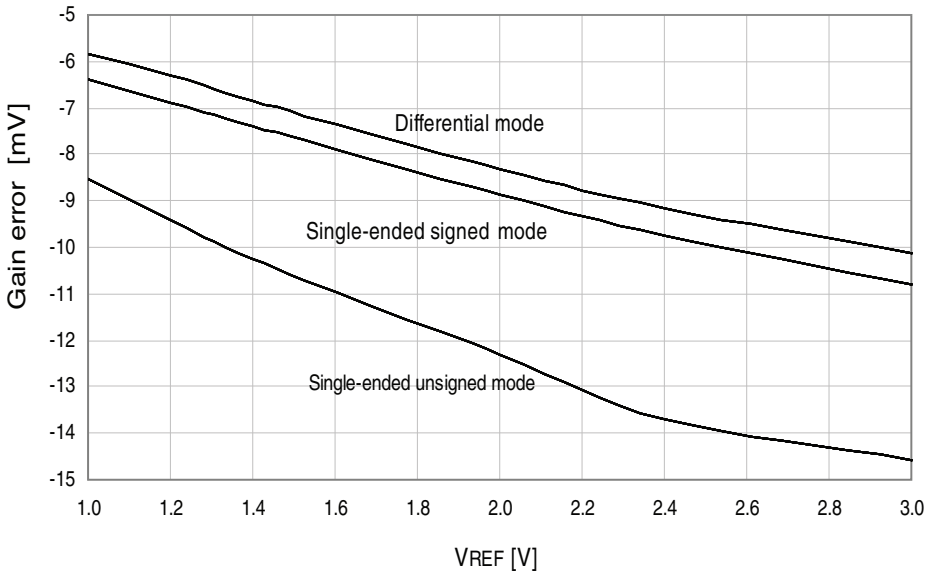


Figure 33-291.Idle Mode Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C

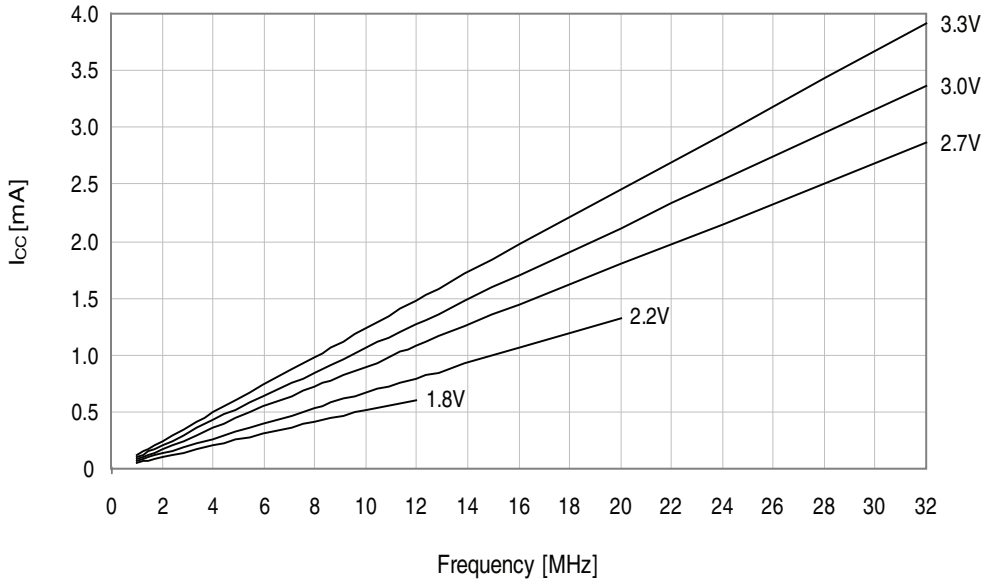
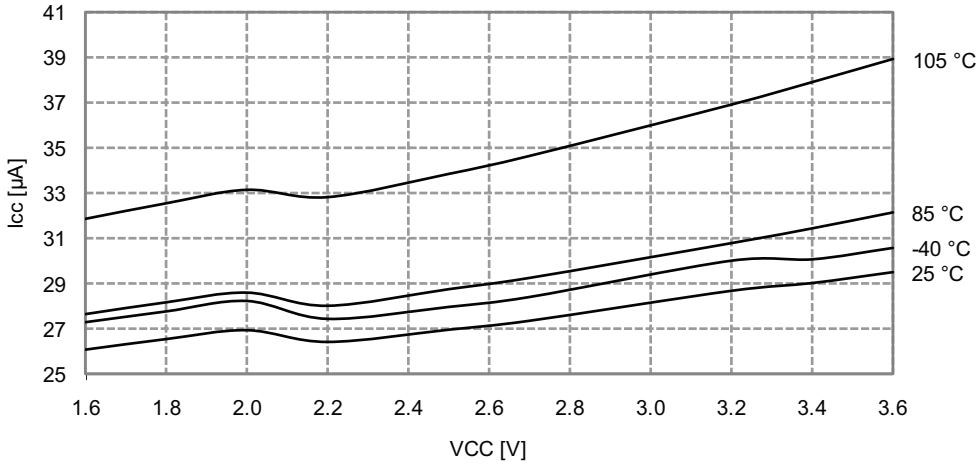


Figure 33-292.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator



33.5.4 Analog Comparator Characteristics

Figure 33-323. Analog Comparator Hysteresis vs. V_{CC}

Small hysteresis

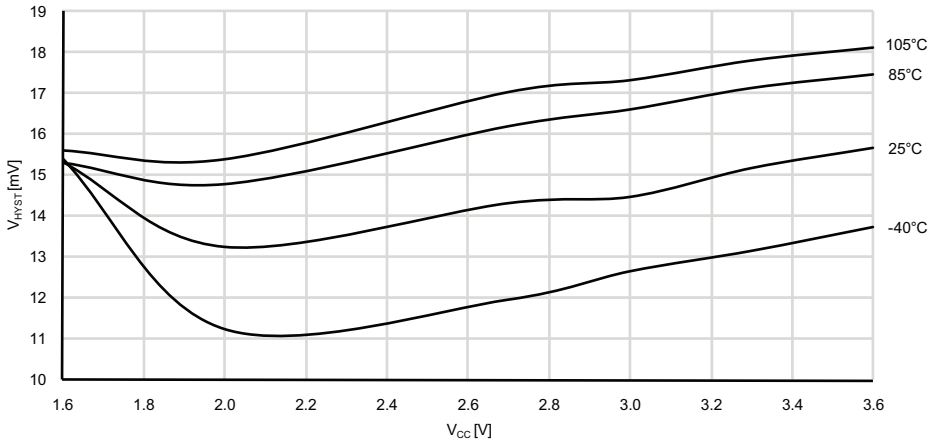


Figure 33-324. Analog Comparator Hysteresis vs. V_{CC}

Large hysteresis

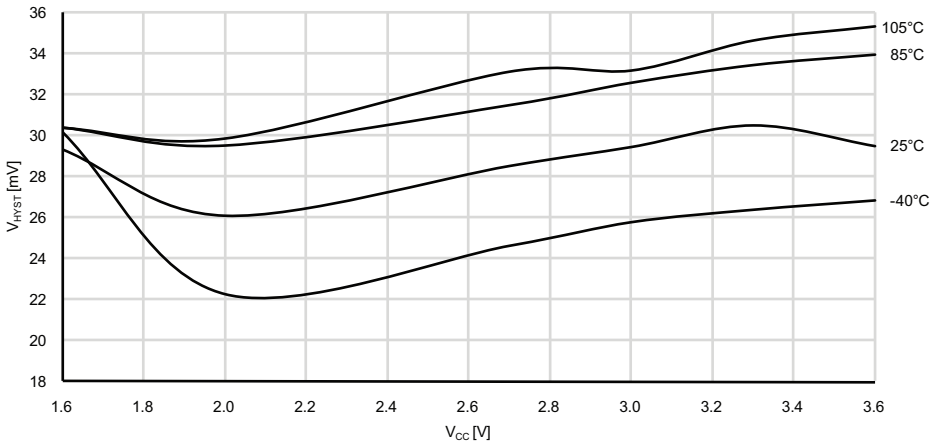
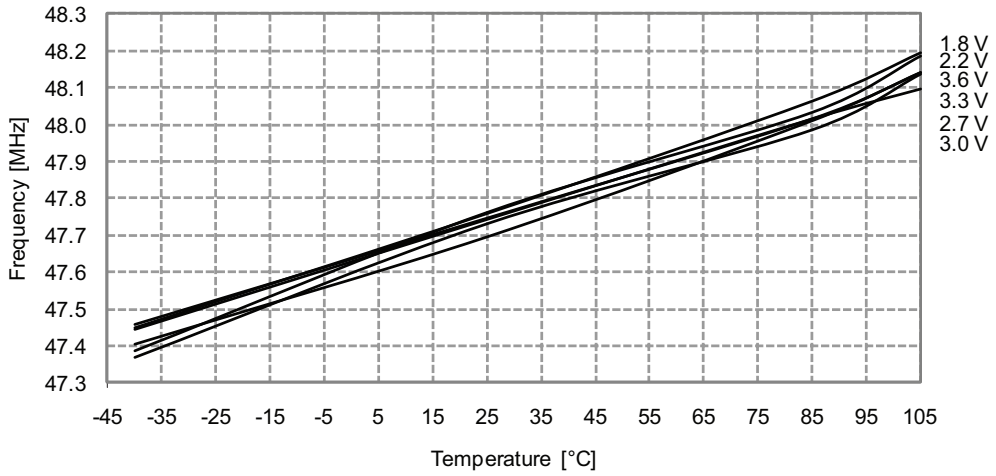


Figure 33-349. 48MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator



33.5.9 Two-Wire Interface Characteristics

Figure 33-350. SDA Hold Time vs. Temperature

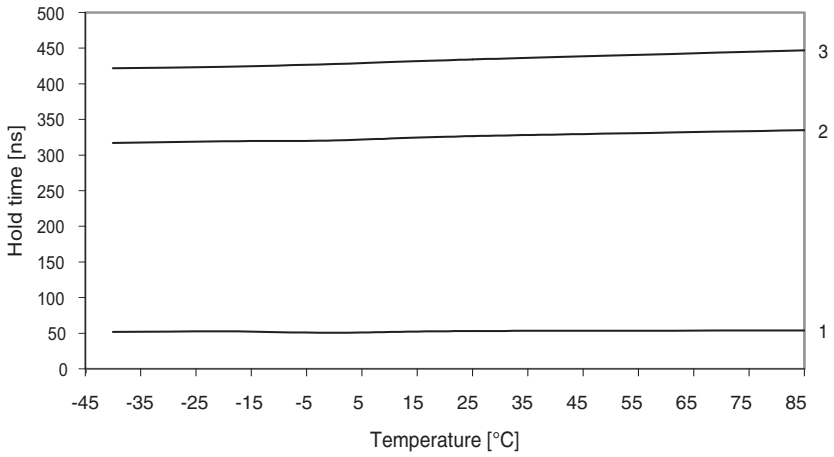


Figure 33-355.Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator

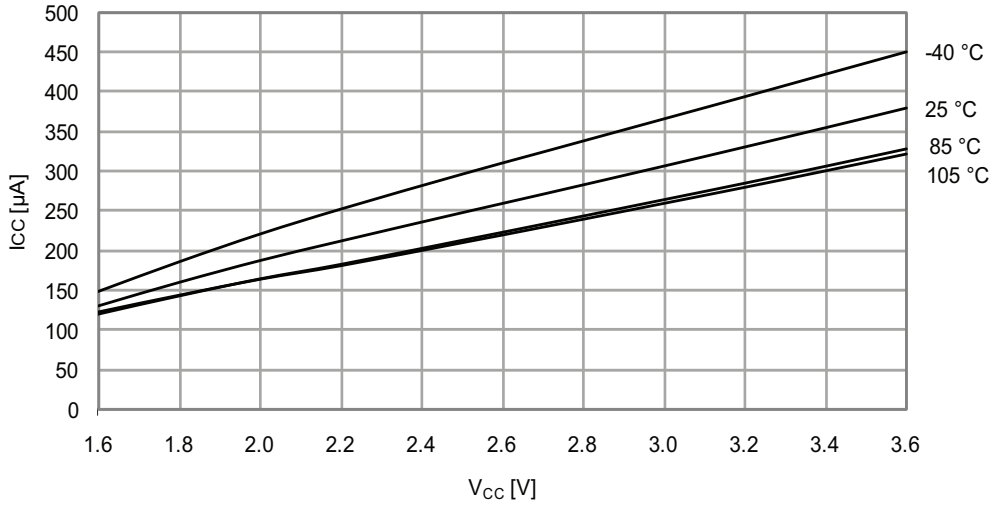
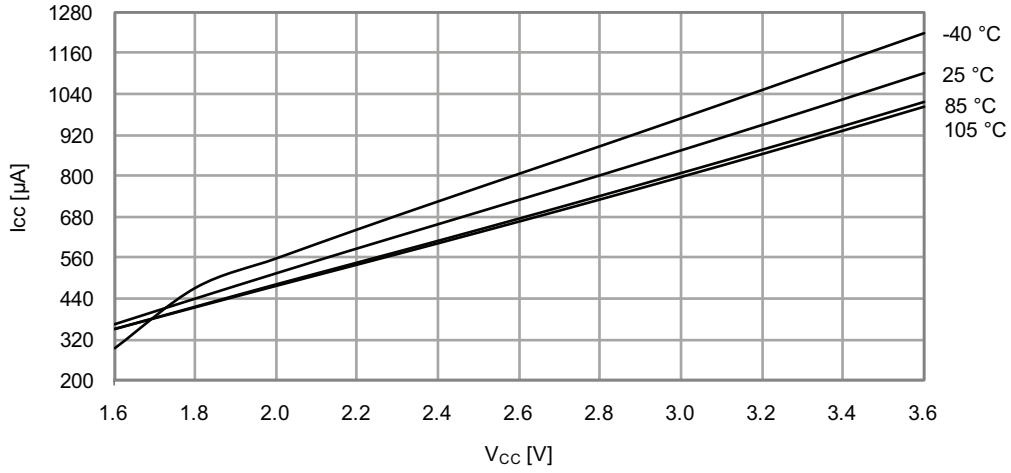


Figure 33-356.Active Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock



34.2 Atmel ATxmega64D3

34.2.1 Rev. I

- AC system status flags are only valid if AC-system is enabled
- Sampled BOD in Active mode will cause noise when bandgap is used as reference
- Temperature sensor not calibrated

1. AC system status flags are only valid if AC-system is enabled

The status flags for the ac-output are updated even though the AC is not enabled which is invalid. Also, it is not possible to clear the AC interrupt flags without enabling either of the Analog comparators.

Problem fix/workaround

Software should clear the AC system flags once, after enabling the AC system before using the AC system status flags.

2. Sampled BOD in Active mode will cause noise when bandgap is used as reference

Using the BOD in sampled mode when the device is running in Active or Idle mode will add noise on the bandgap reference for ADC, DAC, and Analog Comparator.

Problem fix/workaround

If the bandgap is used as reference for either the ADC, DAC and Analog Comparator, the BOD must not be set in sampled mode.

3. Temperature sensor not calibrated

Temperature sensor factory calibration not implemented.

Problem fix/workaround

None.

34.2.2 Rev. H

Not sampled.

34.2.3 Rev. G

Not sampled.

34.2.4 Rev. F

Not sampled.

- PORT remap functions with alternate pin locations for Timer/Counter output compare channels, USART0 and SPI, and the PORT REMAP register
- PORT RTC clock output option and the RTCOUT bit in the PORT CLKEVOUT register
- PORT remap functions with alternate pin locations for the clock and event output, and the CLKEVPIN bit in the PORT CLKEVOUT register
- TOSC alternate pin locations, and TOSCSEL bit in FUSEBYTE2
- Real Time Counter clock source options of external clock from TOSC1, and 32.768kHz from TOSC, and 32.768kHz from the 32.768kHz internal oscillator, and these configuration options in the RTCSRC bits in the Clock RTCTRL register
- PLL divide by two option, and the PLLDIV bit in the Clock PLLCTRL register
- PLL lock detection failure function and the PLLDIF and PLLFDEN bits in the Clock XOSCFAIL register
- The high drive option for external crystal and the XOSCPWR bit on the Oscillator XOSCCTRL register
- The option to enable sequential startup of the analog modules and the ANAINIT register in MCU Control memory

Problem fix/workaround

None.

25. Sampled BOD in Active mode will cause noise when bandgap is used as reference

Using the BOD in sampled mode when the device is running in Active or Idle mode will add noise on the bandgap reference for ADC, DAC and Analog Comparator.

Problem fix/workaround

If the bandgap is used as reference for either the ADC, DAC and Analog Comparator, the BOD must not be set in sampled mode.

26. Temperature sensor not calibrated

Temperature sensor factory calibration not implemented.

Problem fix/workaround

None.

27. Disabling of USART transmitter does not automatically set the TxD pin direction to input

If the USART transmitter is idle with no frames to transmit, setting TXEN to zero will not automatically set the TxD pin direction to input.

Problem fix/workaround

The TxD pin direction can be set to input using the Port DIR register. Be advised that setting the Port DIR register to input will be immediate. Ongoing transmissions will be truncated.

34.3.7 Rev. D

Not sampled.

34.3.8 Rev. C

Not sampled.

6.	Updated ERRATA for ADC (ADC has increased INL error for some operating conditions).
7.	Updated ERRATA “Rev. B” on page 125 with twie (TWIE is not available).
8.	Updated the last page by Atmel new Brand Style Guide.

35.10 8134H – 09/2010

1.	Updated “Errata” on page 388.

35.11 8134G – 08/2010

1.	Updated the Footnote 3 of “Ordering Information” on page 2.
2.	All references to CRC removed. Updated Figure 3-1 on page 5.
3.	Updated “Features” on page 30.
4.	Updated “DC Characteristics” on page 61 by adding Icc for Flash/EEPROM Programming.
5.	Added AV_{CC} in “ADC Characteristics” on page 68.
6.	Updated Start up time in “ADC Characteristics” on page 68.
7.	Updated and fixed typo in “Errata” on page 388.

35.12 8134F – 02/2010

1.	Added “PDI Speed” on page 105.

35.13 8134E – 01/2010

1.	Updated the device pin-out Figure 2-1 on page 5. PDI_CLK and PDI_DATA renamed only PDI.
2.	Updated “ADC – 12-bit Analog to Digital Converter” on page 45.
3.	Updated Figure 25-1 on page 46.
4.	Updated “Alternate Pin Function Description” on page 50.
5.	Updated “Alternate Pin Functions” on page 51.
6.	Updated “Timer/counter and AWEX Functions” on page 50.
7.	Added Table 31-17 on page 68.
8.	Added Table 31-18 on page 69.
9.	Changed internal oscillator speed to “Power-on reset current consumption vs. VCC. BOD level = 3.0V, enabled in continuous mode.” on page 108.
10.	Updated “Errata” on page 388.