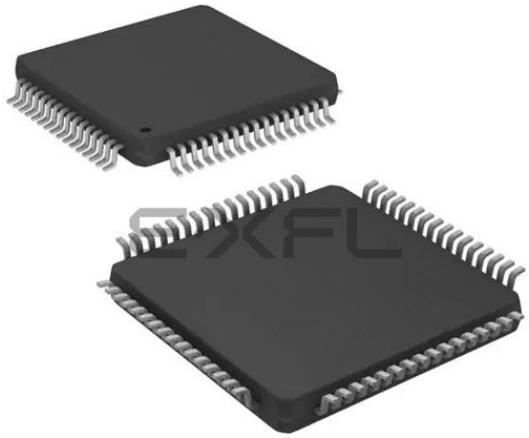

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64d3-au

Package type	
64A	64-lead, 14 * 14mm body size, 1.0mm body thickness, 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)
64M	64-pad, 9 * 9 * 1.0mm body, lead pitch 0.50mm, 7.65mm exposed pad, quad flat no-lead package (QFN)

Typical applications

Industrial control	Climate control	Low power battery applications
Factory automation	RF and ZigBee®	Power tools
Building control	Motor control	HVAC
Board control	Sensor control	Utility metering
White goods	Optical	Medical applications

6.4 ALU - Arithmetic Logic Unit

The arithmetic logic unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed. The ALU operates in direct connection with all 32 general purpose registers. In a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed and the result is stored in the register file. After an arithmetic or logic operation, the status register is updated to reflect information about the result of the operation.

ALU operations are divided into three main categories – arithmetic, logical, and bit functions. Both 8- and 16-bit arithmetic is supported, and the instruction set allows for efficient implementation of 32-bit aritmetic. The hardware multiplier supports signed and unsigned multiplication and fractional format.

6.4.1 Hardware Multiplier

The multiplier is capable of multiplying two 8-bit numbers into a 16-bit result. The hardware multiplier supports different variations of signed and unsigned integer and fractional numbers:

- Multiplication of unsigned integers
- Multiplication of signed integers
- Multiplication of a signed integer with an unsigned integer
- Multiplication of unsigned fractional numbers
- Multiplication of signed fractional numbers
- Multiplication of a signed fractional number with an unsigned one

A multiplication takes two CPU clock cycles.

6.5 Program Flow

After reset, the CPU starts to execute instructions from the lowest address in the flash programmemory ‘0.’ The program counter (PC) addresses the next instruction to be fetched.

Program flow is provided by conditional and unconditional jump and call instructions capable of addressing the whole address space directly. Most AVR instructions use a 16-bit word format, while a limited number use a 32-bit format.

During interrupts and subroutine calls, the return address PC is stored on the stack. The stack is allocated in the general data SRAM, and consequently the stack size is only limited by the total SRAM size and the usage of the SRAM. After reset, the stack pointer (SP) points to the highest address in the internal SRAM. The SP is read/write accessible in the I/O memory space, enabling easy implementation of multiple stacks or stack areas. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR CPU.

6.6 Status Register

The status register (SREG) contains information about the result of the most recently executed arithmetic or logic instruction. This information can be used for altering program flow in order to perform conditional operations. Note that the status register is updated after all ALU operations, as specified in the instruction set reference. This will in many cases remove the need for using the dedicated compare instructions, resulting in faster and more compact code.

The status register is not automatically stored when entering an interrupt routine nor restored when returning from an interrupt. This must be handled by software.

The status register is accessible in the I/O memory space.

6.7 Stack and Stack Pointer

The stack is used for storing return addresses after interrupts and subroutine calls. It can also be used for storing temporary data. The Stack Pointer (SP) register always points to the top of the stack. It is implemented as two 8-bit registers that are accessible in the I/O memory space. Data are pushed and popped from the stack using the PUSH and POP instructions. The stack grows from a higher memory location to a lower memory location. This implies that pushing data onto the stack decreases the SP, and popping data off the stack increases the SP. The SP is automatically loaded

The production signature row cannot be written or erased, but it can be read from application software and external programmers.

Table 7-1. Device ID Bytes

Device	Device ID bytes		
	Byte 2	Byte 1	Byte 0
ATxmega32D3	4A	95	1E
ATxmega64D3	4A	96	1E
ATxmega128D3	48	97	1E
ATxmega192D3	49	97	1E
ATxmega256D3	44	98	1E
ATxmega384D3	47	98	1E

7.3.5 User Signature Row

The user signature row is a separate memory section that is fully accessible (read and write) from application software and external programmers. It is one flash page in size, and is meant for static user parameter storage, such as calibration data, custom serial number, identification numbers, random number seeds, etc. This section is not erased by chip erase commands that erase the flash, and requires a dedicated erase command. This ensures parameter storage during multiple program/erase operations and on-chip debug sessions.

7.4 Fuses and Lock Bits

The fuses are used to configure important system functions, and can only be written from an external programmer. The application software can read the fuses. The fuses are used to configure reset sources such as brownout detector and watchdog, and startup configuration.

The lock bits are used to set protection levels for the different flash sections (that is, if read and/or write access should be blocked). Lock bits can be written by external programmers and application software, but only to stricter protection levels. Chip erase is the only way to erase the lock bits. To ensure that flash contents are protected even during chip erase, the lock bits are erased after the rest of the flash memory has been erased.

An unprogrammed fuse or lock bit will have the value one, while a programmed fuse or lock bit will have the value zero.

Both fuses and lock bits are reprogrammable like the flash program memory.

7.5 Data Memory

The data memory contains the I/O memory, internal SRAM, optionally memory mapped EEPROM, and external memory if available. The data memory is organized as one continuous memory section, see Figure 7-2 on page 16. To simplify development, I/O Memory, EEPROM and SRAM will always have the same start addresses for all Atmel AVR XMEGA devices.

26. AC – Analog Comparator

26.1 Features

- Two analog comparators (AC)
- Selectable hysteresis
  - No
  - Small
  - Large
- Analog comparator output available on pin
- Flexible input selection
  - All pins on the port
  - Bandgap reference voltage
  - A 64-level programmable voltage scaler of the internal AV_{CC} voltage
- Interrupt and event generation on:
  - Rising edge
  - Falling edge
  - Toggle
- Window function interrupt and event generation on:
  - Signal above window
  - Signal inside window
  - Signal below window
- Constant current source with configurable output pin selection

26.2 Overview

The analog comparator (AC) compares the voltage levels on two inputs and gives a digital output based on this comparison. The analog comparator may be configured to generate interrupt requests and/or events upon several different combinations of input change.

The analog comparator hysteresis can be adjusted in order to achieve the optimal operation for each application.

The input selection includes analog port pins, several internal signals, and a 64-level programmable voltage scaler. The analog comparator output state can also be output on a pin for use by external devices.

A constant current source can be enabled and output on a selectable pin. This can be used to replace, for example, external resistors used to charge capacitors in capacitive touch sensing applications.

The analog comparators are always grouped in pairs on each port. These are called analog comparator 0 (AC0) and analog comparator 1 (AC1). They have identical behavior, but separate control registers. Used as pair, they can be set in window mode to compare a signal to a voltage range instead of a voltage level.

PORTA has one AC pair. Notation is ACA.

32.2.4 Wake-up Time from Sleep Modes

Table 32-35. Device Wake-up Time from Sleep Modes with Various System Clock Sources

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from idle, standby, and extended standby mode	External 2MHz clock		2.0		µs
		32.768kHz internal oscillator		125		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from power-save and power-down mode	External 2MHz clock		4.6		
		32.768kHz internal oscillator		330		
		2MHz internal oscillator		9.5		
		32MHz internal oscillator		5.6		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 32-9. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 32-9. Wake-up Time Definition

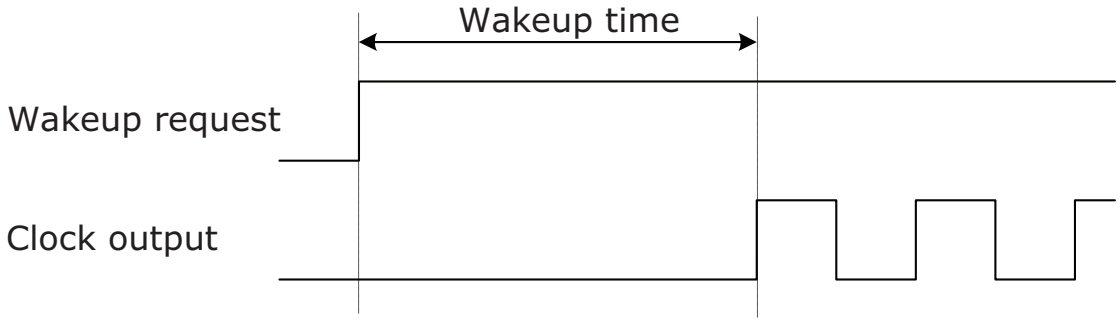
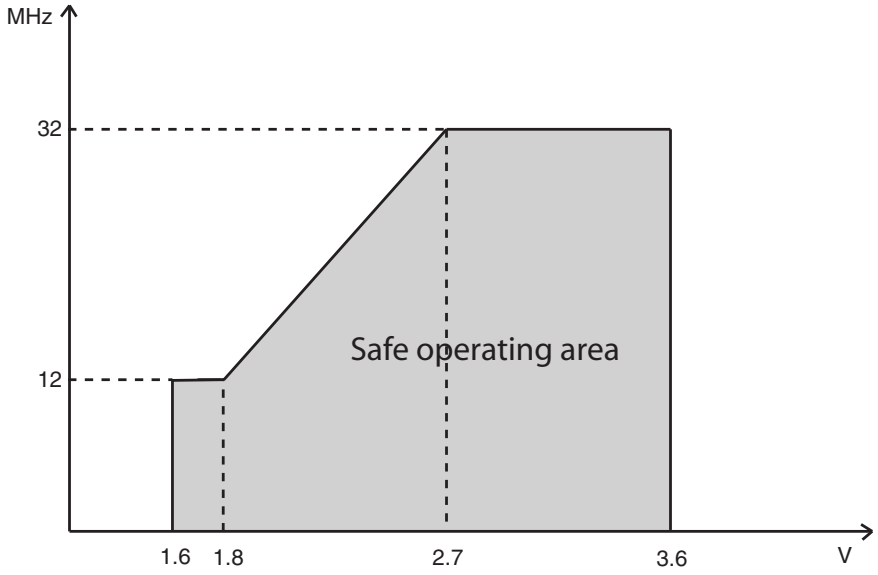


Figure 32-15.Maximum Frequency vs. V_{CC}



32.3.8 Bandgap and Internal 1.0V Reference Characteristics

Table 32-71. Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC		1 Clk_{PER} + 2.5µs		µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T = 85°C, after calibration	0.99	1.0	1.01	
	Variation over voltage and temperature	Calibrated at T = 85°C		1		%

32.3.9 Brownout Detection Characteristics

Table 32-72. Brownout Detection Characteristics (1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.40	1.60	1.70	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.0		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

32.3.10 External Reset Characteristics

Table 32-73. External Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width		1000	100		ns
V_{RST}	Reset threshold voltage	V_{CC} = 2.7 - 3.6V		0.45 * V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.45 * V_{CC}		
R_{RST}	Reset pin pull-up resistor			27		kΩ

32.5.5 I/O Pin Characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

Table 32-123. I/O Pin Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} (1)/ I_{OL} (2)	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage	V_{CC} = 2.4 - 3.6V		0.7 * V_{CC}		V_{CC} + 0.5	V
		V_{CC} = 1.6 - 2.4V		0.8 * V_{CC}		V_{CC} + 0.5	
V_{IL}	Low level input voltage	V_{CC} = 2.4 - 3.6V		-0.5		0.3 * V_{CC}	
		V_{CC} = 1.6 - 2.4V		-0.5		0.2 * V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.6		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current I/O pin	T = 25°C			<0.01	1.0	µA
R_P	Pull/buss keeper resistor				25		kΩ

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
   The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
   The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.

32.5.8 Bandgap and Internal 1.0V Reference Characteristics

Table 32-129. Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC		1 Clk_{PER} + 2.5µs		µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T = 85°C, after calibration	0.99	1.0	1.01	
	Variation over voltage and temperature	Calibrated at T = 85°C		1		%

32.5.9 Brownout Detection Characteristics

Table 32-130. Brownout Detection Characteristics (1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.40	1.60	1.70	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.0		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

32.5.10 External Reset Characteristics

Table 32-131. External Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width		1000	90		ns
V_{RST}	Reset threshold voltage	V_{CC} = 2.7 - 3.6V		0.45 * V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.45 * V_{CC}		
R_{RST}	Reset pin pull-up resistor			25		kΩ

32.5.11 Power-on Reset Characteristics

Table 32-132. Power-on Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} (1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.3		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled $V_{POT-} = V_{POT+}$.

32.5.12 Flash and EEPROM Memory Characteristics

Table 32-133. Endurance and Data Retention

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/Erase cycles	25°C	10K			Cycle
			85°C	10K			
			105°C	2K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			
	EEPROM	Write/Erase cycles	25°C	100K			Cycle
			85°C	100K			
			105°C	30K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			

Table 32-134. Programming Time

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
	Chip erase (2)	256KB flash, EEPROM		105		ms
	Application erase	Section erase		6		
	Flash	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		
	EEPROM	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

Figure 33-82. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

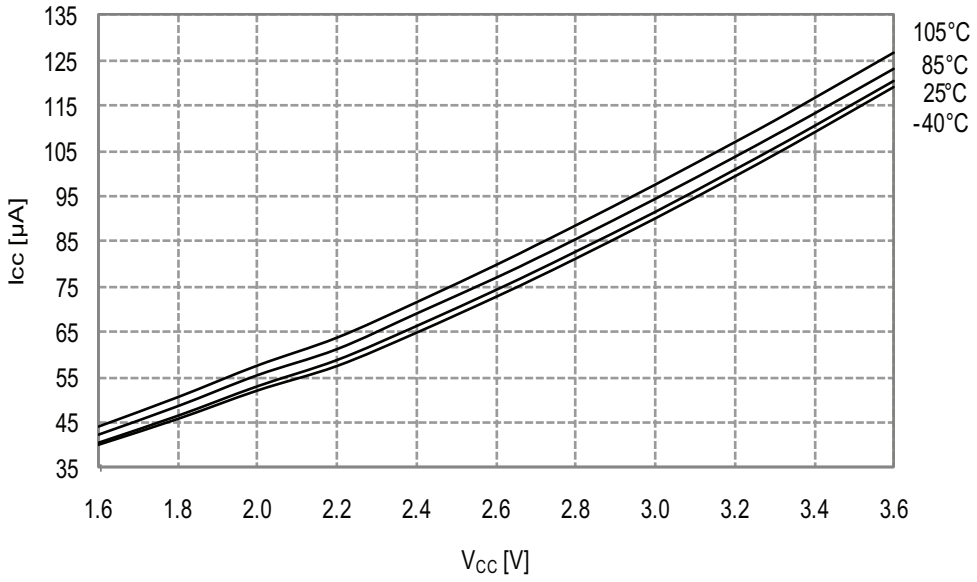


Figure 33-83. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator

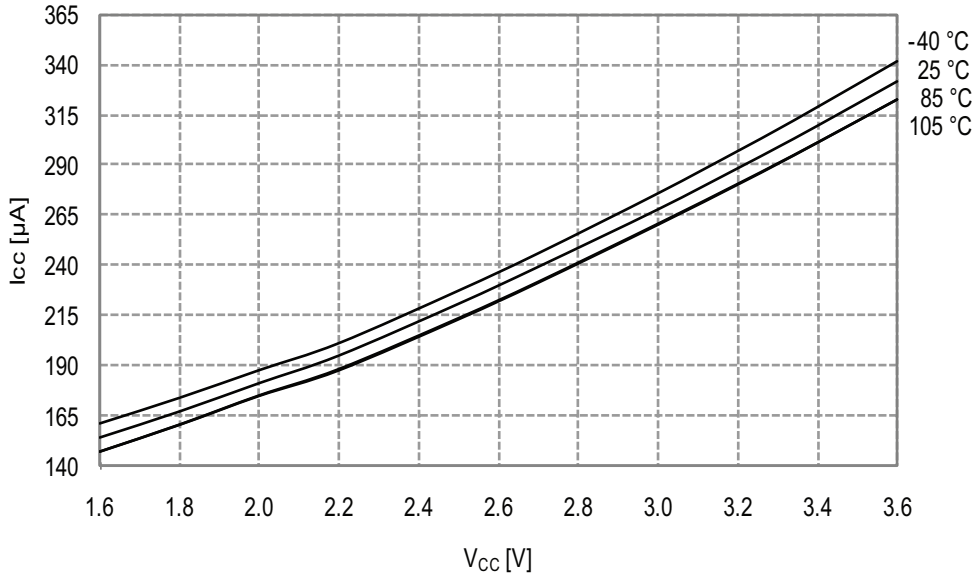


Figure 33-179. Gain Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps

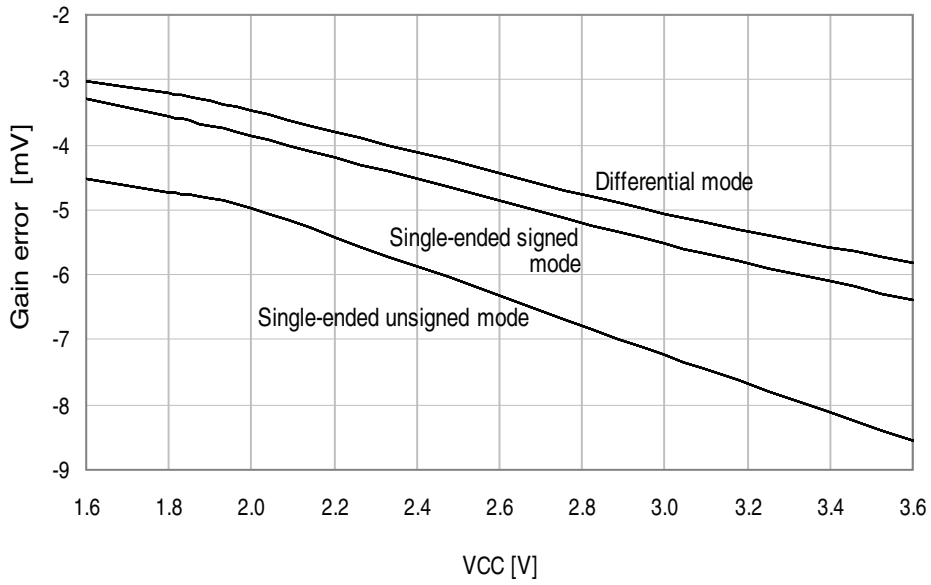


Figure 33-180. Offset Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

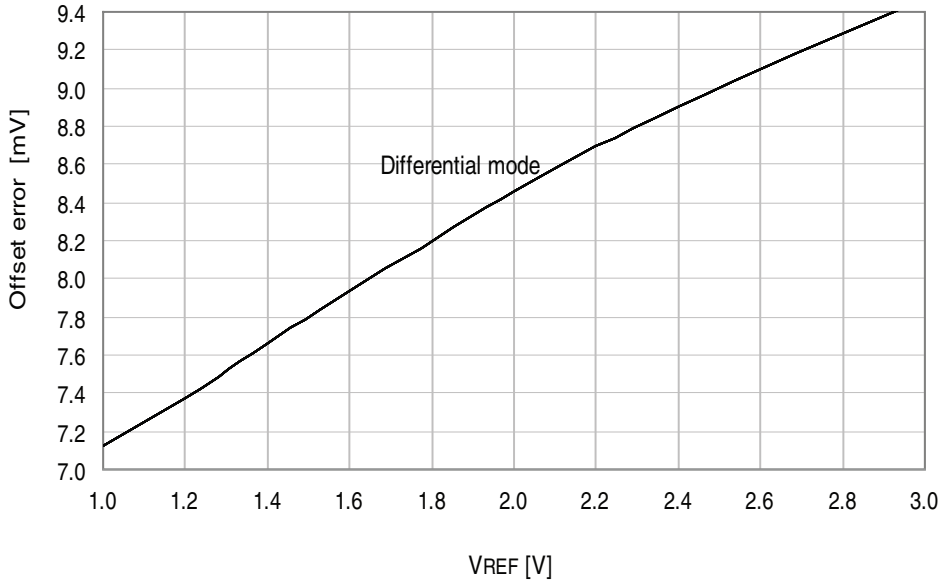


Figure 33-225.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz

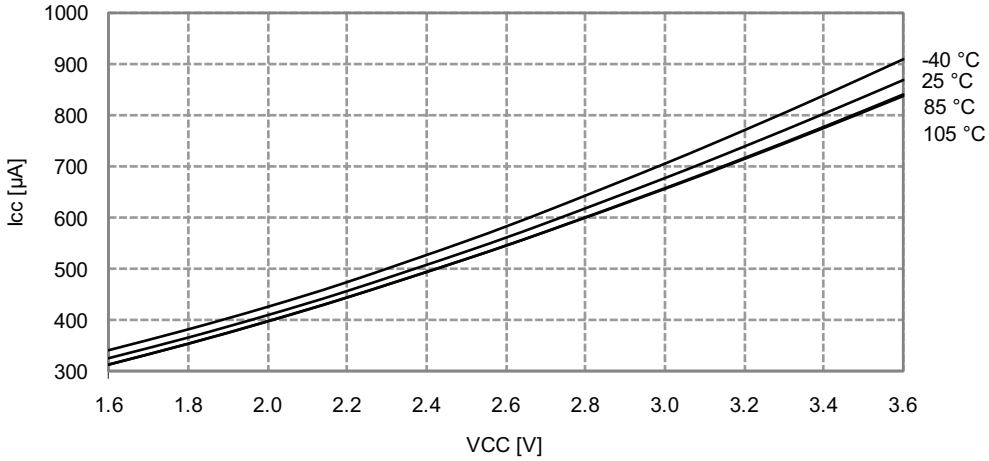


Figure 33-226.Idle Mode Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator

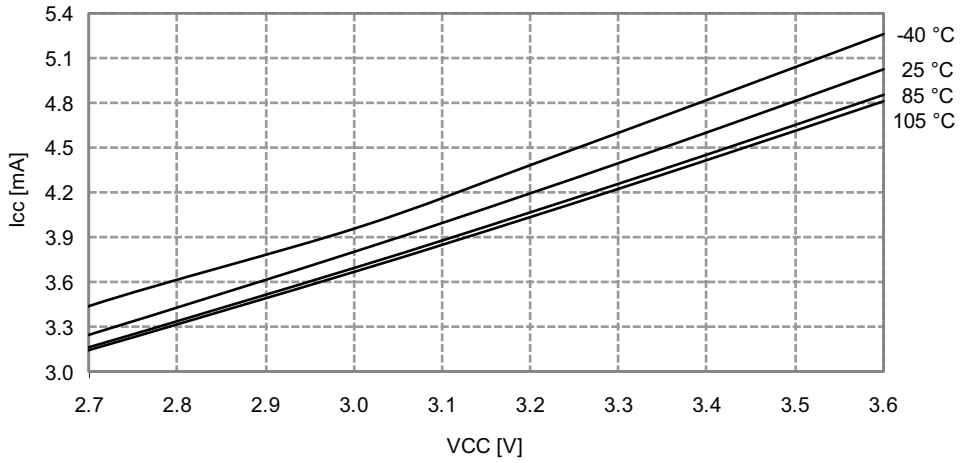


Figure 33-245.DNL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

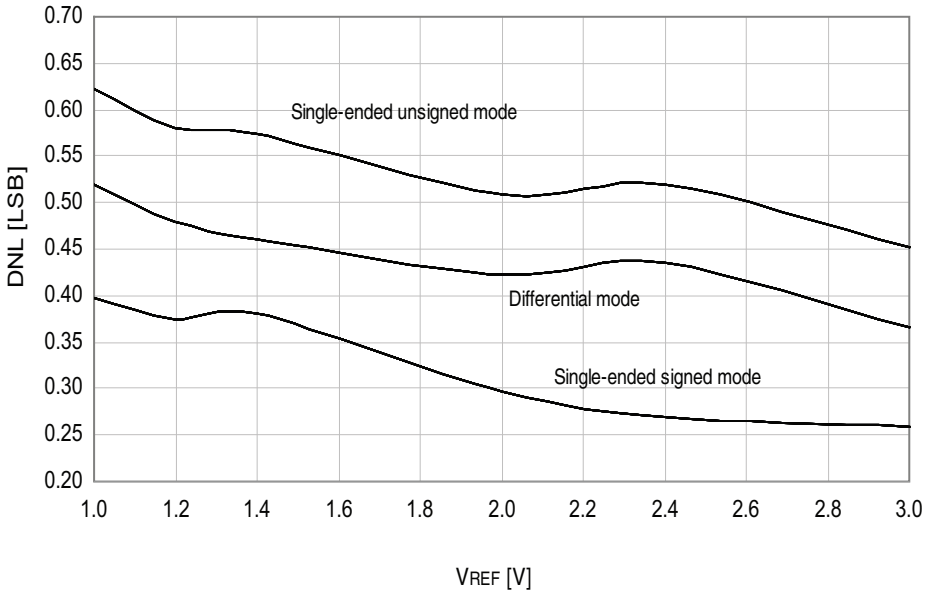


Figure 33-246.DNL Error vs. Sample Rate

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external

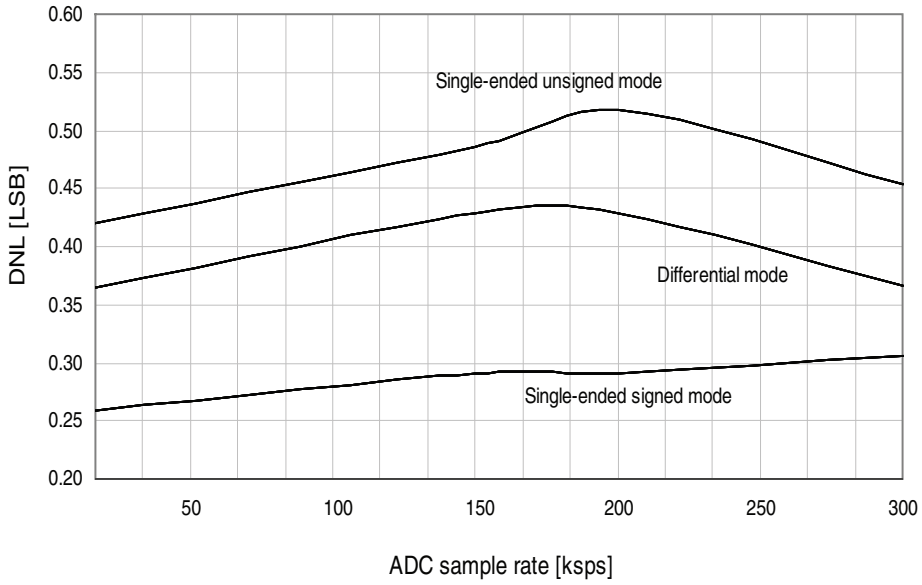


Figure 33-305.I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.3V

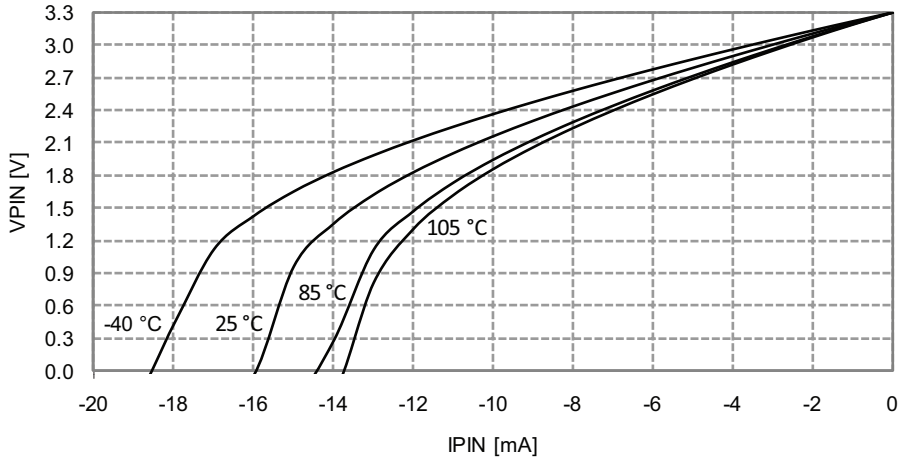


Figure 33-306.I/O Pin Output Voltage vs. Sink Current

V_{CC} = 1.8V

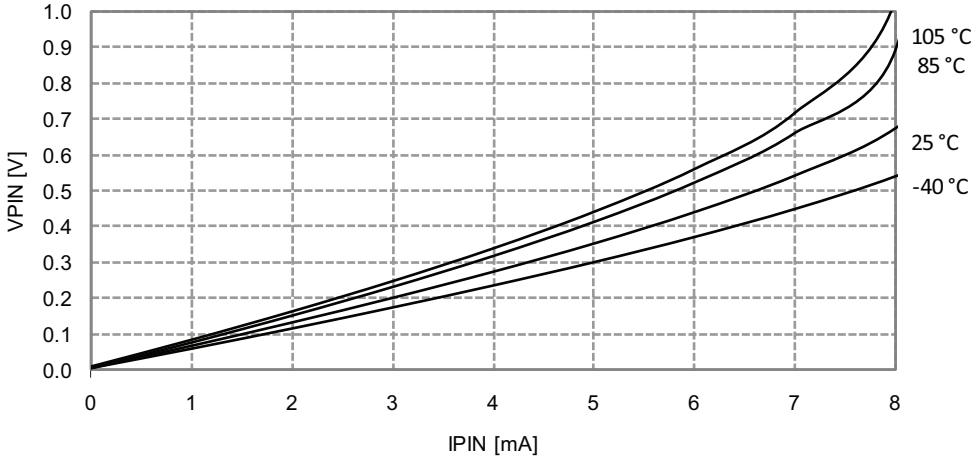
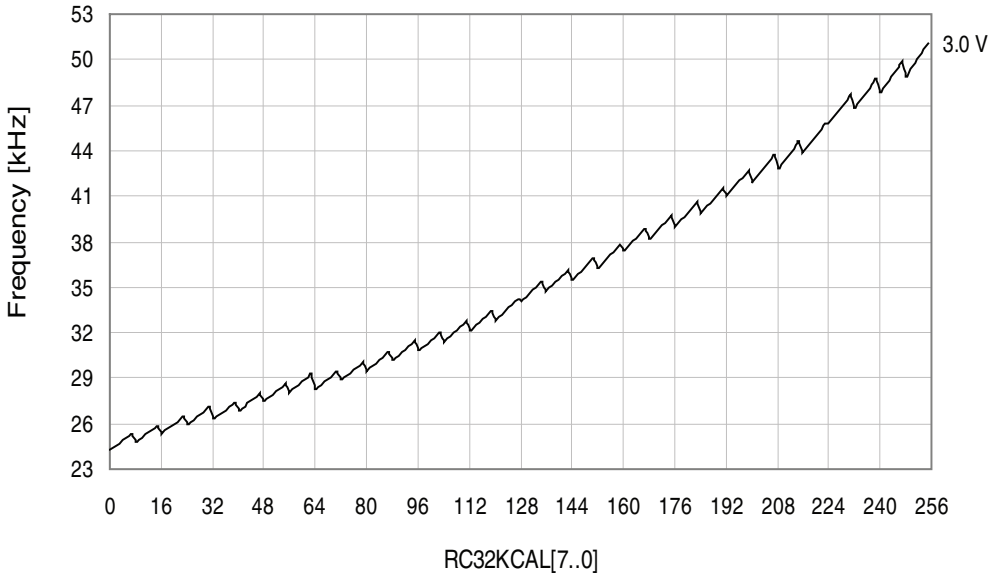


Figure 33-337. 32.768kHz Internal Oscillator Frequency vs. Calibration Value

V_{CC} = 3.0V, T = 25°C



33.5.8.3 2MHz Internal Oscillator

Figure 33-338. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled

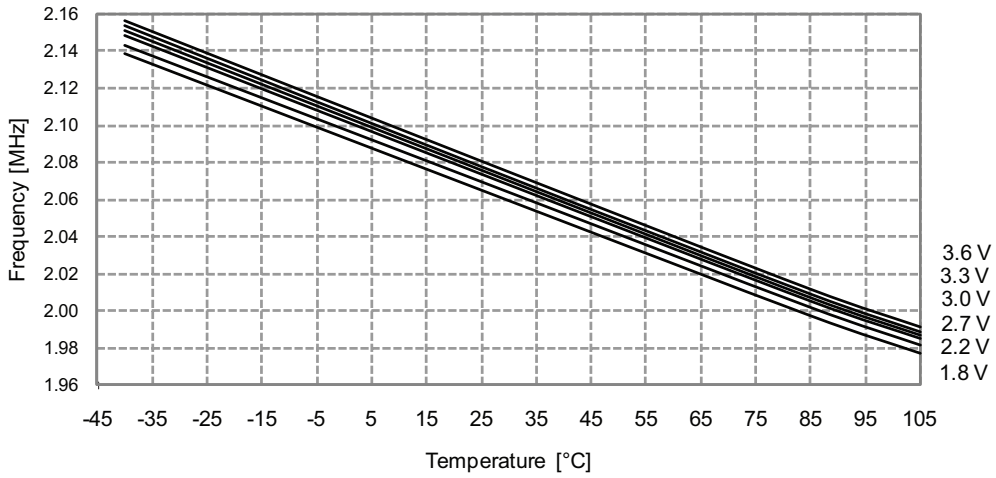


Figure 33-387. DNL Error vs. Input Code

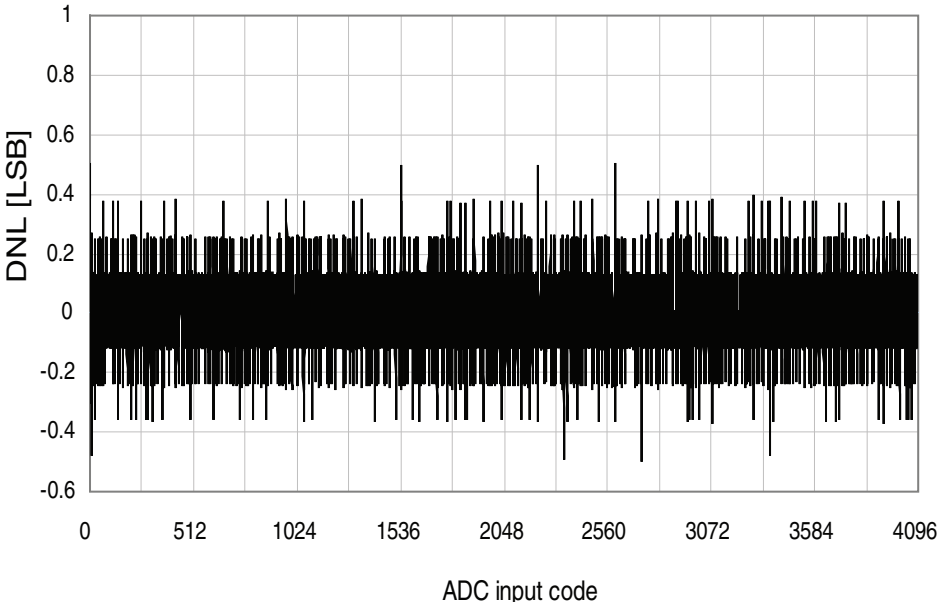
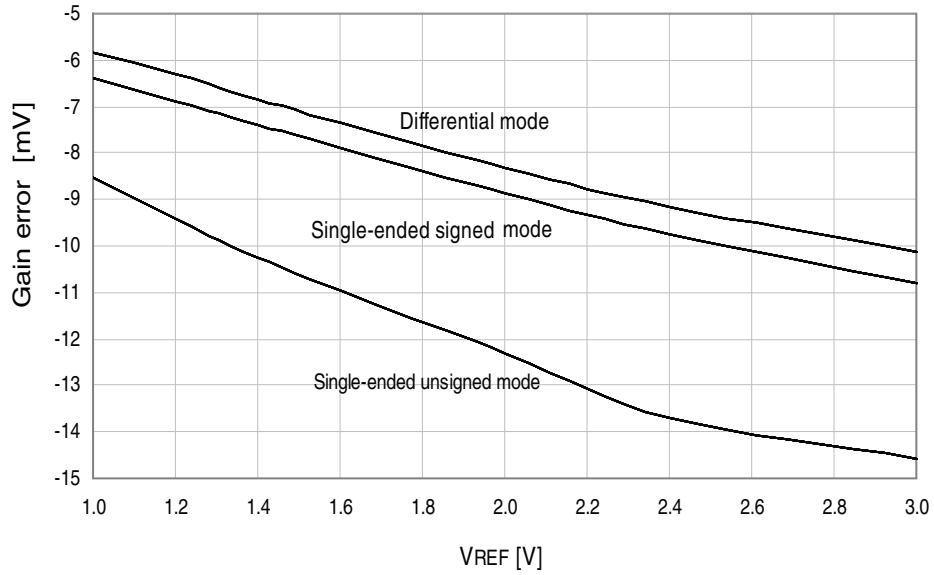


Figure 33-388. Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps



- CRC generator module
- ADC 1/2× gain option, and this configuration option in the GAIN bits in the ADC Channel CTRL register
- ADC VCC/2 reference option and this configuration option in the REFSEL bits on the ADC REFCTRL register
- ADC option to use internal Gnd as negative input in differential measurements and this configuration option in the MUXNEG bits in the ADC Channel MUXCTRL register
- ADC channel scan and the ADC SCAN register
- ADC current limitation option, and the CURRLIMIT bits in the ADC CTRLB register
- ADC impedance mode selection for the gain stage, and the IMPMODE bit in the ADC CTRLB register
- Timer/Counter 2 and the SPLITMODE configuration option in the BYTEM bits in the Timer/Counter 0 CTRLE register
- Analog Comparator (AC) current output option, and the AC CURRCTRL and CURRCALIB registers
- PORT remap functions with alternate pin locations for Timer/Counter output compare channels, USART0 and SPI, and the PORT REMAP register
- PORT RTC clock output option and the RTCOUT bit in the PORT CLKEVOUT register
- PORT remap functions with alternate pin locations for the clock and event output, and the CLKEVPIN bit in the PORT CLKEVOUT register
- TOSC alternate pin locations, and TOSCSEL bit in FUSEBYTE2
- Real Time Counter clock source options of external clock from TOSC1, and 32.768kHz from TOSC, and 32.768kHz from the 32.768kHz internal oscillator, and these configuration options in the RTCSRC bits in the Clock RTCTRL register
- PLL divide by two option, and the PLLDIV bit in the Clock PLLCTRL register
- PLL lock detection failure function and the PLLDIF and PLLFDEN bits in the Clock XOSCFAIL register
- The high drive option for external crystal and the XOSCPWR bit on the Oscillator XOSCCTRL register
- The option to enable sequential startup of the analog modules and the ANAINIT register in MCU Control memory

Problem fix/workaround

None.

27. Sampled BOD in Active mode will cause noise when bandgap is used as reference

Using the BOD in sampled mode when the device is running in Active or Idle mode will add noise on the bandgap reference for ADC, DAC and Analog Comparator.

Problem fix/workaround

If the bandgap is used as reference for either the ADC, DAC and Analog Comparator, the BOD must not be set in sampled mode.

28. Temperature sensor not calibrated

Temperature sensor factory calibration not implemented.

Problem fix/workaround

None.

28. Disabling of USART transmitter does not automatically set the TxD pin direction to input

If the USART transmitter is idle with no frames to transmit, setting TXEN to zero will not automatically set the TxD pin direction to input.

25. Non available functions and options

The below function and options are not available. Writing to any registers or fuse to try and enable or configure these functions or options will have no effect, and will be as writing to a reserved address location.

- TWIE, the TWI module on PORTE
- TWI SDAHOLD option in the TWI CTRL register is one bit
- CRC generator module
- ADC 1/2× gain option, and this configuration option in the GAIN bits in the ADC Channel CTRL register
- ADC VCC/2 reference option and this configuration option in the REFSEL bits on the ADC REFCTRL register
- ADC option to use internal Gnd as negative input in differential measurements and this configuration option in the MUXNEG bits in the ADC Channel MUXCTRL register
- ADC channel scan and the ADC SCAN register
- ADC current limitation option, and the CURRLIMIT bits in the ADC CTRLB register
- ADC impedance mode selection for the gain stage, and the IMPMODE bit in the ADC CTRLB register
- Timer/Counter 2 and the SPLITMODE configuration option in the BYTEM bits in the Timer/Counter 0 CTRLE register
- Analog Comparator (AC) current output option, and the AC CURRCTRL and CURRCALIB registers
- PORT remap functions with alternate pin locations for Timer/Counter output compare channels, USART0 and SPI, and the PORT REMAP register
- PORT RTC clock output option and the RTCOUT bit in the PORT CLKEVOUT register
- PORT remap functions with alternate pin locations for the clock and event output, and the CLKEVPIN bit in the PORT CLKEVOUT register
- TOSC alternate pin locations, and TOSCSEL bit in FUSEBYTE2
- Real Time Counter clock source options of external clock from TOSC1, and 32.768kHz from TOSC, and 32.768kHz from the 32.768kHz internal oscillator, and these configuration options in the RTCSRC bits in the Clock RTCTRL register
- PLL divide by two option, and the PLLDIV bit in the Clock PLLCTRL register
- PLL lock detection failure function and the PLLDIF and PLLFDEN bits in the Clock XOSCFAIL register
- The high drive option for external crystal and the XOSCPWR bit on the Oscillator XOSCCTRL register
- The option to enable sequential startup of the analog modules and the ANAINIT register in MCU Control memory

Problem fix/workaround

None.

26. Sampled BOD in Active mode will cause noise when bandgap is used as reference

Using the BOD in sampled mode when the device is running in Active or Idle mode will add noise on the bandgap reference for ADC, DAC and Analog Comparator.

Problem fix/workaround

If the bandgap is used as reference for either the ADC, DAC and Analog Comparator, the BOD must not be set in sampled mode.

27. Temperature sensor not calibrated

Temperature sensor factory calibration not implemented.

Problem fix/workaround

None.

9.	The sentence “The port pins also have configurable slew rate limitation to reduce electromagnetic emission” in Chapter “I/O Ports” on page 30 is removed.
10.	The sentence “The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification” is added to Section 32.1.5 on page 68, Section 32.2.5 on page 87, Section 32.6.5 on page 163, Section 33.5.2 on page 297 and Section 33.6.2 on page 331.
11.	Figure 2-1 on page 5 is updated by changing V_{DD} to V_{CC}.
12.	Table 7-1 on page 15 is updated.
13.	Figure 7-2 on page 16 is updated.
14.	Figure 14-7 on page 33 is updated.
15.	Former Table 32-24, Table 32-52, Table 32-79, Table 32-107, Table 32-135, Table 32-163 (title: “External clock”) have each been replaced by two new tables, named respectively “External clock used as system clock without prescaling” and “External clock with prescaler for system clock”.
16.	In Table 32-29 on page 81, Table 32-58 on page 100, Table 32-87 on page 119, Table 32-116 on page 138, Table 32-145 on page 157, and Table 32-174 on page 176 the value for the parameter “Input voltage” has been corrected.
17.	In Table 32-18 on page 73, Table 32-47 on page 92, Table 32-76 on page 111, Table 32-105 on page 130, Table 32-134 on page 149, and Table 32-163 on page 168 the parameter “Application erase” has been added.
18.	Table 32-14 on page 72, Table 32-43 on page 91, Table 32-101 on page 129, Table 32-130 on page 148 and Table 32-159 on page 167 (Brownout detection characteristics) are updated.
19.	Table 32-20 on page 74 and Table 32-49 on page 93 (2MHz internal oscillator characteristics) are updated.
20.	Table 32-21 on page 74 and Table 32-50 on page 93 (32MHz internal oscillator characteristics) are updated.
21.	Accuracy added in Table 32-109 on page 131.
22.	Table 32-149 on page 160 has been corrected.
23	Table 32-167 on page 169; “Factory calibration accuracy” and “Accuracy” is added.
24.	Table 32-150 on page 161, Table 32-152 on page 163, Table 32-154 on page 164, Table 32-155 on page 165, Table 32-156 on page 166, and Table 32-157 on page 166 has been updated.
25.	Section 1. “Ordering Information” on page 2 is updated.
26.	Former Section 31.3 “64Z3” has been removed.
27.	Section 31.2 “64M” on page 62 has replaced the former Section 31.2 “64M2”.

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1.	Datasheet status changed to complete: Preliminary removed from front page.
2.	Updated all tables in the The maximum CPU clock frequency depends on VCC. As shown in Figure 32-8 on page 83 the frequency vs. VCC curve is linear between 1.8V < VCC < 2.7V. on page 64.
3.	Replaced Table 31-11 on page 67.
4.	Replaced Table 31-17 on page 68 and added the figure “TOSC input capacitance” on page 78.
5.	Added “Rev. E” on page 118.