



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64d3-aur

17. AWeX – Advanced Waveform Extension

17.1 Features

- Waveform output with complementary output from each compare channel
- Four dead-time insertion (DTI) units
 - 8-bit resolution
 - Separate high and low side dead-time setting
 - Double buffered dead time
 - Optionally halts timer during dead-time insertion
- Pattern generation unit creating synchronised bit pattern across the port pins
 - Double buffered pattern generation
 - Optional distribution of one compare channel output across the port pins
- Event controlled fault protection for instant and predictable fault triggering

17.2 Overview

The advanced waveform extension (AWeX) provides extra functions to the timer/counter in waveform generation (WG) modes. It is primarily intended for use with different types of motor control and other power control applications. It enables low- and high side output with dead-time insertion and fault protection for disabling and shutting down external drivers. It can also generate a synchronized bit pattern across the port pins.

Each of the waveform generator outputs from the timer/counter 0 are split into a complimentary pair of outputs when any AWeX features are enabled. These output pairs go through a dead-time insertion (DTI) unit that generates the non-inverted low side (LS) and inverted high side (HS) of the WG output with dead-time insertion between LS and HS switching. The DTI output will override the normal port value according to the port override setting.

The pattern generation unit can be used to generate a synchronized bit pattern on the port it is connected to. In addition, the WG output from compare channel A can be distributed to and override all the port pins. When the pattern generator unit is enabled, the DTI unit is bypassed.

The fault protection unit is connected to the event system, enabling any event to trigger a fault condition that will disable the AWeX output. The event system ensures predictable and instant fault reaction, and gives flexibility in the selection of fault triggers.

The AWeX is available for TCC0. The notation of this is AWEXC.

28. Pinout and Pin Functions

The device pinout is shown in “[Pinout/block Diagram](#)” on page 5. In addition to general purpose I/O functionality, each pin can have several alternate functions. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the pin functions can be used at time.

28.1 Alternate Pin Function Description

The tables below show the notation for all pin functions available and describe its function.

28.1.1 Operation/power Supply

V_{CC}	Digital supply voltage
AV_{CC}	Analog supply voltage
GND	Ground

28.1.2 Port Interrupt Functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

28.1.3 Analog Functions

ACn	Analog comparator input pin n
ACnOUT	Analog comparator n output
ADCn	Analog to digital converter input pin n
A_{REF}	Analog reference input pin

28.1.4 Timer/counter and AWEX Functions

OCnxLS	Output compare channel x low side for Timer/Counter n
OCnxHS	Output compare channel x high side for Timer/Counter n

Table 28-6. Port F - Alternate Functions

PORT F	PIN #	INTERRUPT	TCF0
PF0	46	SYNC	OC0A
PF1	47	SYNC	OC0B
PF2	48	SYNC/ASYNC	OC0C
PF3	49	SYNC	OC0D
PF4	50	SYNC	
PF5	51	SYNC	
PF6	54	SYNC	
PF7	55	SYNC	
GND	52		
VCC	53		

Table 28-7. Port R - Alternate Functions

PORT R	PIN #	INTERRUPT	PDI	XTAL
PDI	56		PDI_DATA	
$\overline{\text{RESET}}$	57		PDI_CLOCK	
PRO	58	SYNC		XTAL2
PR1	59	SYNC		XTAL1

32.1.5 I/O Pin Characteristics

The I/O pins comply with the JEDEC LVTTTL and LVCMOS specification and the high- and low-level input and output voltage limits reflect or exceed this specification.

Table 32-7. I/O Pin Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
$I_{OH}^{(1)}/I_{OL}^{(2)}$	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage	$V_{CC} = 2.4 - 3.6V$		$0.7 * V_{CC}$		$V_{CC} + 0.5$	V
		$V_{CC} = 1.6 - 2.4V$		$0.8 * V_{CC}$		$V_{CC} + 0.5$	
V_{IL}	Low level input voltage	$V_{CC} = 2.4 - 3.6V$		-0.5		$0.3 * V_{CC}$	
		$V_{CC} = 1.6 - 2.4V$		-0.5		$0.2 * V_{CC}$	
V_{OH}	High level output voltage	$V_{CC} = 3.3V$	$I_{OH} = -4mA$	2.6	2.9		
		$V_{CC} = 3.0V$	$I_{OH} = -3mA$	2.1	2.6		
		$V_{CC} = 1.8V$	$I_{OH} = -1mA$	1.4	1.6		
V_{OL}	Low level output voltage	$V_{CC} = 3.3V$	$I_{OL} = 8mA$		0.4	0.76	
		$V_{CC} = 3.0V$	$I_{OL} = 5mA$		0.3	0.64	
		$V_{CC} = 1.8V$	$I_{OL} = 3mA$		0.2	0.46	
I_{IN}	Input leakage current I/O pin	$T = 25^{\circ}C$			<0.01	1	μA
R_P	Pull/buss keeper resistor				25		$k\Omega$

- Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
The sum of all I_{OH} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.
 2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
The sum of all I_{OL} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.

32.2.13 Clock and Oscillator Characteristics

32.2.13.1 Calibrated 32.768kHz Internal Oscillator Characteristics

Table 32-48. 32.768kHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V _{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

32.2.13.2 Calibrated 2MHz RC Internal Oscillator Characteristics

Table 32-49. 2MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8	2.0	2.2	MHz
	Factory calibrated frequency			2.0		
	Factory calibration accuracy	T = 85°C, V _{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration stepsize			0.18		

32.2.13.3 Calibrated 32MHz Internal Oscillator Characteristics

Table 32-50. 32MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30	32	55	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 85°C, V _{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration step size			0.19		

32.2.13.4 32kHz Internal ULP Oscillator Characteristics

Table 32-51. 32kHz Internal ULP Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			32		kHz
	Factory calibration accuracy	T = 85°C, V _{CC} = 3.0V	-12		12	%
	Accuracy		-30		30	

32.2.13.5 Internal Phase Locked Loop (PLL) Characteristics

Table 32-52. Internal PLL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency ⁽¹⁾	$V_{CC} = 1.6 - 1.8V$	20		48	
		$V_{CC} = 2.7 - 3.6V$	20		128	
	Start-up time			25		μs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

32.2.13.6 External Clock Characteristics

Figure 32-10. External Clock Drive Waveform

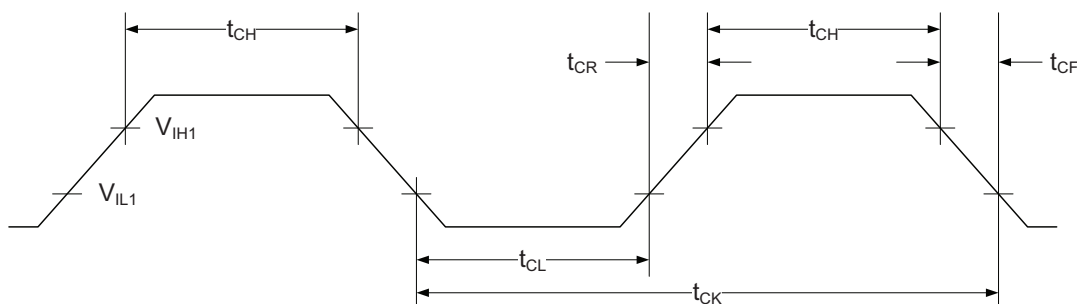


Table 32-53. External Clock used as System Clock without Prescaling

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency ⁽¹⁾	$V_{CC} = 1.6 - 1.8V$	0		12	MHz
		$V_{CC} = 2.7 - 3.6V$	0		32	
t_{CK}	Clock Period	$V_{CC} = 1.6 - 1.8V$	83.3			ns
		$V_{CC} = 2.7 - 3.6V$	31.5			
t_{CH}	Clock High Time	$V_{CC} = 1.6 - 1.8V$	30.0			
		$V_{CC} = 2.7 - 3.6V$	12.5			
t_{CL}	Clock Low Time	$V_{CC} = 1.6 - 1.8V$	30.0			
		$V_{CC} = 2.7 - 3.6V$	12.5			
t_{CR}	Rise Time (for maximum frequency)	$V_{CC} = 1.6 - 1.8V$			10	
		$V_{CC} = 2.7 - 3.6V$			3	
t_{CF}	Fall Time (for maximum frequency)	$V_{CC} = 1.6 - 1.8V$			10	
		$V_{CC} = 2.7 - 3.6V$			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

32.3.13 Clock and Oscillator Characteristics

32.3.13.1 Calibrated 32.768kHz Internal Oscillator Characteristics

Table 32-77. 32.768kHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V _{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

32.3.13.2 Calibrated 2MHz RC Internal Oscillator Characteristics

Table 32-78. 2MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8	2.0	2.2	MHz
	Factory calibrated frequency			2.0		
	Factory calibration accuracy	T = 85°C, V _{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration stepsize			0.18		

32.3.13.3 Calibrated 32MHz Internal Oscillator Characteristics

Table 32-79. 32MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30	32	55	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 85°C, V _{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration step size			0.2		

32.3.13.4 32kHz Internal ULP Oscillator Characteristics

Table 32-80. 32kHz Internal ULP Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			32		kHz
	Factory calibration accuracy	T = 85°C, V _{CC} = 3.0V	-12		12	%
	Accuracy		-30		30	

Table 32-97. Accuracy Characteristics

Symbol	Parameter	Condition ⁽²⁾		Min.	Typ.	Max.	Units
RES	Resolution	12-bit resolution	Differential	8	12	12	Bits
			Single ended signed	7	11	11	
			Single ended unsigned	8	12	12	
INL ⁽¹⁾	Integral non-linearity	Differential mode	16ksps, $V_{REF} = 3V$		0.5	1	lsb
			16ksps, all V_{REF}		0.8	2	
			300ksps, $V_{REF} = 3V$		0.6	1	
			300ksps, all V_{REF}		1	2	
		Single ended unsigned mode	16ksps, $V_{REF} = 3.0V$		0.5	1	
			16ksps, all V_{REF}		1.3	2	
DNL ⁽¹⁾	Differential non-linearity	Differential mode	16ksps, $V_{REF} = 3V$		0.3	1	lsb
			16ksps, all V_{REF}		0.5	1	
			300ksps, $V_{REF} = 3V$		0.3	1	
			300ksps, all V_{REF}		0.5	1	
		Single ended unsigned mode	16ksps, $V_{REF} = 3.0V$		0.6	1	
			16ksps, All V_{REF}		0.6	1	
	Offset error	Differential mode	300ksps, $V_{REF} = 3V$		-7		mV
			Temperature drift, $V_{REF} = 3V$		0.01		mV/K
			Operating voltage drift		0.16		mV/V
	Gain error	Differential mode	External reference		-5		mV
			$AV_{CC}/1.6$		-5		
			$AV_{CC}/2.0$		-6		
			Bandgap		± 10		
			Temperature drift		0.02		mV/K
			Operating voltage drift		2		mV/V
	Gain error	Single ended unsigned mode	External reference		-8		mV
			$AV_{CC}/1.6$		-8		
			$AV_{CC}/2.0$		-8		
			Bandgap		± 10		
			Temperature drift		0.03		mV/K
			Operating voltage drift		2		mV/V

Notes: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

2. Unless otherwise noted all linearity, offset, and gain error numbers are valid under the condition that external V_{REF} is used.

32.4.13.5 Internal Phase Locked Loop (PLL) Characteristics

Table 32-110. Internal PLL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency ⁽¹⁾	$V_{CC} = 1.6 - 1.8V$	20		48	
		$V_{CC} = 2.7 - 3.6V$	20		128	
	Start-up time			25		μs
	Re-lock time			25		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

32.4.13.6 External Clock Characteristics

Figure 32-24. External Clock Drive Waveform

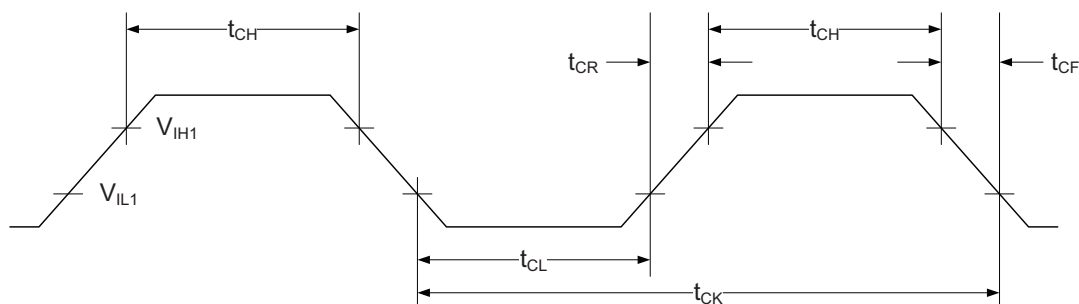


Table 32-111. External Clock used as System Clock without Prescaling

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency ⁽¹⁾	$V_{CC} = 1.6 - 1.8V$	0		12	MHz
		$V_{CC} = 2.7 - 3.6V$	0		32	
t_{CK}	Clock Period	$V_{CC} = 1.6 - 1.8V$	83.3			ns
		$V_{CC} = 2.7 - 3.6V$	31.5			
t_{CH}	Clock High Time	$V_{CC} = 1.6 - 1.8V$	30.0			
		$V_{CC} = 2.7 - 3.6V$	12.5			
t_{CL}	Clock Low Time	$V_{CC} = 1.6 - 1.8V$	30.0			
		$V_{CC} = 2.7 - 3.6V$	12.5			
t_{CR}	Rise Time (for maximum frequency)	$V_{CC} = 1.6 - 1.8V$			10	
		$V_{CC} = 2.7 - 3.6V$			3	
t_{CF}	Fall Time (for maximum frequency)	$V_{CC} = 1.6 - 1.8V$			10	
		$V_{CC} = 2.7 - 3.6V$			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

Table 32-112.External Clock with Prescaler ⁽¹⁾ for System Clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
1/t _{CK}	Clock Frequency ⁽²⁾	V _{CC} = 1.6 - 1.8V	0		90	MHz
		V _{CC} = 2.7 - 3.6V	0		142	
t _{CK}	Clock Period	V _{CC} = 1.6 - 1.8V	11			ns
		V _{CC} = 2.7 - 3.6V	7			
t _{CH}	Clock High Time	V _{CC} = 1.6 - 1.8V	4.5			
		V _{CC} = 2.7 - 3.6V	2.4			
t _{CL}	Clock Low Time	V _{CC} = 1.6 - 1.8V	4.5			
		V _{CC} = 2.7 - 3.6V	2.4			
t _{CR}	Rise Time (for maximum frequency)	V _{CC} = 1.6 - 1.8V			1.5	
		V _{CC} = 2.7 - 3.6V			1.0	
t _{CF}	Fall Time (for maximum frequency)	V _{CC} = 1.6 - 1.8V			1.5	
		V _{CC} = 2.7 - 3.6V			1.0	
Δt _{CK}	Change in period from one clock cycle to the next				10	%

- Notes:
1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
 2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

32.4.13.7 External 16MHz Crystal Oscillator and XOSC Characteristics

Table 32-113. External 16MHz Crystal Oscillator and XOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0	0		ns
			FRQRANGE=1, 2, or 3	0		
		XOSCPWR=1		0		
	Long term jitter	XOSCPWR=0	FRQRANGE=0	0		
			FRQRANGE=1, 2, or 3	0		
		XOSCPWR=1		0		
	Frequency error	XOSCPWR=0	FRQRANGE=0	0.03		%
			FRQRANGE=1	0.03		
			FRQRANGE=2 or 3	0.03		
		XOSCPWR=1		0.003		
	Duty cycle	XOSCPWR=0	FRQRANGE=0	50		
			FRQRANGE=1	50		
			FRQRANGE=2 or 3	50		
		XOSCPWR=1		50		

Figure 33-104. INL Error vs. Input Code

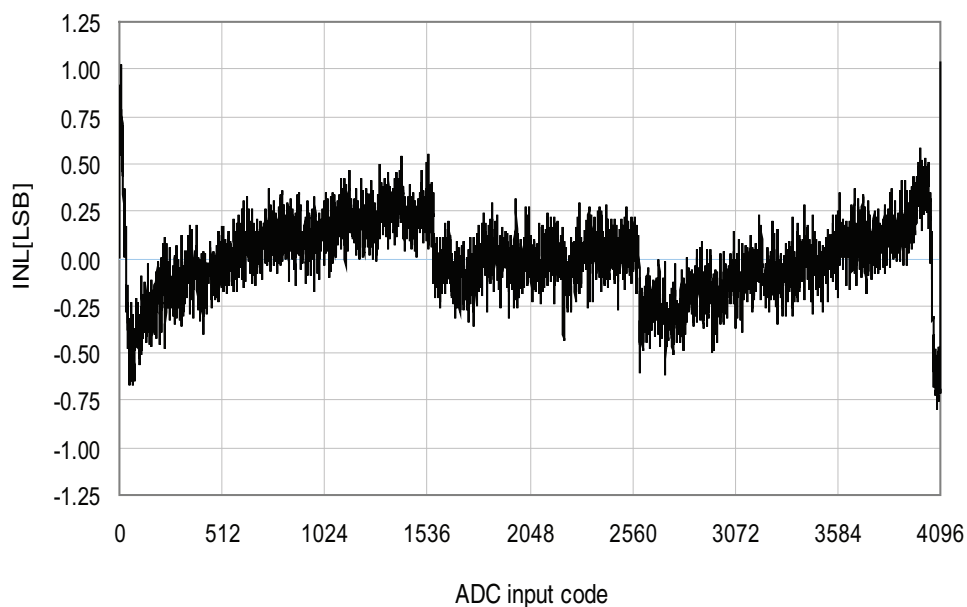


Figure 33-105. DNL Error vs. External V_{REF}
 $T = 25^{\circ}\text{C}$, $V_{CC} = 3.6\text{V}$, external reference

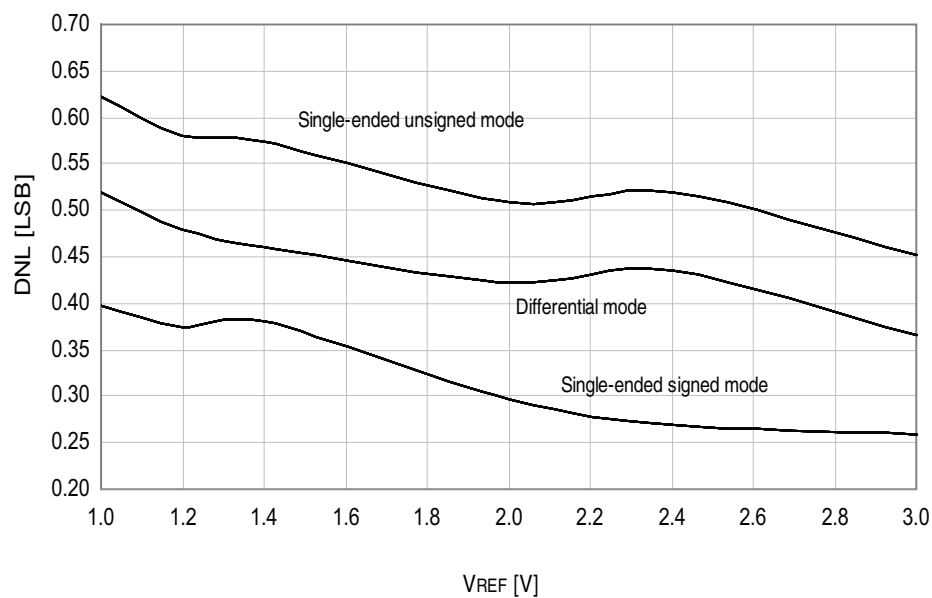
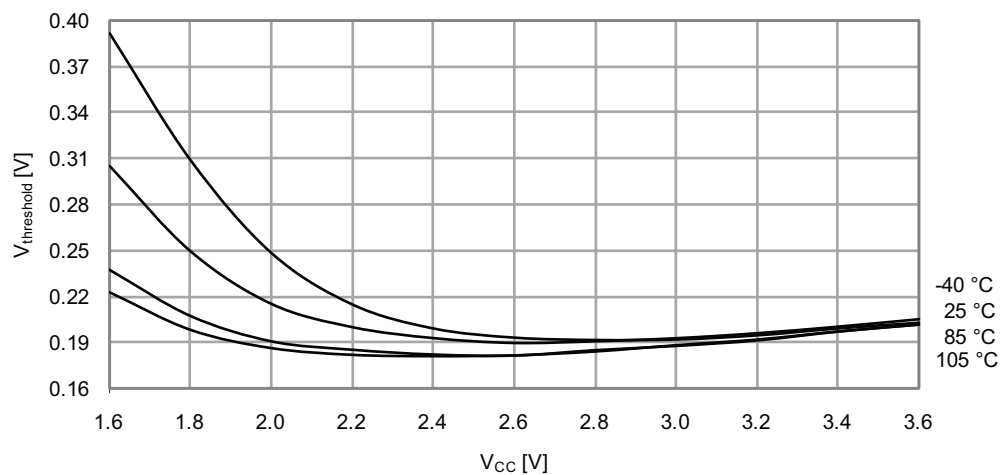


Figure 33-241. I/O Pin Input Hysteresis vs. V_{CC}



33.4.3 ADC Characteristics

Figure 33-242. INL Error vs. External V_{REF}

$T = 25^{\circ}\text{C}$, $V_{CC} = 3.6\text{V}$, external reference

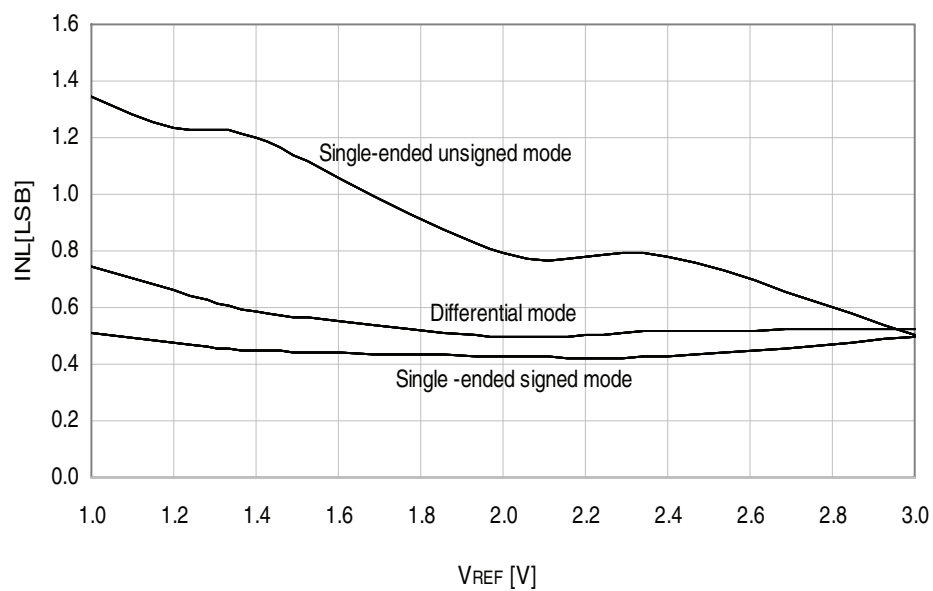


Figure 33-273. 32MHz Internal Oscillator CALA Calibration Step Size

$T = -40^{\circ}\text{C}$, $V_{CC} = 3.0\text{V}$

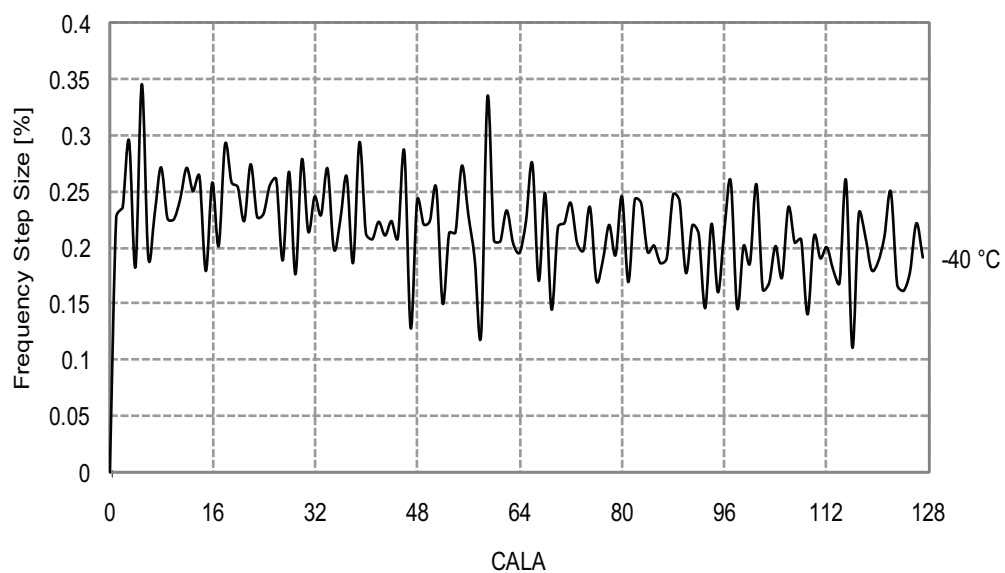


Figure 33-274. 32MHz Internal Oscillator CALA Calibration Step Size

$T = 25^{\circ}\text{C}$, $V_{CC} = 3.0\text{V}$

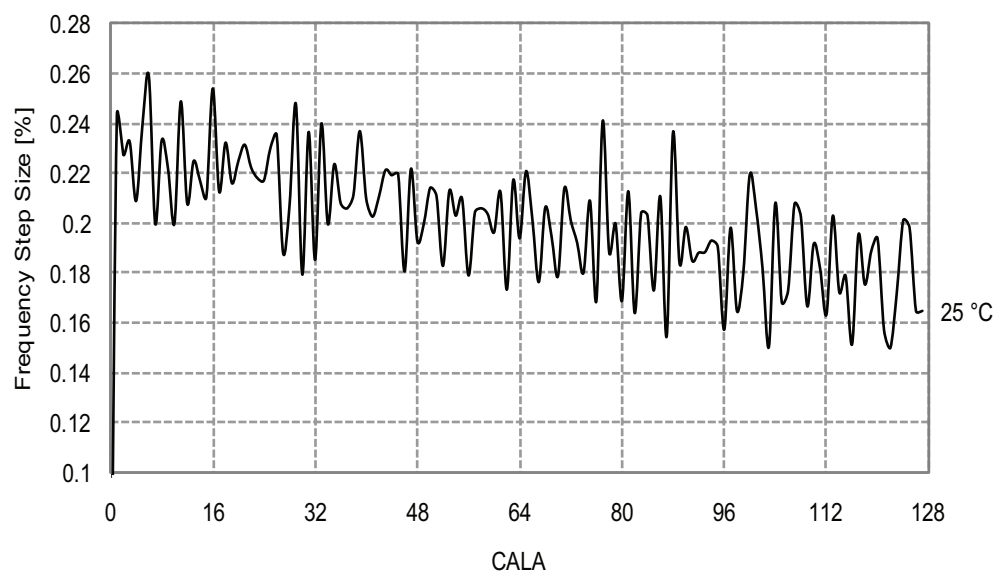
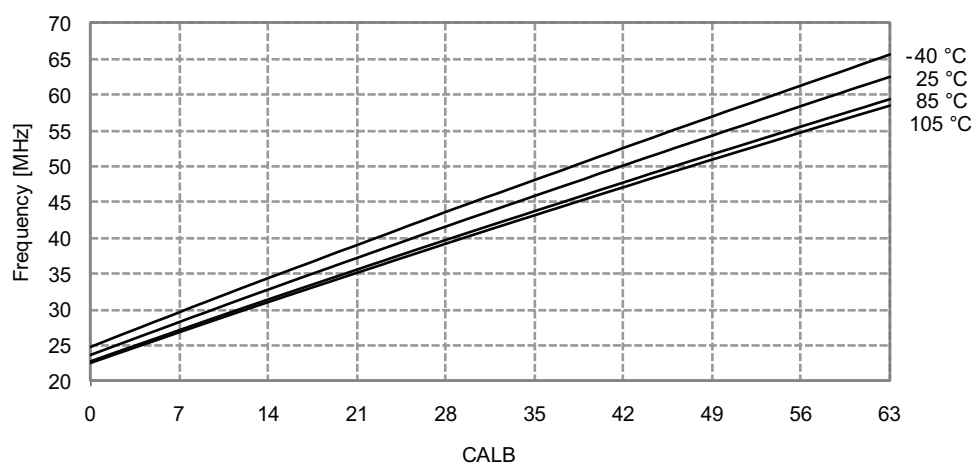


Figure 33-277. 32MHz Internal Oscillator Frequency vs. CALB Calibration Value

$V_{CC} = 3.0V$



33.4.8.5 32MHz Internal Oscillator Calibrated to 48MHz

Figure 33-278. 48MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled

32MHz internal oscillator frequency vs. temperature
Using 48MHz calibration value from signature row. DFLL disabled

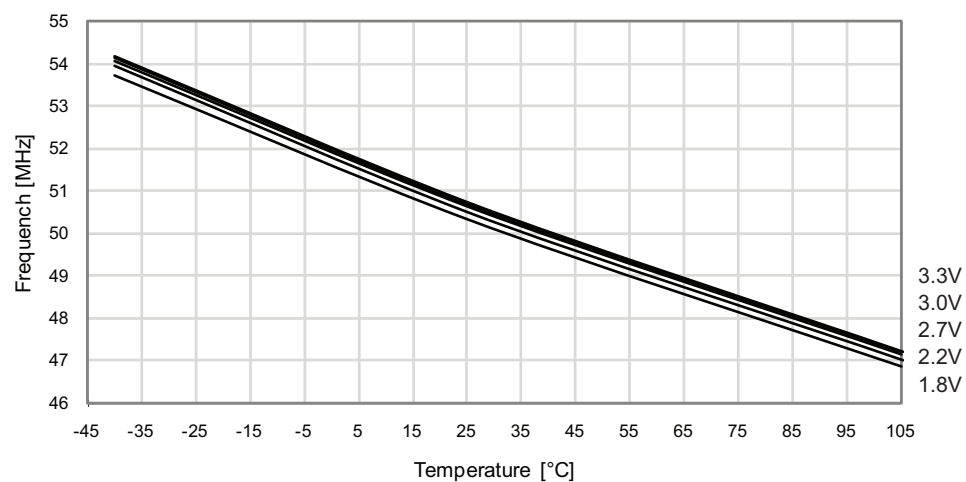
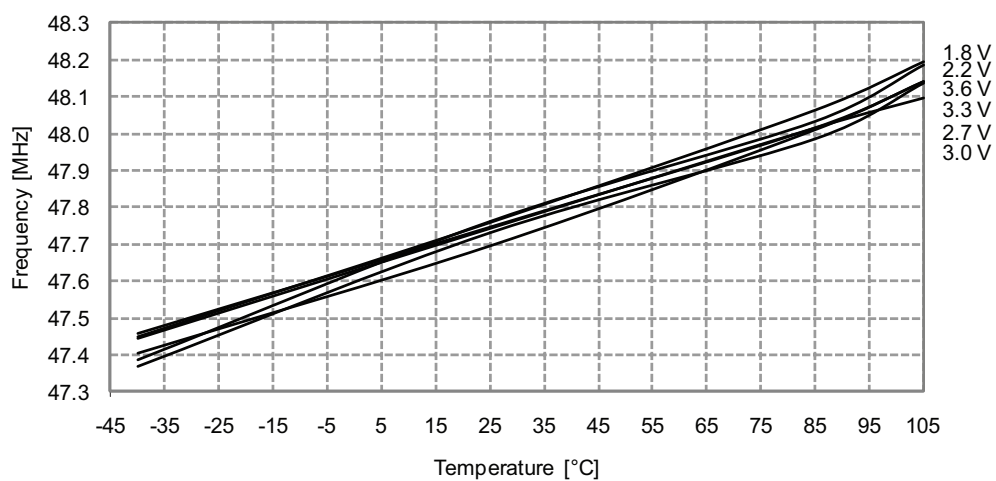
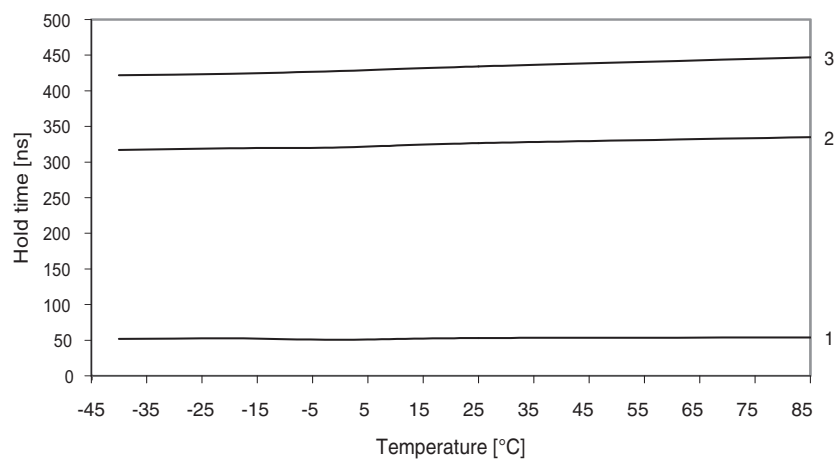


Figure 33-349. 48MHz Internal Oscillator Frequency vs. Temperature
DFLL enabled, from the 32.768kHz internal oscillator



33.5.9 Two-Wire Interface Characteristics

Figure 33-350. SDA Hold Time vs. Temperature



33.6.2.3 Thresholds and Hysteresis

Figure 33-379. I/O Pin Input Threshold Voltage vs. V_{CC}
 V_{IH} I/O pin read as “1”

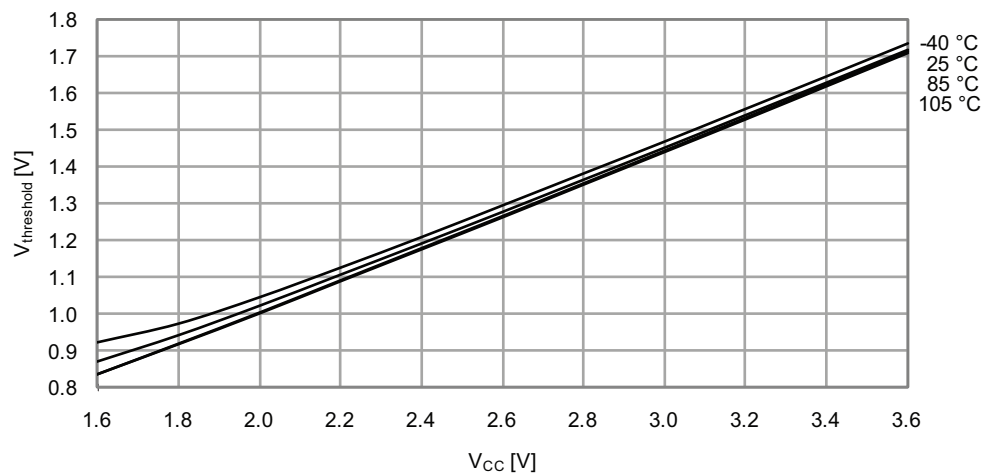
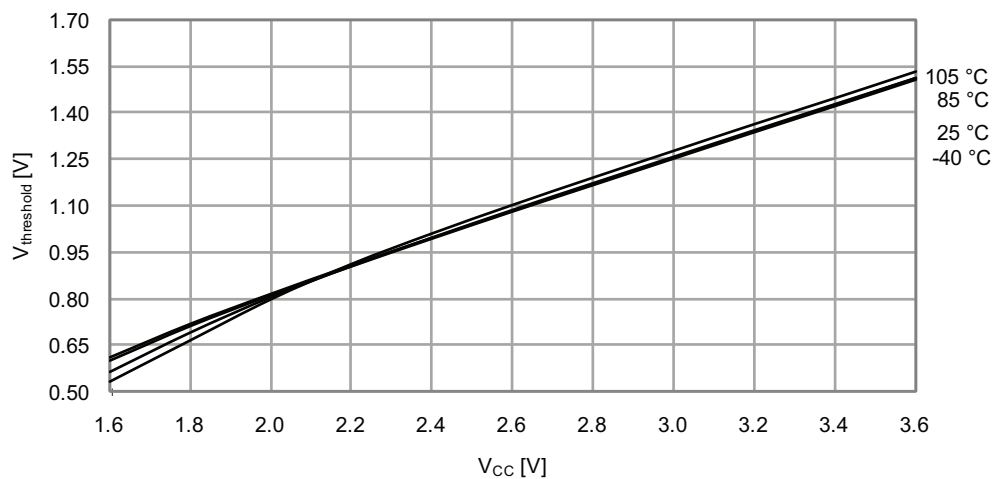


Figure 33-380. I/O Pin Input Threshold Voltage vs. V_{CC}
 V_{IL} I/O pin read as “0”



34.2.5 Rev. E

- Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously
- V_{CC} voltage scaler for AC is non-linear
- ADC gain stage cannot be used for single conversion
- ADC has increased INL error for some operating conditions
- ADC gain stage output range is limited to 2.4V
- ADC Event on compare match non-functional
- ADC propagation delay is not correct when $8\times - 64\times$ gain is used
- Bandgap measurement with the ADC is non-functional when V_{CC} is below 2.7V
- Accuracy lost on first three samples after switching input to ADC gain stage
- Configuration of PGM and CWCM not as described in the XMEGA D Manual
- PWM is not restarted properly after a fault in cycle-by-cycle mode
- BOD will be enabled at any reset
- EEPROM page buffer always written when NVM DATA0 is written
- Pending full asynchronous pin change interrupts will not wake the device
- Pin configuration does not affect Analog Comparator Output
- NMI Flag for Crystal Oscillator Failure automatically cleared
- RTC Counter value not correctly read after sleep
- Pending asynchronous RTC-interrupts will not wake up device
- TWI Transmit collision flag not cleared on repeated start
- Clearing TWI Stop Interrupt Flag may lock the bus
- TWI START condition at bus timeout will cause transaction to be dropped
- TWI Data Interrupt Flag (DIF) erroneously read as set
- WDR instruction inside closed window will not issue reset
- Non available functions and options
- Sampled BOD in Active mode will cause noise when bandgap is used as reference
- Temperature sensor not calibrated
- Disabling of the USART transmitter does not automatically set the TxD pin direction to input.

1. Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously

If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1 μ s and could potentially give a wrong comparison result.

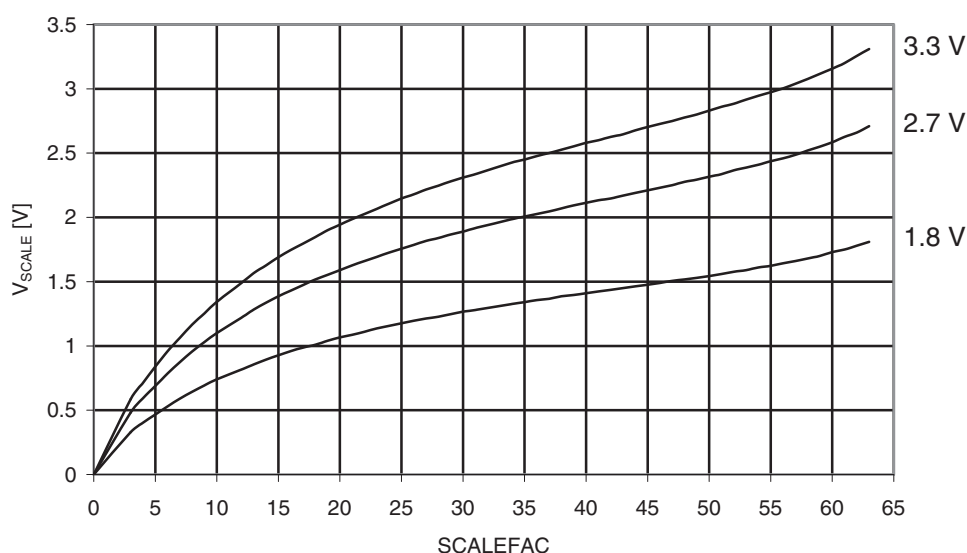
Problem fix/workaround

If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. V_{CC} voltage scaler for AC is non-linear

The 6-bit V_{CC} voltage scaler in the Analog Comparators is non-linear.

Figure 34-2. Analog Comparator Voltage Scaler vs. Scalefac
 $T = 25^{\circ}\text{C}$



Problem fix/workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed.

3. ADC gain stage cannot be used for single conversion

The ADC gain stage will not output correct result for single conversion that is triggered and started from software or event system.

Problem fix/workaround

When the gain stage is used, the ADC must be set in free running mode for correct results.

4. ADC has increased INL error for some operating conditions

Some ADC configurations or operating condition will result in increased INL error.

In signed mode INL is increased to:

6LSB for sample rates above 130ksps, and up to 8LSB for 200ksps sample rate.

6LSB for reference voltage below 1.1V when V_{CC} is above 3.0V.

20LSB for ambient temperature below 0°C and reference voltage below 1.3V.

In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

Problem fix/workaround

None, avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

5. ADC gain stage output range is limited to 2.4V

The amplified output of the ADC gain stage will never go above 2.4V, hence the differential input will only give correct output when below $2.4\text{V}/\text{gain}$. For the available gain settings, this gives a differential input range of:

```

        if ( !(COMMS_PORT.IN & PIN1_bm) )
            if ( !(COMMS_PORT.IN & PIN1_bm) )
                break;
    }
    /* Check for an pending address match interrupt */
    if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
    {
        /* Safely clear interrupt flag */
        COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
    }

```

21. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

Problem fix/workaround

None.

22. TWI Data Interrupt Flag erroneously read as set

When issuing the TWI slave response command CMD=0b11, it takes one Peripheral Clock cycle to clear the data interrupt flag (DIF). A read of DIF directly after issuing the command will show the DIF still set.

Problem fix/workaround

Add one NOP instruction before checking DIF.

23. WDR instruction inside closed window will not issue reset

When a WDR instruction is execute within one ULP clock cycle after updating the window control register, the counter can be cleared without giving a system reset.

Problem fix/workaround

Wait at least one ULP clock cycle before executing a WDR instruction.

24. Non available functions and options

The below function and options are not available. Writing to any registers or fuse to try and enable or configure these functions or options will have no effect, and will be as writing to a reserved address location.

- TWIE, the TWI module on PORTE
- TWI SDAHOLD option in the TWI CTRL register is one bit
- CRC generator module
- ADC 1/2× gain option, and this configuration option in the GAIN bits in the ADC Channel CTRL register
- ADC VCC/2 reference option and this configuration option in the REFSEL bits on the ADC REFCTRL register
- ADC option to use internal Gnd as negative input in differential measurements and this configuration option in the MUXNEG bits in the ADC Channel MUXCTRL register
- ADC channel scan and the ADC SCAN register
- ADC current limitation option, and the CURRLIMIT bits in the ADC CTRLB register
- ADC impedance mode selection for the gain stage, and the IMPMODE bit in the ADC CTRLB register
- Timer/Counter 2 and the SPLITMODE configuration option in the BYTEM bits in the Timer/Counter 0 CTRL register
- Analog Comparator (AC) current output option, and the AC CURRCTRL and CURRCALIB registers

35. Datasheet revision history

Note that the referring page numbers in this section are referred to this document. The referring revisions in this section are referring to the document revision.

35.1 8134Q – 10/2015

1.	Updated “Ordering Information” on page 2 . <ul style="list-style-type: none">• All ATxmegayyD3-MT and ATxmegayyD3-MTR changed respectively to ATxmegayyD3-MN and ATxmegayyD3-MNR
----	--

35.2 8134P – 11/2014

1.	Changed EEPROM value for ATxmega32D3 to 1K in Section 1. “Ordering Information” on page 2 , in Figure 7-2 on page 16 and in Table 7-3 on page 18 .
2.	Section naming in Chapter “Typical Characteristics” has been corrected.

35.3 8134O – 09/2014

1.	Updated “Ordering Information” on page 2 . Added Ordering codes for the devices characterized @ 105°C.
2.	Updated “Electrical Characteristics” on page 63 : <ul style="list-style-type: none">• Updated Table 32-4 on page 65, Table 32-33 on page 84, Table 32-62 on page 103, Table 32-91 on page 122, Table 32-120 on page 141 and Table 32-149 on page 160. Added I_{CC} Power-down power consumption for T=105°C for all functions disabled and for WDT and sampled BOD enabled.• Updated, Table 32-17 on page 73, Table 32-46 on page 92, Table 32-75 on page 111, Table 32-104 on page 130, Table 32-133 on page 149, and Table 32-162 on page 168. Updated all tables to include values for T=85°C and T=105°C. Removed T=55°C.
3.	Updated “Typical Characteristics” on page 177 . Added 105°C characteristics.
4.	Changed V _{CC} to AV _{CC} in Section 25. “ADC – 12-bit Analog to Digital Converter” on page 45 and Section 26. “AC – Analog Comparator” on page 47 .
5.	Added ERRATA concerning disabling of the USART transmitter in Section 34.2 “Atmel ATxmega64D3” on page 389 , Section 34.3 “Atmel ATxmega128D3” on page 405 and Section 34.5 “Atmel ATxmega256D3” on page 437 .

35.4 8134N – 03/2014

1.	Updated Table 28-2 on page 52 . PORT PB1 has PIN# 7
----	---