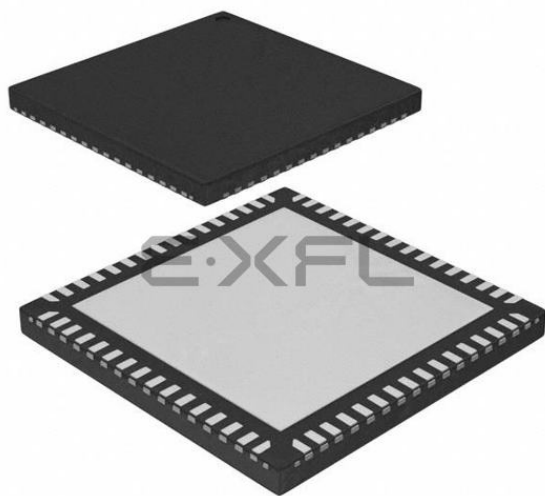




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Details

Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64d3-mhr

The production signature row cannot be written or erased, but it can be read from application software and external programmers.

Table 7-1. Device ID Bytes

Device	Device ID bytes		
	Byte 2	Byte 1	Byte 0
ATxmega32D3	4A	95	1E
ATxmega64D3	4A	96	1E
ATxmega128D3	48	97	1E
ATxmega192D3	49	97	1E
ATxmega256D3	44	98	1E
ATxmega384D3	47	98	1E

7.3.5 User Signature Row

The user signature row is a separate memory section that is fully accessible (read and write) from application software and external programmers. It is one flash page in size, and is meant for static user parameter storage, such as calibration data, custom serial number, identification numbers, random number seeds, etc. This section is not erased by chip erase commands that erase the flash, and requires a dedicated erase command. This ensures parameter storage during multiple program/erase operations and on-chip debug sessions.

7.4 Fuses and Lock Bits

The fuses are used to configure important system functions, and can only be written from an external programmer. The application software can read the fuses. The fuses are used to configure reset sources such as brownout detector and watchdog, and startup configuration.

The lock bits are used to set protection levels for the different flash sections (that is, if read and/or write access should be blocked). Lock bits can be written by external programmers and application software, but only to stricter protection levels. Chip erase is the only way to erase the lock bits. To ensure that flash contents are protected even during chip erase, the lock bits are erased after the rest of the flash memory has been erased.

An unprogrammed fuse or lock bit will have the value one, while a programmed fuse or lock bit will have the value zero. Both fuses and lock bits are reprogrammable like the flash program memory.

7.5 Data Memory

The data memory contains the I/O memory, internal SRAM, optionally memory mapped EEPROM, and external memory if available. The data memory is organized as one continuous memory section, see [Figure 7-2 on page 16](#). To simplify development, I/O Memory, EEPROM and SRAM will always have the same start addresses for all Atmel AVR XMEGA devices.

Figure 7-2. Data Memory Map (hexadecimal address)

Byte address	ATxmega32D3
0	I/O registers (4K)
FFF	
1000	EEPROM (1K)
17FF	
	RESERVED
2000	Internal SRAM (4K)
2FFF	

Byte address	ATxmega64D3
0	I/O registers (4K)
FFF	
1000	EEPROM (2K)
17FF	
	RESERVED
2000	Internal SRAM (4K)
2FFF	

Byte address	ATxmega128D3
0	I/O registers (4K)
FFF	
1000	EEPROM (2K)
17FF	
	RESERVED
2000	Internal SRAM (8K)
3FFF	

Byte address	ATxmega192D3
0	I/O registers (4K)
FFF	
1000	EEPROM (2K)
17FF	
	RESERVED
2000	Internal SRAM (16K)
5FFF	

Byte address	ATxmega256D3
0	I/O registers (4K)
FFF	
1000	EEPROM (4K)
1FFF	
2000	Internal SRAM (16K)
5FFF	

Byte address	ATxmega384D3
0	I/O registers (4K)
FFF	
1000	EEPROM (4K)
1FFF	
2000	Internal SRAM (32K)
9FFF	

7.6 EEPROM

All devices have EEPROM for nonvolatile data storage. It is either addressable in a separate data space (default) or memory mapped and accessed in normal data space. The EEPROM supports both byte and page access. Memory mapped EEPROM allows highly efficient EEPROM reading and EEPROM buffer loading. When doing this, EEPROM is accessible using load and store instructions. Memory mapped EEPROM will always start at hexadecimal address 0x1000.

12. WDT – Watchdog Timer

12.1 Features

- Issues a device reset if the timer is not reset before its timeout period
- Asynchronous operation from dedicated oscillator
- 1kHz output of the 32kHz ultra low power oscillator
- 11 selectable timeout periods, from 8ms to 8s
- Two operation modes:
 - Normal mode
 - Window mode
- Configuration lock to prevent unwanted changes

12.2 Overview

The watchdog timer (WDT) is a system function for monitoring correct program operation. It makes it possible to recover from error situations such as runaway or deadlocked code. The WDT is a timer, configured to a predefined timeout period, and is constantly running when enabled. If the WDT is not reset within the timeout period, it will issue a microcontroller reset. The WDT is reset by executing the WDR (watchdog timer reset) instruction from the application code.

The window mode makes it possible to define a time slot or window inside the total timeout period during which WDT must be reset. If the WDT is reset outside this window, either too early or too late, a system reset will be issued. Compared to the normal mode, this can also catch situations where a code error causes constant WDR execution.

The WDT will run in active mode and all sleep modes, if enabled. It is asynchronous, runs from a CPU-independent clock source, and will continue to operate to issue a system reset even if the main clocks fail.

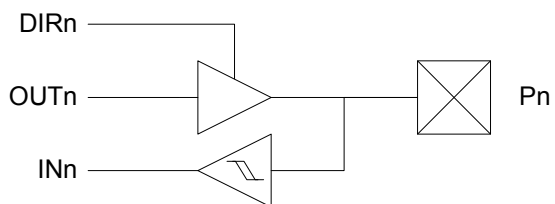
The configuration change protection mechanism ensures that the WDT settings cannot be changed by accident. For increased safety, a fuse for locking the WDT settings is also available.

14.3 Output Driver

All port pins (P_n) have programmable output configuration.

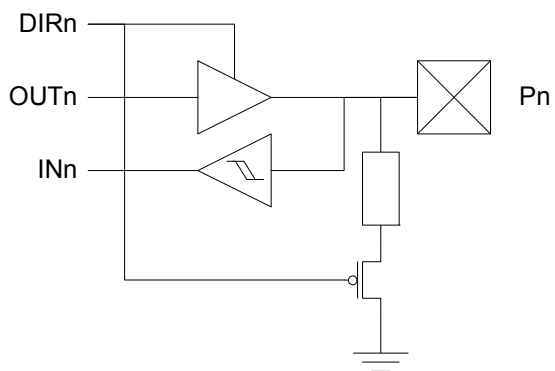
14.3.1 Push-pull

Figure 14-1. I/O Configuration - Totem-pole



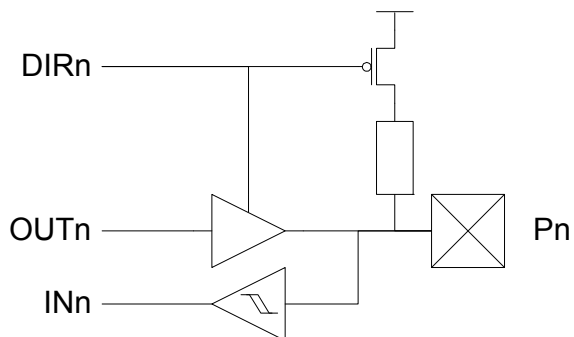
14.3.2 Pull-down

Figure 14-2. I/O Configuration - Totem-pole with Pull-down (on input)



14.3.3 Pull-up

Figure 14-3. I/O Configuration - Totem-pole with Pull-up (on input)



17. AWeX – Advanced Waveform Extension

17.1 Features

- Waveform output with complementary output from each compare channel
- Four dead-time insertion (DTI) units
 - 8-bit resolution
 - Separate high and low side dead-time setting
 - Double buffered dead time
 - Optionally halts timer during dead-time insertion
- Pattern generation unit creating synchronised bit pattern across the port pins
 - Double buffered pattern generation
 - Optional distribution of one compare channel output across the port pins
- Event controlled fault protection for instant and predictable fault triggering

17.2 Overview

The advanced waveform extension (AWeX) provides extra functions to the timer/counter in waveform generation (WG) modes. It is primarily intended for use with different types of motor control and other power control applications. It enables low- and high side output with dead-time insertion and fault protection for disabling and shutting down external drivers. It can also generate a synchronized bit pattern across the port pins.

Each of the waveform generator outputs from the timer/counter 0 are split into a complimentary pair of outputs when any AWeX features are enabled. These output pairs go through a dead-time insertion (DTI) unit that generates the non-inverted low side (LS) and inverted high side (HS) of the WG output with dead-time insertion between LS and HS switching. The DTI output will override the normal port value according to the port override setting.

The pattern generation unit can be used to generate a synchronized bit pattern on the port it is connected to. In addition, the WG output from compare channel A can be distributed to and override all the port pins. When the pattern generator unit is enabled, the DTI unit is bypassed.

The fault protection unit is connected to the event system, enabling any event to trigger a fault condition that will disable the AWeX output. The event system ensures predictable and instant fault reaction, and gives flexibility in the selection of fault triggers.

The AWeX is available for TCC0. The notation of this is AWEXC.

19. RTC – 16-bit Real-Time Counter

19.1 Features

- 16-bit resolution
- Selectable clock source
 - 32.768kHz external crystal
 - External clock
 - 32.768kHz internal oscillator
 - 32kHz internal ULP oscillator
- Programmable 10-bit clock prescaling
- One compare register
- One period register
- Clear counter on period overflow
- Optional interrupt/event on overflow and compare match

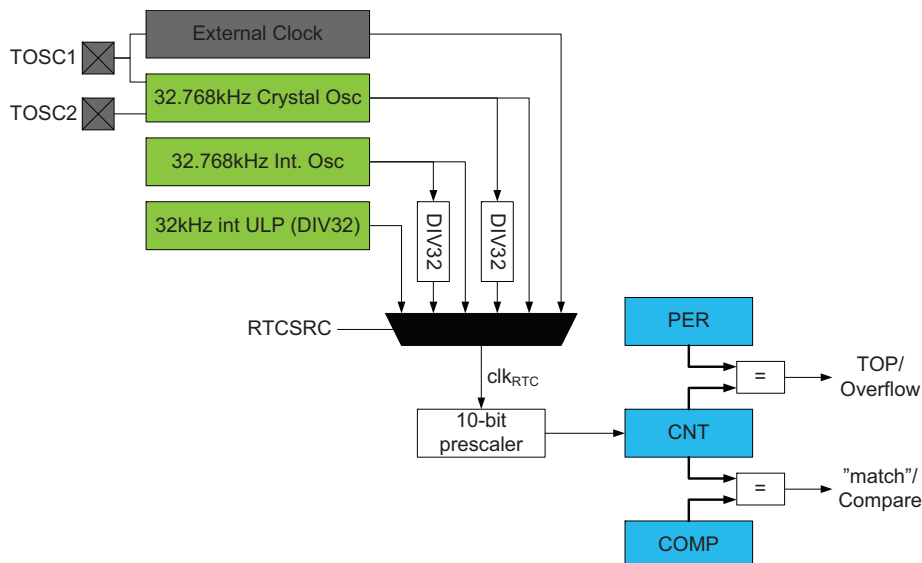
19.2 Overview

The 16-bit real-time counter (RTC) is a counter that typically runs continuously, including in low-power sleep modes, to keep track of time. It can wake up the device from sleep modes and/or interrupt the device at regular intervals.

The reference clock is typically the 1.024kHz output from a high-accuracy crystal of 32.768kHz, and this is the configuration most optimized for low power consumption. The faster 32.768kHz output can be selected if the RTC needs a resolution higher than 1ms. The RTC can also be clocked from an external clock signal, the 32.768kHz internal oscillator or the 32kHz internal ULP oscillator.

The RTC includes a 10-bit programmable prescaler that can scale down the reference clock before it reaches the counter. A wide range of resolutions and time-out periods can be configured. With a 32.768kHz clock source, the maximum resolution is 30.5 μ s, and time-out periods can range up to 2000 seconds. With a resolution of 1s, the maximum timeout period is more than 18 hours (65536 seconds). The RTC can give a compare interrupt and/or event when the counter equals the compare register value, and an overflow interrupt and/or event when it equals the period register value.

Figure 19-1. Real-time Counter Overview



32.2.8 Bandgap and Internal 1.0V Reference Characteristics

Table 32-42. Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC	1 Clk _{PER} + 2.5μs			μs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T = 85°C, after calibration	0.99	1	1.01	
	Variation over voltage and temperature	Calibrated at T = 85°C		1		%

32.2.9 Brownout Detection Characteristics

Table 32-43. Brownout Detection Characteristics ⁽¹⁾

Symbol	Parameter (BOD level 0 at 85°C)	Condition	Min.	Typ.	Max.	Units
V _{BOT}	BOD level 0 falling V _{CC}		1.40	1.60	1.70	V
	BOD level 1 falling V _{CC}			1.8		
	BOD level 2 falling V _{CC}			2.0		
	BOD level 3 falling V _{CC}			2.2		
	BOD level 4 falling V _{CC}			2.4		
	BOD level 5 falling V _{CC}			2.6		
	BOD level 6 falling V _{CC}			2.8		
	BOD level 7 falling V _{CC}			3.0		
t _{BOD}	Detection time	Continuous mode		0.4		μs
		Sampled mode		1000		
V _{HYST}	Hysteresis			1.0		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

32.2.10 External Reset Characteristics

Table 32-44. External Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t _{EXT}	Minimum reset pulse width		1000	90		ns
V _{RST}	Reset threshold voltage	V _{CC} = 2.7 - 3.6V		0.45 * V _{CC}		V
		V _{CC} = 1.6 - 2.7V		0.42 * V _{CC}		
R _{RST}	Reset pin pull-up resistor			25		kΩ

32.3.3 Current Consumption

Table 32-62. Current Consumption for Active Mode and Sleep Modes

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I _{CC}	Active power consumption ⁽¹⁾	32kHz, Ext. Clk	V _{CC} = 1.8V	55		μA
			V _{CC} = 3.0V	135		
		1MHz, Ext. Clk	V _{CC} = 1.8V	237		
			V _{CC} = 3.0V	515		
		2MHz, Ext. Clk	V _{CC} = 1.8V	425	700	mA
			V _{CC} = 3.0V	0.9	1.5	
	Idle power consumption ⁽¹⁾	32kHz, Ext. Clk	V _{CC} = 1.8V	2.8		μA
			V _{CC} = 3.0V	3.1		
		1MHz, Ext. Clk	V _{CC} = 1.8V	47		
			V _{CC} = 3.0V	95		
		2MHz, Ext. Clk	V _{CC} = 1.8V	94	200	mA
			V _{CC} = 3.0V	190	400	
	Power-down power consumption	T = 25°C	V _{CC} = 3.0V	0.1	1.0	μA
				1.9	4.0	
				4.0	8.0	
		T = 85°C	V _{CC} = 3.0V	1.5	2.0	
				3.0	8.0	
				5.0	10	
	Power-save power consumption ⁽²⁾	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V _{CC} = 1.8V	1.3		
			V _{CC} = 3.0V	1.4		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V _{CC} = 1.8V	0.7	2.0	
			V _{CC} = 3.0V	0.8	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V _{CC} = 1.8V	0.9	3.0	
			V _{CC} = 3.0V	1.1	3.0	
	Reset power consumption	Current through RESET pin subtracted	V _{CC} = 3.0V	145		

- Notes:
1. All Power Reduction Registers set.
 2. Maximum limits are based on characterization, and not tested in production.

32.3.5 I/O Pin Characteristics

The I/O pins complies with the JEDEC LVTTTL and LVCMOS specification and the high- and low level input and output voltage limits or exceeds this specification.

Table 32-65. I/O Pin Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
$I_{OH}^{(1)}/I_{OL}^{(2)}$	I/O pin source/sink current			-15		15	mA
V_{IH}	High level input voltage	$V_{CC} = 2.4 - 3.6V$		$0.7 * V_{CC}$		$V_{CC} + 0.5$	V
		$V_{CC} = 1.6 - 2.4V$		$0.8 * V_{CC}$		$V_{CC} + 0.5$	
V_{IL}	Low level input voltage	$V_{CC} = 2.4 - 3.6V$		-0.5		$0.3 * V_{CC}$	
		$V_{CC} = 1.6 - 2.4V$		-0.5		$0.2 * V_{CC}$	
V_{OH}	High level output voltage	$V_{CC} = 3.3V$	$I_{OH} = -4mA$	2.6	2.9		
		$V_{CC} = 3.0V$	$I_{OH} = -3mA$	2.1	2.6		
		$V_{CC} = 1.8V$	$I_{OH} = -1mA$	1.4	1.6		
V_{OL}	Low level output voltage	$V_{CC} = 3.3V$	$I_{OL} = 8mA$		0.4	0.76	
		$V_{CC} = 3.0V$	$I_{OL} = 5mA$		0.3	0.64	
		$V_{CC} = 1.8V$	$I_{OL} = 3mA$		0.2	0.46	
I_{IN}	Input leakage current I/O pin	$T = 25^{\circ}C$			<0.01	1.0	μA
R_P	Pull/buss keeper resistor				25		$k\Omega$

- Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
The sum of all I_{OH} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.
 2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
The sum of all I_{OL} for PORTC, PORTD, and PORTE must for each port not exceed 200mA.
The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR, and PDI must not exceed 100mA.

Table 32-87. Two-wire Interface Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7V_{CC}$		$V_{CC} + 0.5$	V
V_{IL}	Input low voltage		-0.5		$0.3V_{CC}$	
V_{hys}	Hysteresis of Schmitt trigger inputs		$0.05V_{CC}^{(1)}$			
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		$20 + 0.1C_b^{(1)(2)}$		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF^{(2)}$	$20 + 0.1C_b^{(1)(2)}$		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	μA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	SCL clock frequency	$f_{PER}^{(3)} > \max(10f_{SCL}, 250kHz)$	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC} - 0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold time (repeated) START condition	$f_{SCL} \leq 100kHz$	4.0			μs
		$f_{SCL} > 100kHz$	0.6			
t_{LOW}	Low period of SCL clock	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			
t_{HIGH}	High period of SCL clock	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100kHz$	4.7			μs
		$f_{SCL} > 100kHz$	0.6			
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq 100kHz$	0		3.45	
		$f_{SCL} > 100kHz$	0		0.9	
$t_{SU;DAT}$	Data setup time	$f_{SCL} \leq 100kHz$	250			
		$f_{SCL} > 100kHz$	100			
$t_{SU;STO}$	Setup time for STOP condition	$f_{SCL} \leq 100kHz$	4.0			μs
		$f_{SCL} > 100kHz$	0.6			
t_{BUF}	Bus free time between a STOP and START condition	$f_{SCL} \leq 100kHz$	4.7			μs
		$f_{SCL} > 100kHz$	1.3			

- Notes:
1. Required only for $f_{SCL} > 100kHz$.
 2. C_b = Capacitance of one bus line in pF.
 3. f_{PER} = Peripheral clock frequency.

32.4.8 Bandgap and Internal 1.0V Reference Characteristics

Table 32-100. Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC	1 Clk _{PER} + 2.5μs			μs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T = 85°C, after calibration	0.99	1.0	1.01	
	Variation over voltage and temperature	Calibrated at T = 85°C		1		%

32.4.9 Brownout Detection Characteristics

Table 32-101. Brownout Detection Characteristics ⁽¹⁾

Symbol	Parameter (BOD level 0 at 85°C)	Condition	Min.	Typ.	Max.	Units
V _{BOT}	BOD level 0 falling V _{CC}		1.40	1.60	1.70	V
	BOD level 1 falling V _{CC}			1.8		
	BOD level 2 falling V _{CC}			2.0		
	BOD level 3 falling V _{CC}			2.2		
	BOD level 4 falling V _{CC}			2.4		
	BOD level 5 falling V _{CC}			2.6		
	BOD level 6 falling V _{CC}			2.8		
	BOD level 7 falling V _{CC}			3.0		
t _{BOD}	Detection time	Continuous mode		0.4		μs
		Sampled mode		1000		
V _{HYST}	Hysteresis			1.0		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

32.4.10 External Reset Characteristics

Table 32-102. External Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t _{EXT}	Minimum reset pulse width		1000	90		ns
V _{RST}	Reset threshold voltage	V _{CC} = 2.7 - 3.6V		0.45 * V _{CC}		V
		V _{CC} = 1.6 - 2.7V		0.45 * V _{CC}		
R _{RST}	Reset pin pull-up resistor			25		kΩ

Table 32-155. Accuracy Characteristics

Symbol	Parameter	Condition ⁽¹⁾		Min.	Typ.	Max.	Units
RES	Resolution	12-bit resolution	Differential	8	12	12	Bits
			Single ended signed	7	11	11	
			Single ended unsigned	8	12	12	
INL ⁽²⁾	Integral non-linearity	Differential mode	16ksps, $V_{REF} = 3V$		0.5	1	lsb
			16ksps, all V_{REF}		0.8	2	
			300ksps, $V_{REF} = 3V$		0.6	1	
			300ksps, all V_{REF}		1	2	
		Single ended unsigned mode	16ksps, $V_{REF} = 3.0V$		0.5	1	
			16ksps, all V_{REF}		1.3	2	
DNL ⁽²⁾	Differential non-linearity	Differential mode	16ksps, $V_{REF} = 3V$		0.3	1	
			16ksps, all V_{REF}		0.5	1	
			300ksps, $V_{REF} = 3V$		0.35	1	
			300ksps, all V_{REF}		0.5	1	
		Single ended unsigned mode	16ksps, $V_{REF} = 3.0V$		0.6	1	
			16ksps, all V_{REF}		0.6	1	
	Offset error	Differential mode	300ksps, $V_{REF} = 3V$		-7		mV
			Temperature drift, $V_{REF} = 3V$		0.01		mV/K
			Operating voltage drift		0.16		mV/V
	Gain error	Differential mode	External reference		-5		mV
			$AV_{CC}/1.6$		-5		
			$AV_{CC}/2.0$		-6		
			Bandgap		±10		
			Temperature drift		0.02		mV/K
			Operating voltage drift		2		mV/V
	Gain error	Single ended unsigned mode	External reference		-8		mV
			$AV_{CC}/1.6$		-8		
			$AV_{CC}/2.0$		-8		
			Bandgap		±10		
			Temperature drift		0.03		mV/K
			Operating voltage drift		2		mV/V

- Notes:
1. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external V_{REF} is used.
 2. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

Table 32-170. External Clock with Prescaler ⁽¹⁾ for System Clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
1/t _{CK}	Clock Frequency ⁽²⁾	V _{CC} = 1.6 - 1.8V	0		90	MHz
		V _{CC} = 2.7 - 3.6V	0		142	
t _{CK}	Clock Period	V _{CC} = 1.6 - 1.8V	11			ns
		V _{CC} = 2.7 - 3.6V	7			
t _{CH}	Clock High Time	V _{CC} = 1.6 - 1.8V	4.5			
		V _{CC} = 2.7 - 3.6V	2.4			
t _{CL}	Clock Low Time	V _{CC} = 1.6 - 1.8V	4.5			
		V _{CC} = 2.7 - 3.6V	2.4			
t _{CR}	Rise Time (for maximum frequency)	V _{CC} = 1.6 - 1.8V			1.5	
		V _{CC} = 2.7 - 3.6V			1.0	
t _{CF}	Fall Time (for maximum frequency)	V _{CC} = 1.6 - 1.8V			1.5	
		V _{CC} = 2.7 - 3.6V			1.0	
Δt _{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

32.6.13.7 External 16MHz Crystal Oscillator and XOSC Characteristics

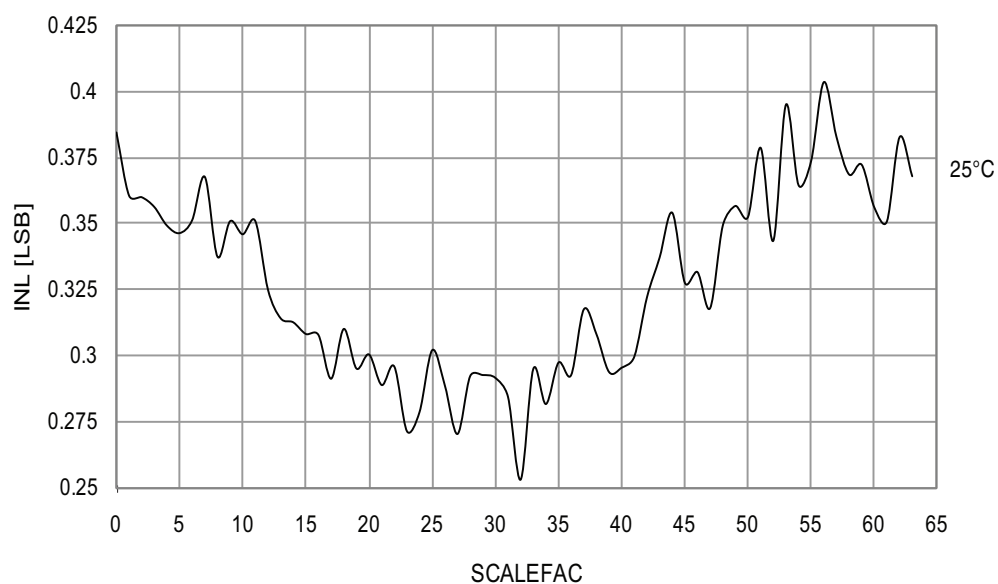
Table 32-171. External 16MHz Crystal Oscillator and XOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0	0		ns
			FRQRANGE=1, 2, or 3	0		
		XOSCPWR=1		0		
	Long term jitter	XOSCPWR=0	FRQRANGE=0	0		ns
			FRQRANGE=1, 2, or 3	0		
		XOSCPWR=1		0		
	Frequency error	XOSCPWR=0	FRQRANGE=0	0.03		%
			FRQRANGE=1	0.03		
			FRQRANGE=2 or 3	0.03		
		XOSCPWR=1		0.003		
	Duty cycle	XOSCPWR=0	FRQRANGE=0	50		%
			FRQRANGE=1	50		
			FRQRANGE=2 or 3	50		
		XOSCPWR=1		50		

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
R _Q	Negative impedance ⁽¹⁾	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF	44k		Ω
			1MHz crystal, CL=20pF	67k		
			2MHz crystal, CL=20pF	67k		
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal	82k		
			8MHz crystal	1500		
			9MHz crystal	1500		
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal	2700		
			9MHz crystal	2700		
			12MHz crystal	1000		
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal	3600		
			12MHz crystal	1300		
			16MHz crystal	590		
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal	390		
			12MHz crystal	50		
			16MHz crystal	10		
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal	1500		
			12MHz crystal	650		
			16MHz crystal	270		
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal	1000		
			16MHz crystal	440		
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal	1300		
			16MHz crystal	590		
	ESR	SF = safety factor			min(R _Q)/SF	kΩ
	Start-up time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF	1.0		ms
		XOSCPWR=0, FRQRANGE=1	2MHz crystal, CL=20pF	2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz crystal, CL=20pF	0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz crystal, CL=20pF	1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz crystal, CL=20pF	1.4		

Figure 33-116. Voltage Scaler INL vs. SCALEFAC

$T = 25^{\circ}\text{C}$, $V_{CC} = 3.0\text{V}$



33.2.5 Internal 1.0V Reference Characteristics

Figure 33-117. ADC Internal 1.0V Reference vs. Temperature

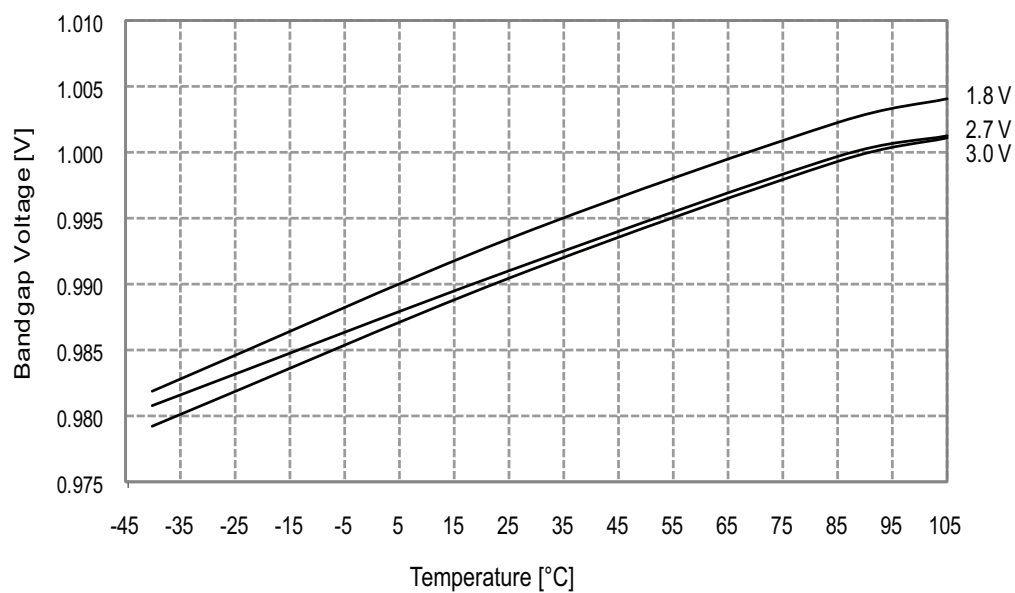


Figure 33-179. Gain Error vs. V_{CC}

$T = 25^{\circ}\text{C}$, $V_{REF} = \text{external } 1.0\text{V}$, ADC sample rate = 300ksps

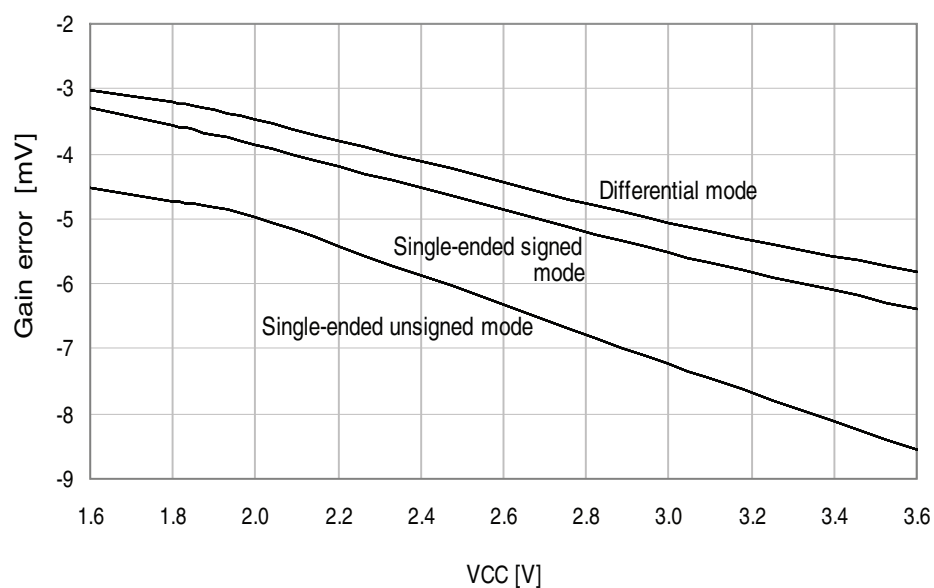


Figure 33-180. Offset Error vs. V_{REF}

$T = 25^{\circ}\text{C}$, $V_{CC} = 3.6\text{V}$, ADC sample rate = 300ksps

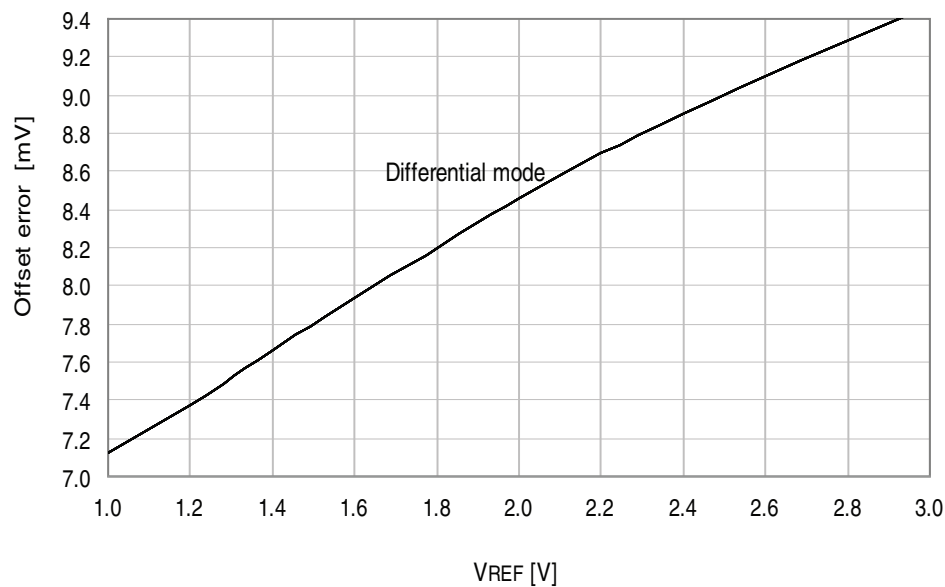
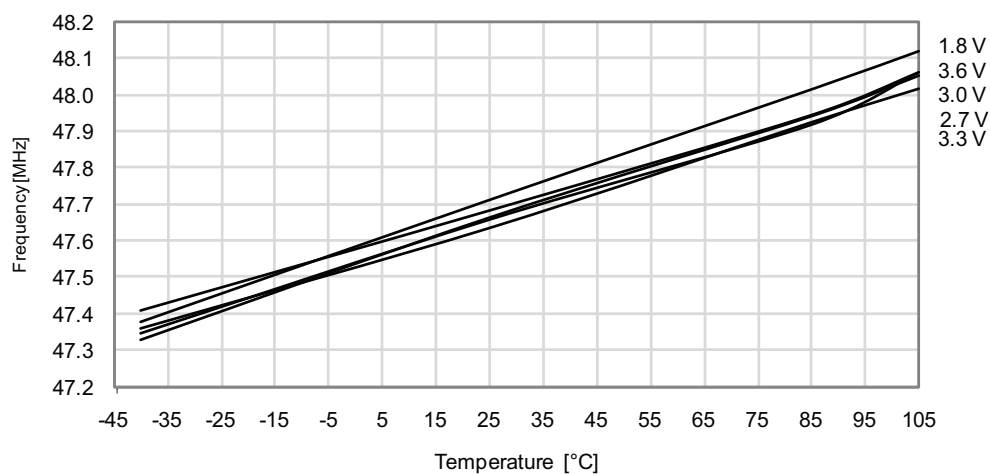


Figure 33-209. 48MHz Internal Oscillator Frequency vs. Temperature
DPLL enabled, from the 32.768kHz internal oscillator



33.3.9 Two-Wire Interface Characteristics

Figure 33-210. SDA Hold Time vs. Temperature

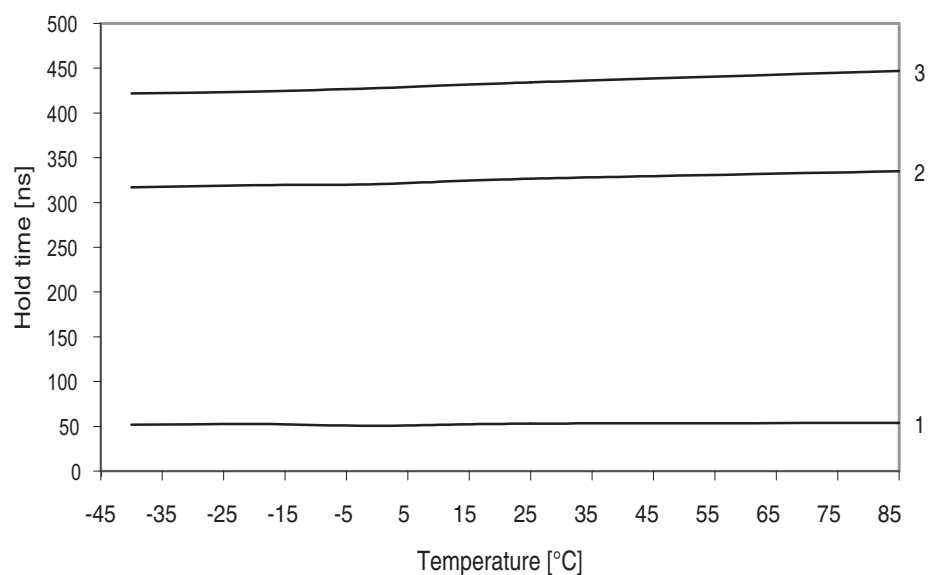


Figure 33-225. Idle Mode Supply Current vs. V_{CC}
 $f_{SYS} = 32\text{MHz}$ internal oscillator prescaled to 8MHz

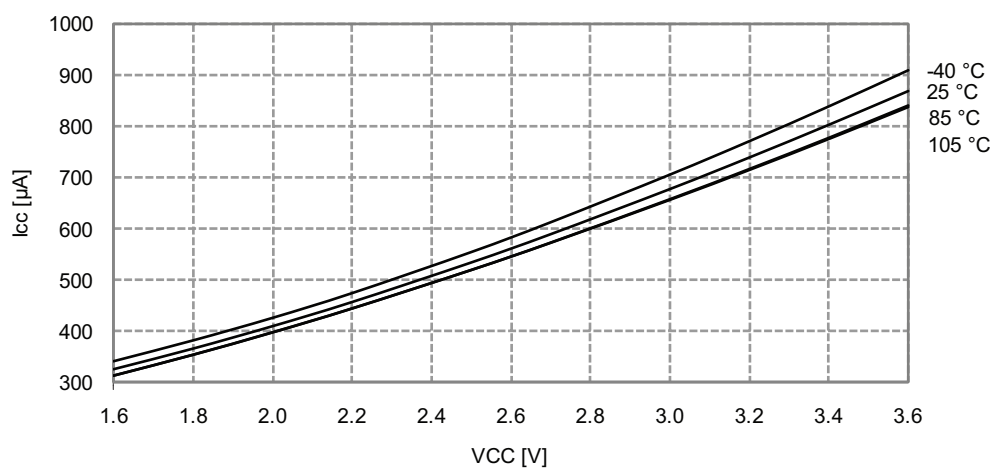
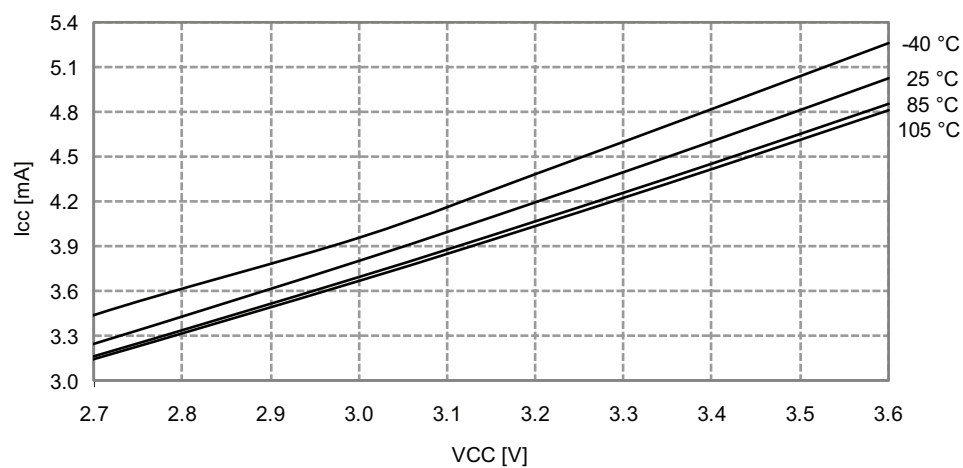


Figure 33-226. Idle Mode Current vs. V_{CC}
 $f_{SYS} = 32\text{MHz}$ internal oscillator



33.4.2.2 Output Voltage vs. Sink/Source Current

Figure 33-233. I/O Pin Output Voltage vs. Source Current
 $V_{CC} = 1.8V$

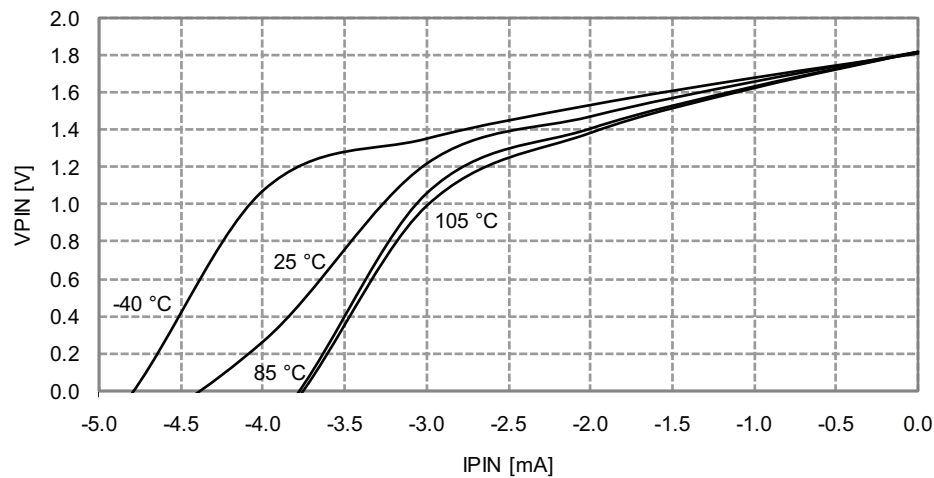


Figure 33-234. I/O Pin Output Voltage vs. Source Current
 $V_{CC} = 3.0V$

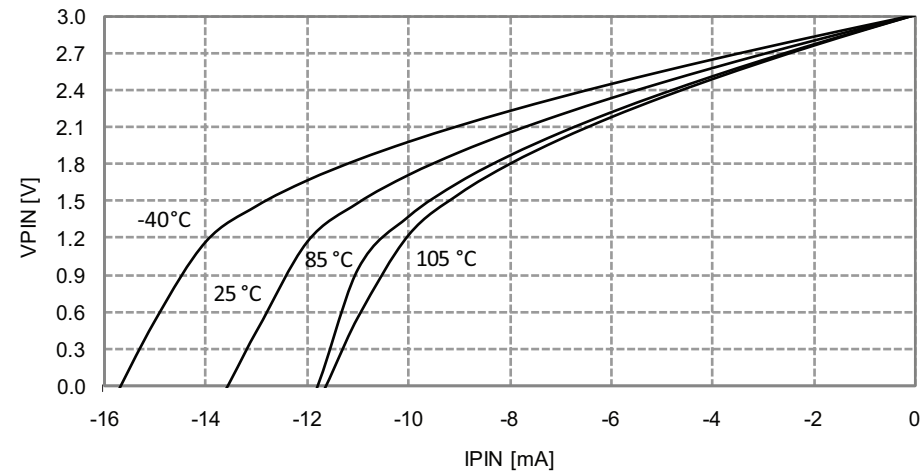
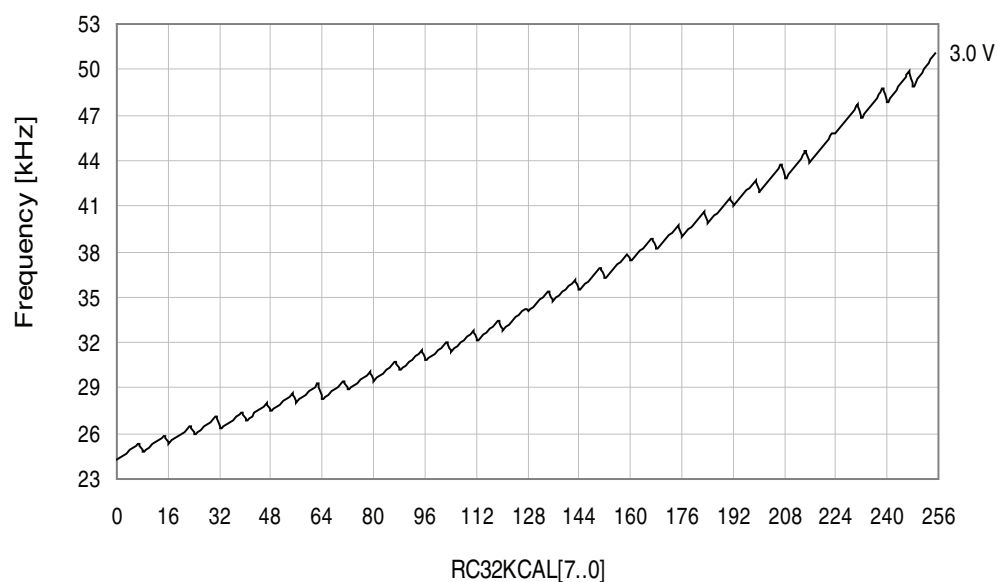


Figure 33-407. 32.768kHz Internal Oscillator Frequency vs. Calibration Value

$V_{CC} = 3.0V$, $T = 25^{\circ}C$



33.6.8.3 2MHz Internal Oscillator

Figure 33-408. 2MHz Internal Oscillator Frequency vs. Temperature

DPLL disabled

