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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA
Number of I/O	64
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	256K x 8
RAM Size	608K x 8
Voltage - Supply (Vcc/Vdd)	1.2V, 3.3V, 5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-eLQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc58ee80e7qmhay

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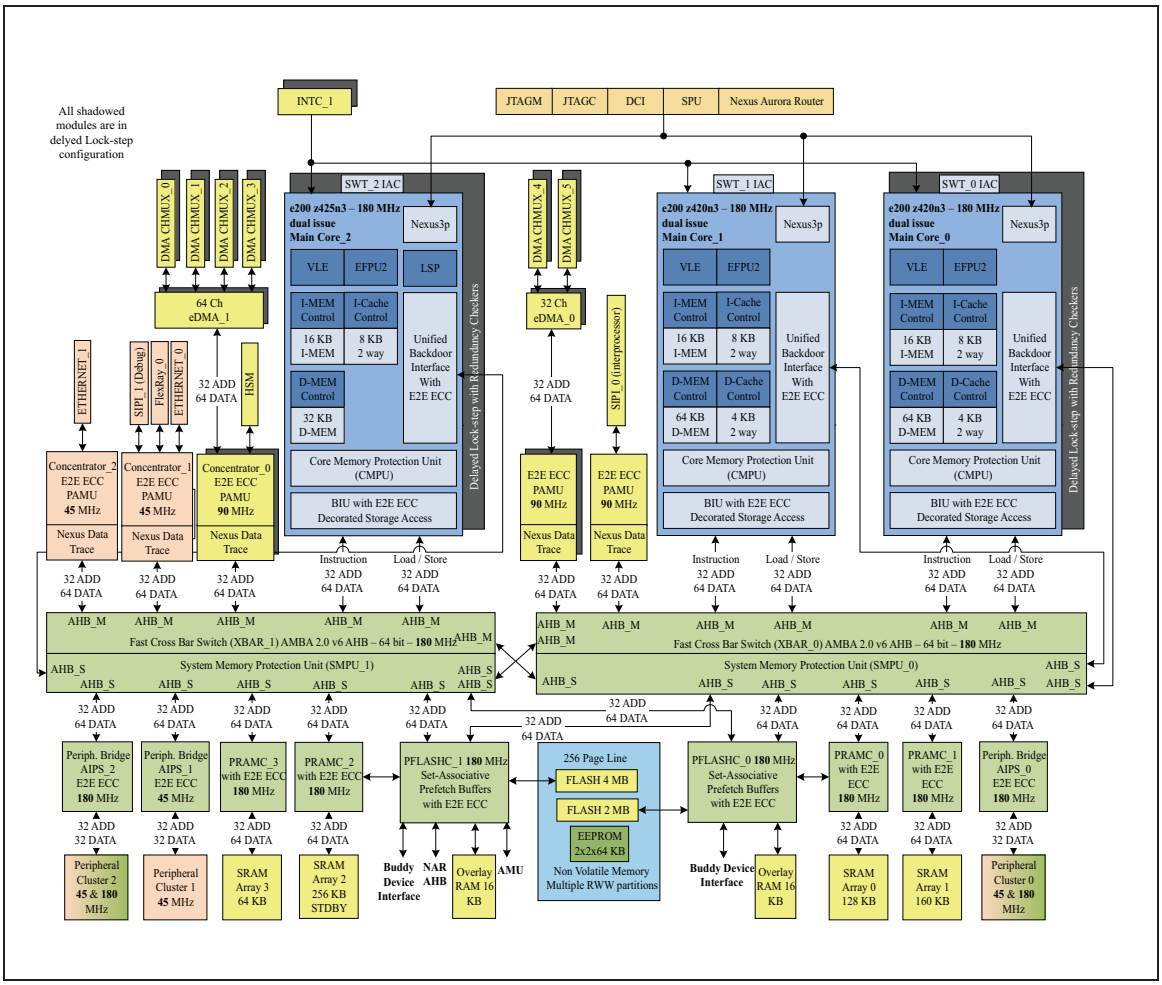
Figure 1. Block diagram



1.5 Features

On-chip modules within SPC58xEx include the following features:

- main CPUs, dual issue, 32-bit CPU core complexes (e200z4), paired in lock-step.
  - Power Architecture embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), encoding a mix of 16-bit and 32-bit instructions, for code size footprint reduction
  - Single-precision floating point operations
  - Lightweight signal processing auxiliary processing unit (LSP APU) instruction support for digital signal processing (DSP) on Core_2
  - 16 KB Local instruction RAM and 64 KB local data RAM for Core_0 and Core_1, 16 KB Local instruction RAM and 32 KB local data RAM for Core_2
  - 8 KB I-Cache and 4 KB D-Cache for Core_0 and Core_1, 8kB I-Cache for Core_2
- 6582 KB on-chip Flash
  - Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
  - Supports read while read between the two code Flash partitions.
- 608 KB on-chip general-purpose SRAM (+ 160 KB data RAM included in the CPUs)
- Multi channel direct memory access controllers (eDMA paired in lock-step)
  - One eDMA with 64 channels
  - One eDMA with 32 channels
- One interrupt controller (INTC) in lock-step
- Dual phase-locked loops with stable clock domain for peripherals and FM modulation domain for computational shell
- Dual crossbar switch architecture for concurrent access to peripherals, Flash, or RAM from multiple bus masters with end-to-end ECC
- Hardware security module (HSM) to provide robust integrity checking of Flash memory
- System integration unit lite (SIUL)
- Boot assist Flash (BAF) supports factory programming using a serial bootload through the asynchronous CAN or LIN/UART.
- GTM343 - generic timer module
  - Intelligent complex timer module
  - 144 channels (40 input and 104 output)
  - 5 programmable fine grain multi-threaded cores
  - 61 KB of dedicated RAM
  - 24-bit wide channels
  - Hardware support for engine control, motor control and safety related applications
- Enhanced analog-to-digital converter system with
  - One supervisor 12-bit SAR analog converter
  - Four separate fast 12-bit SAR analog converters
  - Three separate 10-bit SAR analog converters, one with STDBY mode support (except in eLQFP176 package)
  - Six separate 16-bit Sigma-Delta analog converters
- Ten deserial serial peripheral interface (DSPI) modules

Figure 3. I/O input electrical characteristics

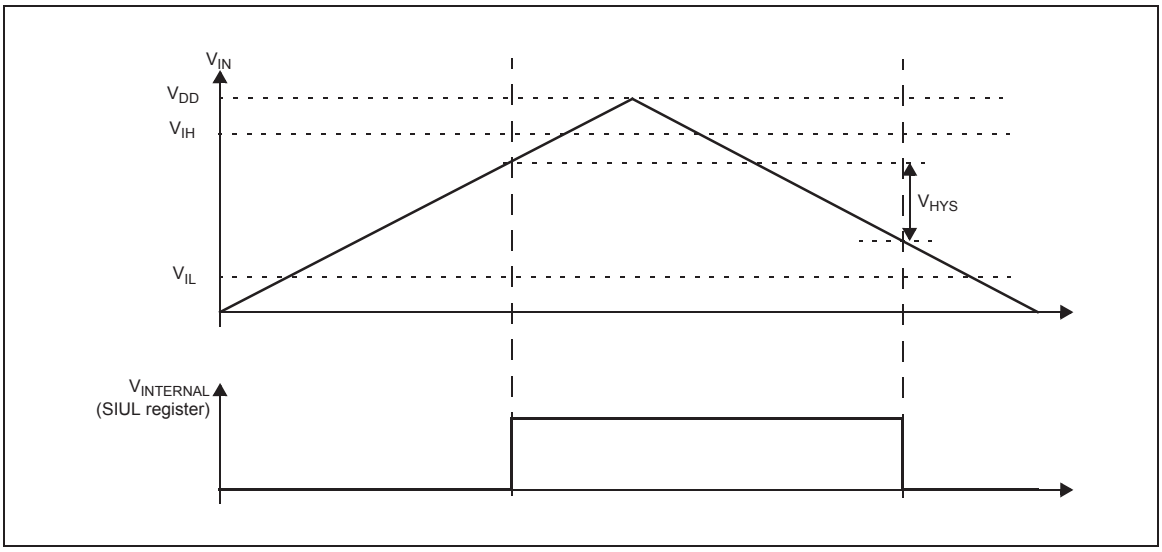


Table 11. I/O input electrical characteristics (1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
TTL								
V_{ihttl}	SR	P	Input high level TTL	—	2	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ilttl}	SR	P	Input low level TTL	—	–0.3	—	0.8	V
V_{hysttl}	CC	C	Input hysteresis TTL	—	0.3	—	—	V
AUTOMOTIVE								
V_{ihaut} (2)	SR	P	Input high level AUTO	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	3.8	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ilaut} (3)	SR	P	Input low level AUTO	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	–0.3	—	2.2	V
V_{hysaut} (4)	CC	C	Input hysteresis AUTO	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	0.5	—	—	V
CMOS								
V_{ihcmos}	SR	P	Input high level CMOS(1)	—	0.65 * V_{DD}	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ihcmos} BD	SR	T	Input high level CMOS	Buddy Device, hysteresis on	0.65 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
				Buddy Device, hysteresis off	0.60 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ilcmos}	SR	P	Input low level CMOS	—	–0.3	—	0.35 * V_{DD}	V

Table 12. I/O pull-up/pull-down electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{WPU}	CC	T	Weak pull-up current absolute value	V_{IN} = 1.1 V(1)	—	—	130	µA
		P		V_{IN} = 0.69 * $V_{DD\_HV\_IO}$(2)	15	—	—	
R_{WPU}	CC	D	Weak Pull-up resistance	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	33	—	93	KΩ
I_{WPD}	CC	T	Weak pull-down current absolute value	V_{IN} = 0.69 * $V_{DD\_HV\_IO}$(1)	—	—	130	µA
		P		V_{IN} = 0.9 V(2)	15	—	—	
R_{WPD}	CC	D	Weak Pull-down resistance	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	29	—	60	KΩ

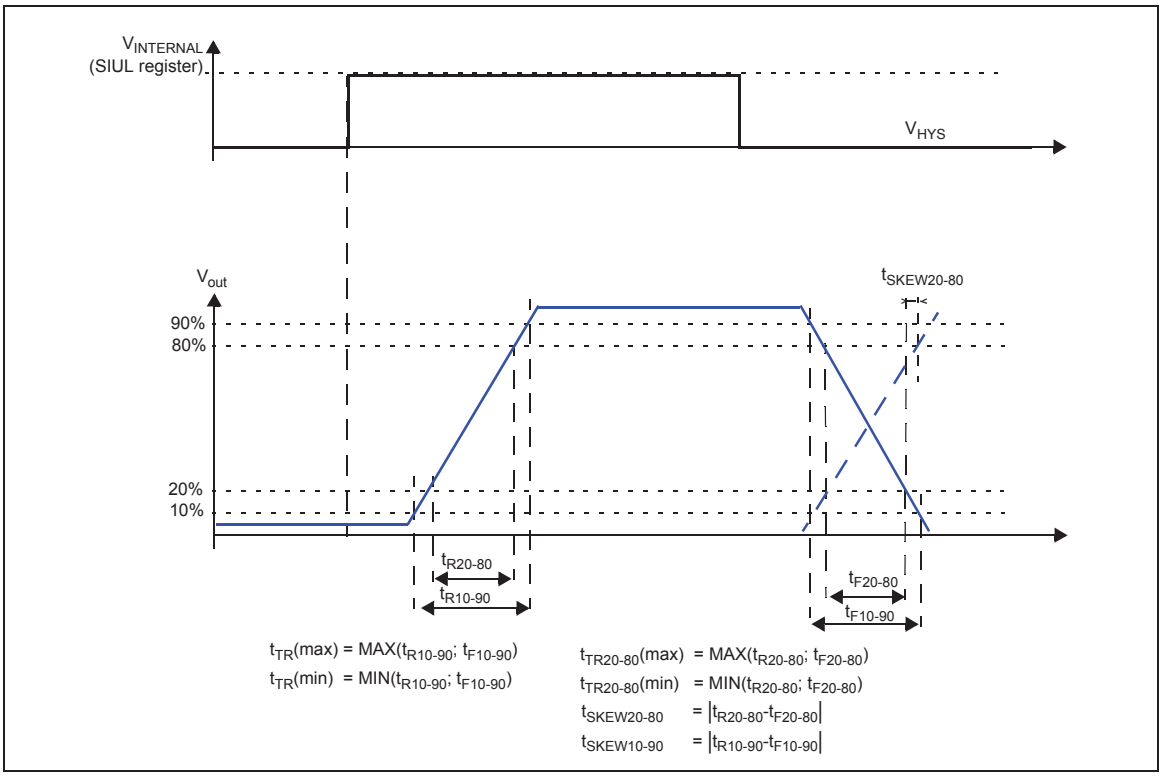
1. Maximum current when forcing a change in the pin level opposite to the pull configuration.
2. Minimum current when keeping the same pin level state as the pull configuration.

Note: When the device enters into standby mode, the LP pads have the input buffer switched-on. As a consequence, if the pad input voltage VIN is V_{SS}<V_{IN}<V_{DD_HV}, an additional consumption can be measured in the VDD_HV domain. The highest consumption can be seen around mid-range (VIN ~=VDD_HV/2), 2-3mA depending on process, voltage and temperature.
This situation may occur if the PAD is used as a ADC input channel, and V_{SS}<V_{IN}<V_{DD_HV}. The applications should ensure that LP pads are always set to VDD_HV or VSS, to avoid the extra consumption. Please refer to the device pin out IO definition excel file to identify the low-power pads which also have an ADC function.

3.8.2 I/O output DC characteristics

Figure 4 provides description of output DC electrical characteristics.

Figure 4. I/O output DC electrical characteristics definition



The following tables provide DC characteristics for bidirectional pads:

- *Table 13* provides output driver characteristics for I/O pads when in WEAK/SLOW configuration.
- *Table 14* provides output driver characteristics for I/O pads when in MEDIUM configuration.
- *Table 15* provides output driver characteristics for I/O pads when in STRONG/FAST configuration.
- *Table 16* provides output driver characteristics for I/O pads when in VERY STRONG/VERY FAST configuration.

Note: 10%/90% is the default condition for any parameter if not explicitly mentioned differently.

Table 13. WEAK/SLOW I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ol_W}	CC	D	Output low voltage for Weak type PADs	I_{ol} = 0.5 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	0.1*V_{DD}	V
V_{oh_W}	CC	D	Output high voltage for Weak type PADs	Ioh = 0.5 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	0.9*V_{DD}	—	—	V

3.11.4 Low power RC oscillator

Table 25. 1024 kHz internal RC oscillator electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
F_{sirc}	CC	T	Slow Internal RC oscillator frequency	—	—	1024	—	kHz
δf_{var_T}	CC	P	Frequency variation across temperature	–40 °C < T < 150 °C	–9	—	+9	%
δf_{var_V}	CC	P	Frequency variation across voltage	–40 °C < T < 150 °C	–5	—	+5	%
I_{sirc}	CC	T	Slow Internal RC oscillator current	T = 55 °C	—	—	6	µA
T_{sirc}	CC	T	Start up time, after switching ON the internal regulator.	—	—	—	12	µS

3.12 ADC system

3.12.1 ADC input description

Figure 8 shows the input equivalent circuit for SARn and SARB channels.

Figure 8. Input equivalent circuit (Fast SARn and SARB channels)

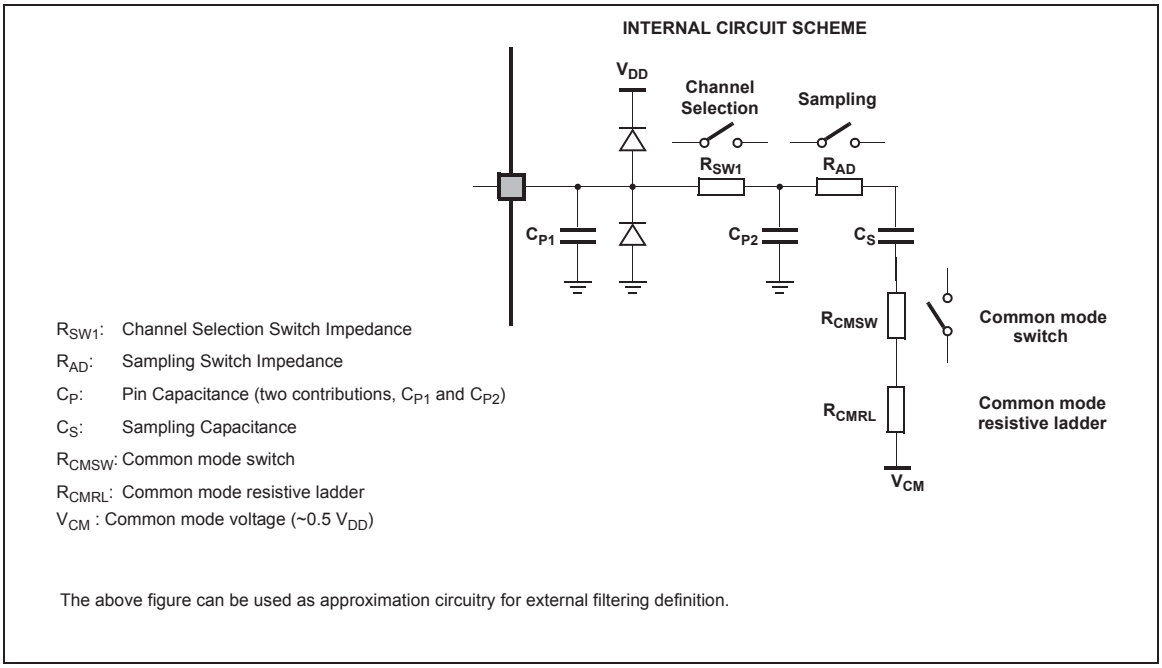


Table 26. ADC pin specification(1),(2)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
I_{LKG}	CC	—	Input leakage current, two ADC channels on input-only pin.	See IO chapter *Table 11: I/O input electrical characteristics*, parameter I_{LKG}			
$I_{INJ1,2}$	SR	—	Injection current on analog input preserving functionality at full or degraded performances.	See Operating Conditions chapter *Table 5: Operating conditions*, I_{INJ1} and I_{INJ2} parameters.			
C_{HV_ADC}	SR	D	$V_{DD\_HV\_ADV}$ external capacitance.	See Power Management chapter *Table 38: External components integration*, C_{ADC} parameter.			
C_{P1}	CC	D	Pad capacitance	See IO chapter *Table 11: I/O input electrical characteristics*, parameter C_{P1}			
C_{P2}	CC	D	Internal routing capacitance	SARB channels	—	2	pF
				SARn 10bit channels	—	0.5	
				SARn 12bit channels	—	1	
C_S	CC	D	SAR ADC sampling capacitance	SARn 12bit	—	5	pF
				SARn 10bit	—	2	

Table 27. SARn ADC electrical specification(1) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
ΔTUE_{12}	CC	D	TUE degradation due to $V_{DD\_HV\_ADR}$ offset with respect to $V_{DD\_HV\_ADV}$	$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	–1	1	LSB (12b)
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–2	2	
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–4	4	
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–6	6	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	–2.5	2.5	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–4	4	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–7	7	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–12	12	
TUE_{INJ2}	CC	T	TUE degradation addition, due to current injection in I_{INJ2} range.(9)	See *Table 5: Operating conditions*, I_{INJ2} parameter.	+8		LSB
DNL(8)	CC	P	Differential non-linearity	Standard frequency mode, $V_{DD\_HV\_ADV} > 4$ V $V_{DD\_HV\_ADR\_S} > 4$ V	–1	2	LSB (12b)
		T		High frequency mode, $V_{DD\_HV\_ADV} > 4$ V $V_{DD\_HV\_ADR\_S} > 4$ V	–1	2	

1. Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Minimum ADC sample times are dependent on adequate charge transfer from the external driving circuit to the internal sample capacitor. The time constant of the entire circuit must allow the sampling capacitor to charge within 1/2 LSB within the sampling window. Please refer to Figure 8 for models of the internal ADC circuit, and the values to use in external RC sizing and calculating the sampling window duration.

Table 29. SDn ADC electrical specification(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$SNR_{DIFF150}$(10)	CC	P	Signal to noise ratio in differential mode 150 ksps output rate(11)	$4.0 < V_{DD\_HV\_ADV} < 5.5$ $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV}$ GAIN = 1 $T_J < 150$ °C	80	—	—	dBFS
		C		$4.0 < V_{DD\_HV\_ADV} < 5.5$ $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV}$ GAIN = 2 $T_J < 150$ °C	77	—	—	
		C		$4.0 < V_{DD\_HV\_ADV} < 5.5$ $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV}$ GAIN = 4 $T_J < 150$ °C	74	—	—	
		C		$4.0 < V_{DD\_HV\_ADV} < 5.5$ $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV}$ GAIN = 8 $T_J < 150$ °C	71	—	—	
		D		$4.0 < V_{DD\_HV\_ADV} < 5.5$ $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV}$ GAIN = 16 $T_J < 150$ °C	68	—	—	

4. Startup times are valid for the maximum external loads CL defined in both the LFAST/HSD and MSC/DSPI transmitter electrical characteristic tables.
5. Bias startup time is defined as the time taken by the current reference block to reach the settling bias current after being enabled.
6. Total transmitter startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_TX} + 2 peripheral bridge clock periods.
7. Total transmitter startup time from sleep mode to normal mode is t_{SM2NM_TX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
8. Total receiver startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_RX} + 2 peripheral bridge clock periods.
9. Total receiver startup time from power down to sleep mode is t_{PD2SM_RX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
10. Absolute min = 0.15 V – (285 mV/2) = 0 V
11. Absolute max = 1.6 V + (285 mV/2) = 1.743 V
12. Value valid for LFAST mode. The LXRXOP[0] bit in the LFAST LVDS Control Register (LCR) must be set to one to ensure proper LFAST receive timing.
13. Total internal capacitance including receiver and termination, co-bonded GPIO pads, and package contributions. For bare die devices, subtract the package value given in *Figure 12*.

Table 32. LFAST transmitter electrical characteristics(1),(2),(3)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{DATA}	SR	D	Data rate	—	—	—	320	Mbps
V_{OS}	CC	P	Common mode voltage	—	1.08	—	1.32	V
$\|\Delta_{VOD}\|$	CC	P	Differential output voltage swing (terminated)(4),(5)	—	110	—	285	mV
t_{TR}	CC	T	Rise time from -|ΔVOD(min)| to +|ΔVOD(min)|. Fall time from +|ΔVOD(min)| to -|ΔVOD(min)|	—	0.26	—	1.25	ns
C_L	SR	D	External lumped differential load capacitance4	$V_{DD\_HV\_IO}$ = 4.5 V	—	—	6.0	pF
				$V_{DD\_HV\_IO}$ = 3.0 V	—	—	4.0	
I_{LVDS_TX}	CC	C	Transmitter DC current consumption	Enabled	—	—	3.6	mA
I_{PIN_TX}	CC	D	Transmitter DC current sourced through output pin	—	1.1		2.85	mA

1. This table is applicable to LFAST LVDS pads used in LFAST configuration (SIUL2_MSCR_IO_n.ODC=101).
2. The LFAST and High-Speed Debug LFAST pad electrical characteristics are based on worst case internal capacitance values shown in *Figure 12*.
3. All LFAST and High-Speed Debug LVDS pad electrical characteristics are valid from -40 °C to 165 °C.
4. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in *Figure 12*.
5. Valid for maximum external load C_L.

Table 47. Flash memory Life Specification

Symbol	Characteristics[1] [2]	Value				Unit
		Min	C	Typ	C	
N_{CER16K}	16 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER32K}	32 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER64K}	64 KB CODE Flash endurance	10	—	100	—	Kcycles
$N_{CER256K}$	256 KB CODE Flash endurance	1	—	100	—	Kcycles
	256 KB CODE Flash endurance[3]	10	—	100	—	Kcycles
N_{DER64K}	64 KB DATA EEPROM Flash endurance	250	—	—	—	Kcycles
t_{DR1k}	Minimum data retention Blocks with 0 - 1,000 P/E cycles	25	—	—	—	Years
t_{DR10k}	Minimum data retention Blocks with 1,001 - 10,000 P/E cycles	20	—	—	—	Years
t_{DR100k}	Minimum data retention Blocks with 10,001 - 100,000 P/E cycles	15	—	—	—	Years
t_{DR250k}	Minimum data retention Blocks with 100,001 - 250,000 P/E cycles	10	—	—	—	Years

1. Program and erase cycles supported across specified temperature specs.
2. It is recommended that the application enables the core chace memory.
3. 10K cycles on 4-256 KB blocks is not intended for production. Reduced reliability and degraded erase time are possible.

Table 49. Nexus debug port timing(1) (continued)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
12	t_{NTDIH}	CC	D	TDI data hold time	5	—	ns
13	t_{NTMSS}	CC	D	TMS data setup time	5	—	ns
14	t_{NTMSH}	CC	D	TMS data hold time	5	—	ns
15	—	CC	D	TDO propagation delay from falling edge of TCK(8)	—	16	ns
16	—	CC	D	TDO hold time with respect to TCK falling edge (minimum TDO propagation delay)	2.25	—	ns

1. Nexus timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 3.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet.
2. t_{CYC} is system clock period.
3. Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual peripheral frequency being used. To ensure proper operation TCK frequency should be set to the peripheral frequency divided by a number greater than or equal to that specified here.
4. This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.
5. This value is TDO propagation time 36 ns + 4 ns setup time to sampling edge.
6. This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.
7. This value is TDO propagation time 16n s + 4 ns setup time to sampling edge.
8. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.

Figure 22. Nexus output timing

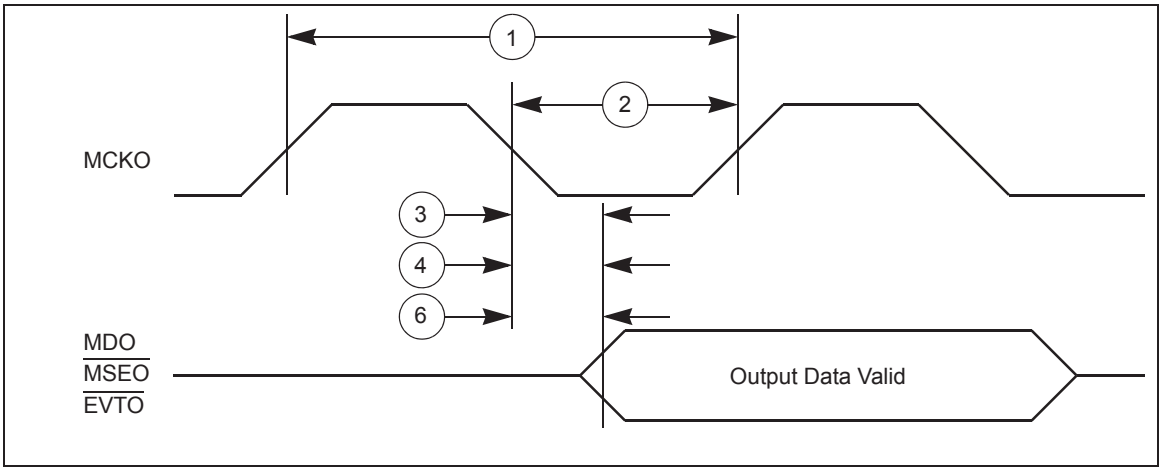


Figure 23. Nexus event trigger and test clock timings

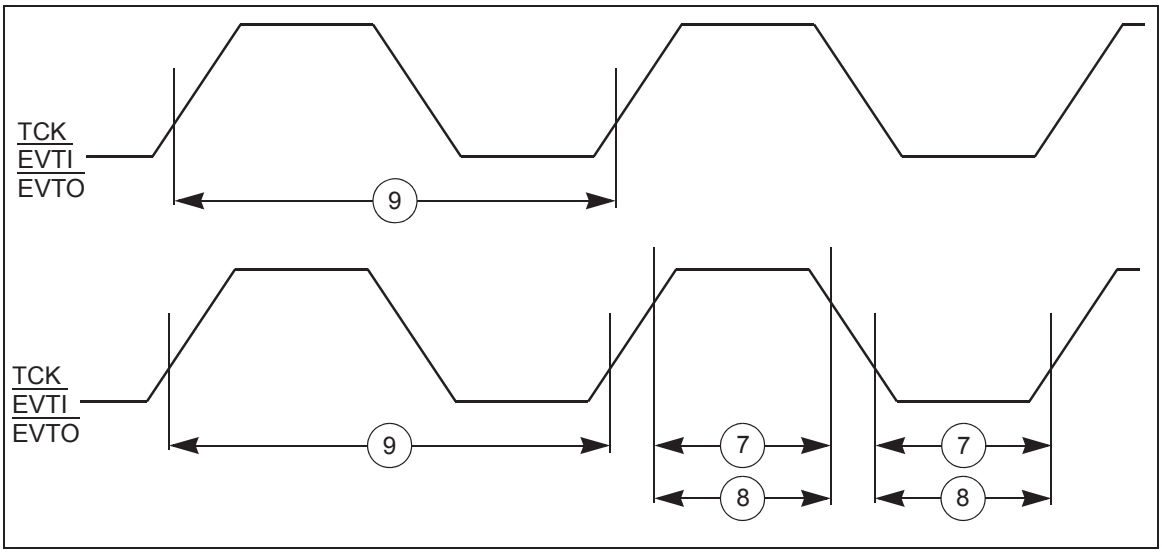


Figure 24. Nexus TDI, TMS, TDO timing

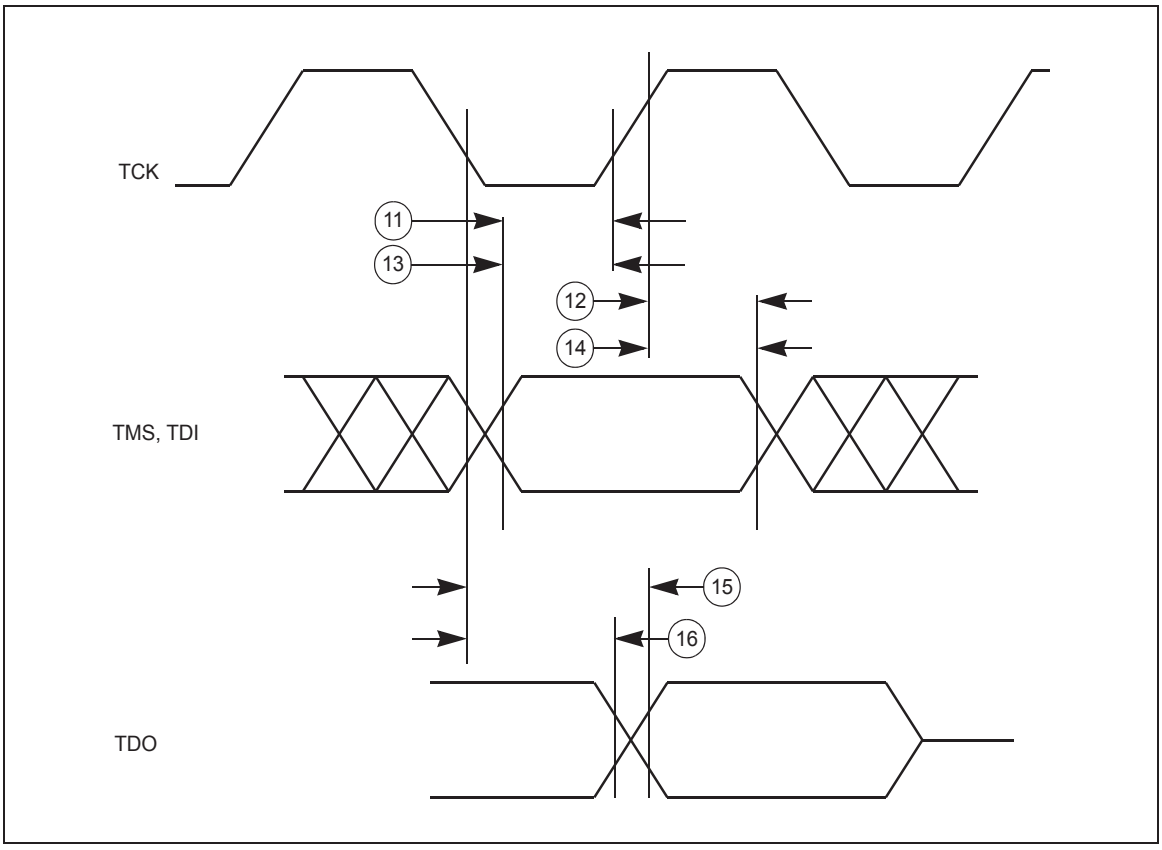
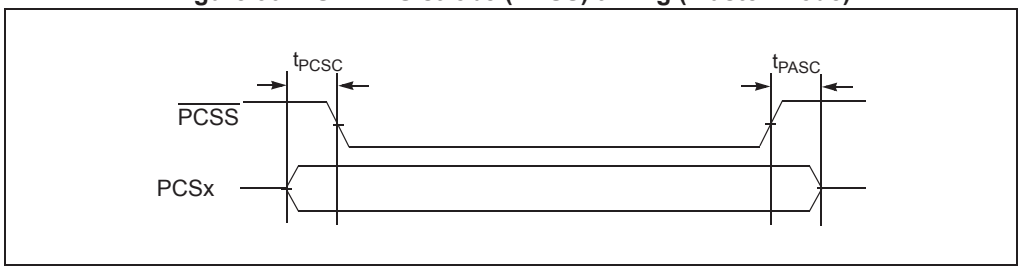


Figure 30. DSPI PCS strobe ($\overline{PCSS}$) timing (master mode)



3.18.2.1.2 DSPI CMOS master mode — modified timing

Table 55. DSPI CMOS master modified timing (full duplex and output only) — MTFE = 1, CPHA = 0 or 1(1)

#	Symbol		C	Characteristic	Condition		Value(2)		Unit
					Pad drive(3)	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	33.0	—	ns
					Strong	50 pF	80.0	—	
					Medium	50 pF	200.0	—	
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	ns
					Strong	50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	
					Medium	50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 29$	—	
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
					Medium	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
4	t_{SDC}	CC	D	SCK duty cycle(7)	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	
					Medium	0 pF	$^1/_2t_{SCK} - 5$	$^1/_2t_{SCK} + 5$	

Table 55. DSPI CMOS master modified timing (full duplex and output only) — MTFE = 1, CPHA = 0 or 1[1] (continued)

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
9	t_{SUO}	CC	D	SOUT data valid time from SCK CPHA = 0[10]	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0 + t_{SYS}[5]	ns
					Strong	50 pF	—	8.0 + t_{SYS}[5]	
					Medium	50 pF	—	16.0 + t_{SYS}[5]	
				SOUT data valid time from SCK CPHA = 1[10]	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	8.0	
					Medium	50 pF	—	16.0	
SOUT data hold time (after SCK edge)									
10	t_{HO}	CC	D	SOUT data hold time after SCK CPHA = 0[11]	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7 + t_{SYS}[5]	—	ns
					Strong	50 pF	–11.0 + t_{SYS}[5]	—	
					Medium	50 pF	–15.0 + t_{SYS}[5]	—	
				SOUT data hold time after SCK CPHA = 1[11]	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	
					Medium	50 pF	–15.0	—	

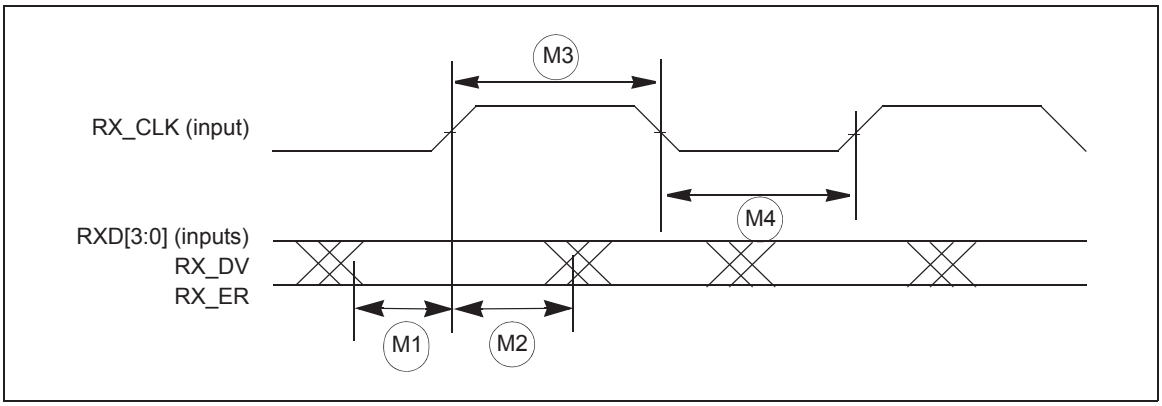
1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. All timing values for output signals in this table are measured to 50% of the output voltage.
3. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
4. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
5. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
6. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
7. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
8. PCSx and PCSS using same pad configuration.
9. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
10. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.

Table 56. DSPI LVDS master timing — full duplex — modified transfer format (MTFE = 1), CPHA = 0 or 1 (continued)

#	Symbol		C	Characteristic	Condition		Value(1)		Unit
					Pad drive	Load	Min	Max	
8	t_{HI}	CC	D	SIN Hold Time					
				SIN hold time from SCK CPHA = 0(7)	SCK drive strength				
					LVDS	0 pF differential	– 1 + (P(8) × t_{SYS}(4))	—	ns
				SIN hold time from SCK CPHA = 1(7)	SCK drive strength				
					LVDS	0 pF differential	–1	—	ns
9	t_{SUO}	CC	D	SOUT data valid time (after SCK edge)					
				SOUT data valid time from SCK CPHA = 0(9)	SOUT and SCK drive strength				
					LVDS	15 pF to 25 pF differential	—	7.0 + t_{SYS}(4)	ns
				SOUT data valid time from SCK CPHA = 1(9)	SOUT and SCK drive strength				
					LVDS	15 pF to 25 pF differential	—	7.0	ns
10	t_{HO}	CC	D	SOUT data hold time (after SCK edge)					
				SOUT data hold time after SCK CPHA = 0(9)	SOUT and SCK drive strength				
					LVDS	15 pF to 25 pF differential	–7.5 + t_{SYS}(4)	—	ns
				SOUT data hold time after SCK CPHA = 1(9)	SOUT and SCK drive strength				
					LVDS	15 pF to 25 pF differential	–7.5	—	ns

1. All timing values for output signals in this table are measured to 50% of the output voltage.
2. LVDS differential load considered is the capacitance on each terminal of the differential pair, as shown in *Figure 12*.
3. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
4. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
5. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
6. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
7. Input timing assumes an input slew rate of 1 ns (10% – 90%) and LVDS differential voltage = ±100 mV.
8. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.

Figure 39. MII receive signal timing diagram



3.18.3.2 MII transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the *Microcontroller Reference Manual's* Ethernet chapter for details of this option and how to enable it.

Table 61. MII transmit signal timing(1)

Symbol		C	Characteristic	Value(2)		Unit
				Min	Max	
M5	CC	D	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
M6	CC	D	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
M7	CC	D	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	CC	D	TX_CLK pulse width low	35%	65%	TX_CLK period

1. All timing specifications are referenced from TX_CLK = 1.4 V to the valid output levels, 0.8 V and 2.0 V.
2. Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value

Table 82. Document revision history (continued)

Date	Revision	Changes
03-April-2017	2	*Table 28: ADC-Comparator electrical specification*: – Classification for parameter "$I_{ADCREFH}$" changed from "C" to "T" – Removed table footnote "Values are subject to change (possibly improved to ±2 LSB) after characterization" – For parameter f_{ADCK} , replaced the min value "7.5" with ">13.33" *Table 26: ADC pin specification,*: For I_{LKG}, changed condition "C" to "—". *Table 29: SDn ADC electrical specification*: – Added footnote "When using a GAIN ... resolution of 15 bits" to parameter "RESOLUTION". – Added footnote "Conversion offset ... offset error" to parameter V_{OFFSET}. – Removed footnote "SNR value guaranteed ... frequency range" from parameters- $SNR_{DIFF150}$ and $SNR_{DIFF333}$. – In V_{cmrr}, changed "SR" to "CC" and "D" to "T" – Changed min value from "1.5" to "—" in parameter "I_{ADV_D}" – Changed min value from "3" to "—" in parameter "ΣI_{ADR_D}". – Added footnote "Consumption is given ... set-up" to parameter "ΣI_{ADR_D}" – Removed footnote "Sampling is .... $f_{ADCD\_M}/2$" – Updated footnote "S/D ADC is ...12 dB" – Added table footnote "This parameter ...3 dB less" to parameters - $SNR_{DIFF150}$, $SNR_{DIFF333}$, and SNR_{SE150} – Replaced the max value of ΣI_{ADR_D} of "16" with "80". *Figure 8: Input equivalent circuit (Fast SARn and SARB channels)*: Updated the figure. *Table 30: Temperature sensor electrical characteristics*: For "temperature monitoring range", classification removed (was C) *Table 35: LFAST PLL electrical characteristics*: – Min and Max value of parameter "ERR_{REF}" updated from "TBD" to "-1" and "+1" respectively – Max value of parameter "PN" updated from "TBD" to "-58" – Frequency of parameter "ΔPER_{REF}" updated from "10MHz" to "20MHz". – Max value of parameter "ΔPER_{REF}" for condition "Single period" updated from "TBD" to "350" – Min and Max value of parameter "ΔPER_{REF}" for condition "Long period" updated from "TBD" to "-500" and "+500" respectively. *Table 36: Aurora LVDS electrical characteristics,*: – For parameter $\lvert\Delta V_{I\_L}\rvert$, changed classification to "T" – For parameter $\lvert\Delta V_{OD\_LVDS}\rvert$, changed the classification to "T".