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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA
Number of I/O	64
Program Memory Size	6MB (6M x 8)
Program Memory Type	FLASH
EEPROM Size	256K x 8
RAM Size	608K x 8
Voltage - Supply (Vcc/Vdd)	1.2V, 3.3V, 5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-eLQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc58ee84e7qmsar

Table 1. Device summary

Package	Part number			
	4 MB		6 MB	
	Dual core	Triple core	Dual core	Triple core
eLQFP176	SPC58EE80E7	SPC58NE80E7	SPC58EE84E7	SPC58NE84E7
FPBGA292	SPC58EE80C3	SPC58NE80C3	SPC58EE84C3	SPC58NE84C3
KGD	—	—	—	SPC58NE84H0

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Table 2. SPC58xEx feature summary

Feature	Description
Other	
MPU	Yes
Security (HSM Module)	up to 1
Semaphores	Yes
CRC Channels	2 x 4
Software Watchdog Timer (SWT)	4
Core Nexus Class	3+
Event Processor	4 x SCU
	4 x PMC
Run control Module	Yes
System SRAM	608 KB (including 256 KB of standby RAM(1))
User Flash memory	up to 6144 KB code / 256 KB data
Flash fetch accelerator	2 x 2 x4 x 256-bit
Security Flash memory	up to 144 KB code / 32 KB data
Flash Overlay RAM	2 x 16 KB
Calibration Interface	64-bit IPS Slave
DMA channels	96
DMA Nexus Class	3
LINFlexD	18
M_CAN supporting CAN-FD according to ISO 11898-1 2015 (instances supporting also TTCAN)	8 (1)
DSPI	10
Microsecond channel downlink	2
SENT bus	15
I2C	1
PSI5 bus	2
FlexRay	1 x Dual channel
Ethernet	2
SIPI / LFAST Interprocessor bus	High Speed
System Timers	8 PIT channels
	4 AUTOSAR® (STM)
	RTC/API
GTM Timer	40 Input Channels, 104 Output Channels
GTM RAM	61 KB

3 Electrical characteristics

3.1 Introduction

The present document contains the target Electrical Specification for the 40 nm family 32-bit MCU SPC58xEx products.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” (Controller Characteristics) is included in the “Symbol” column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” (System Requirement) is included in the “Symbol” column.

The electrical parameters shown in this document are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 3* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 3. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device. NOTE: Parameters specified at junction temperature T_J = 165 °C are tested at T_J = 150 °C in production. Evaluation at higher temperature is performed during Design and Validation phases.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design validation on a small sample size from typical devices.
D	Those parameters are derived mainly from simulations.

Table 5. Operating conditions (continued)

Symbol		C	Parameter	Conditions	Value[1]			Unit
					Min	Typ	Max	
$V_{SS_HV_ADR_D}$-$V_{SS_HV_ADV}$	SR	D	$V_{SS_HV_ADR_D}$ differential voltage	—	–25	—	25	mV
$V_{DD_HV_ADR_S}$	SR	P	SAR ADC reference voltage	—	3.0	—	5.5	V
$V_{DD_HV_ADR_S}$-$V_{DD_HV_ADV}$	SR	D	SAR ADC reference differential voltage	—	$V_{DD_HV_ADV}$ -10%	—	25	mV
$V_{SS_HV_ADR_S}$	SR	P	SAR ADC ground reference voltage	—	$V_{SS_HV_ADV}$			V
$V_{SS_HV_ADR_S}$-$V_{SS_HV_ADV}$	SR	D	$V_{SS_HV_ADR_S}$ differential voltage	—	–25	—	25	mV
V_{RAMP_LV}	SR	D	Slew rate on core power supply pins	V_{DD_LV} $V_{DD_LV_BD}$	—	—	20	V/ms
V_{RAMP_HV}	SR	D	Slew rate on HV power supply	—	—	—	100	V/ms
V_{IN}	SR	P	I/O input voltage range	—	0	—	5.5	V
I_{INJ1}	SR	T	DC Injection current (per pin) without performance degradation[8] [9] [10]	Digital pins and analog pins	–3.0	—	3.0	mA
I_{INJ2}	SR	D	Dynamic Injection current (per pin) with performance degradation[10] [11]	Digital pins and analog pins	–10	—	10	mA

1. The ranges in this table are design targets and actual data may vary in the given range.
2. The maximum number of PRAM wait states has to be configured according to the system clock frequency. Refer to *Table 6*.
3. Core voltage as measured on device pin to guarantee published silicon performance.
4. In the range [1.14-1.08]V, the device functionality and specifications are granted and the device is expected to receive a flag by the internal LVD100 monitors to warn that the regulator (internal or external), providing the V_{DD_LV} supply, exited the expected operating conditions. If the internal LVD100 monitors are disabled by the application, then an external voltage monitor with minimum threshold of V_{DD_LV}(min) = 1.08 V measured at the device pad, has to be implemented. Please refer to *Section 3.16.3: Voltage monitors* for the list of available internal monitors and to the Reference Manual for the configurability of the monitors.

5. Core voltage can exceed 1.26 V with the limitations provided in *Section 3.2: Absolute maximum ratings*, provided that HVD134_C monitor reset is disabled.
6. 1.260 V - 1.290 V range allowed periodically for supply with sinusoidal shape and average supply value below or equal to 1.236 V at the given temperature profile.
7. S/D ADC is functional in the range 3.0 V < $V_{DD_HV_ADV}$ < 4.0 V and 3.0 V < $V_{DD_HV_ADR_D}$ < 4.0 V, but precision of conversion is not guaranteed.
8. Full device lifetime. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See *Section 3.2: Absolute maximum ratings* for maximum input current for reliability requirements.
9. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pins is above the supply rail, current will be injected through the clamp diode to the supply rails. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
10. The limits for the sum of all normal and injected currents on all pads within the same supply segment can be found in *Section 3.8.3: I/O pad current specifications*.
11. Positive and negative Dynamic current injection pulses are allowed up to this limit, with different specifications for I/O, ADC accuracy and analog input. See the dedicated chapters for the different specification limits. See the Absolute Maximum Ratings table for maximum input current for reliability requirements. Refer to the following pulses definitions: Pulse1 (ISO 7637-2:2011), Pulse 2a(ISO 7637-2:2011 5.6.2), Pulse 3a (ISO 7637-2:2011 5.6.3), Pulse 3b (ISO 7637-2:2011 5.6.3).

Table 6. PRAM wait states configuration

PRAMC WS	Clock Frequency (MHz)
1	≤ 180
0	≤ 120

3.3.1 Power domains and power up/down sequencing

The following table shows the constraints and relationships for the different power domains. Supply1 (on rows) can exceed Supply2 (on columns), only if the cell at the given row and column is reporting ‘ok’. This limitation is valid during power-up and power-down phases, as well as during normal device operation.

Table 17. I/O consumption(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{RMS_S}	CC	D	RMS I/O current for STRONG configuration	C_L = 25 pF, 50 MHz, V_{DD} = 5.0 V ± 10%	—	—	21	mA
				C_L = 50 pF, 25 MHz, V_{DD} = 5.0 V ± 10%	—	—	21	
				C_L = 25 pF, 25 MHz, V_{DD} = 3.3 V ± 10%	—	—	10	
				C_L = 25 pF, 12.5 MHz, V_{DD} = 3.3 V ± 10%	—	—	10	
I_{RMS_V}	CC	D	RMS I/O current for VERY STRONG configuration	C_L = 25 pF, 50 MHz, V_{DD} = 5.0 V ± 10%	—	—	23	mA
				C_L = 50 pF, 25 MHz, V_{DD} = 5.0 V ± 10%	—	—	23	
				C_L = 25 pF, 50 MHz, V_{DD} = 3.3 V ± 10%	—	—	16	
				C_L = 25 pF, 25 MHz, V_{DD} = 3.3 V ± 10%	—	—	16	
Dynamic consumption(3)								
I_{DYN_SEG}	SR	D	Sum of all the dynamic and DC I/O current within a supply segment	V_{DD} = 5.0 V ± 10%	—	—	195	mA
				V_{DD} = 3.3 V ± 10%	—	—	150	
I_{DYN_W}	CC	D	Dynamic I/O current for WEAK configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	16.7	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	16.8	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	12.9	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	12.9	
I_{DYN_M}	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	18.2	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	18.4	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	14.3	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	16.4	

Table 26. ADC pin specification(1),(2) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
R_{SWn}	CC	D	Analog switches resistance	SARB channels	0	1.8	kΩ
				SARn 10bit channels	0	0.8	
				SARn 12bit channels	0	1.8	
R_{AD}	CC	D	ADC input analog switches resistance	SARn 12bit	—	0.8	kΩ
				SARn 10bit	—	3.2	
R_{CMSW}	CC	D	Common mode switch resistance	sum of the two resistances	—	9	kΩ
R_{CMRL}	CC	D	Common mode resistive ladder				kΩ
R_{SAFEPD}(3)	CC	D	Discharge resistance for ADC input-only pins (strong pull-down for safety)	$V_{DD_HV_IO}$ = 5.0 V ± 10%	—	300	Ω
				$V_{DD_HV_IO}$ = 3.3 V ± 10%	—	500	Ω
A_{BGAP}	CC	D	ADC digital bandgap accuracy		-1.5	+1.5	%

1. Specifications in this table apply to both packaged parts and Known Good Die (KGD) parts, except where noted.
2. All specifications in this table valid for the full input voltage range for the analog inputs.
3. It enables discharge of up to 100 nF from 5 V every 300 ms. Please refer to the device pin out IO definition excel file, for the pads supporting it.

3.12.2 SAR ADC 12 bit electrical specification

The SARn ADCs are 12-bit Successive Approximation Register analog-to-digital converters with full capacitive DAC. The SARn architecture allows input channel multiplexing.

Table 27. SARn ADC electrical specification(1)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{ADCK}	SR	P	Clock frequency	Standard frequency mode	7.5	13.33	MHz
		T		High frequency mode	>13.33	16.0	
$t_{ADCINIT}$	SR	—	ADC initialization time	—	1.5	—	µs
$t_{ADCBIASINIT}$	SR	—	ADC BIAS initialization time	—	5	—	µs
$t_{ADCPRECH}$	SR	T	ADC decharge time	Fast SAR	$1/f_{ADCK}$	—	µs
				Slow SAR (SARDAC_B)	$2/f_{ADCK}$	—	
ΔV_{PRECH}	SR	D	Decharge voltage precision	T_J < 150 °C	0	0.25	V
				T_J < 165 °C	0	0.3	
ΔV_{INTREF}	CC	P	Internal reference voltage precision	Applies to all internal reference points ($V_{SS_HV_ADR}$, 1/3 * $V_{DD_HV_ADR}$, 2/3 * $V_{DD_HV_ADR}$, $V_{DD_HV_ADR}$)	–0.20	0.20	V

3. $I_{ADCREFH}$ and $I_{ADCREFL}$ are independent from ADC clock frequency. It depends on conversion rate: consumption is driven by the transfer of charge between internal capacitances during the conversion.
4. Current parameter values are for a single ADC.
5. All channels of all SAR-ADC12bit and SAR-ADC10bit are impacted with same degradation, independently from the ADC and the channel subject to current injection.
6. TUE and DNL are granted with injection current within the range defined in Table 26, for parameters classified as T and D.

3.12.4 S/D ADC electrical specification

The SDn ADCs are Sigma Delta 16-bit analog-to-digital converters with 333Ksps maximum output rate.

Table 29. SDn ADC electrical specification(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IN_PK2PK}(2)	SR	D	Input range peak to peak $V_{IN_PK2PK} = V_{INP}$(3) $- V_{INM}$(4)	Single ended $V_{INM} = V_{SS_HV_ADR_D}$	$V_{DD_HV_ADR_D}$/GAIN			V
		D		Single ended $V_{INM} = 0.5*V_{DD_HV_ADR_D}$ GAIN = 1	±0.5*$V_{DD_HV_ADR_D}$			
		D		Single ended $V_{INM} = 0.5*V_{DD_HV_ADR_D}$ GAIN = 2,4,8,16	±$V_{DD_HV_ADR_D}$/GAIN			
		D		Differential, $0 < V_{IN} < V_{DD_HV_IO_MAIN}$	±$V_{DD_HV_ADR_D}$/GAIN			
f_{ADCD_M}	SR	P	S/D modulator input Clock 3	T_J < 150 °C	4	14.4	16	MHz
f_{IN}	SR	P	Input signal frequency	—	0.01	—	75(5)	Khz
f_{ADCD_S}	SR	D	Output conversion rate	T_J < 150 °C	—	—	333	ksps
—	CC	D	Oversampling ratio	Internal modulator	24	—	256	—
				External modulator	—	—	256	—
RESOLUTION	CC	D	S/D register resolution(6)	2's complement notation	16			bit
GAIN	SR	D	ADC gain	Defined via ADC_SD[PGA] register. Only integer powers of 2 are valid gain values.	1	—	16	—

4. Startup times are valid for the maximum external loads CL defined in both the LFAST/HSD and MSC/DSPI transmitter electrical characteristic tables.
5. Bias startup time is defined as the time taken by the current reference block to reach the settling bias current after being enabled.
6. Total transmitter startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_TX} + 2 peripheral bridge clock periods.
7. Total transmitter startup time from sleep mode to normal mode is t_{SM2NM_TX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
8. Total receiver startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_RX} + 2 peripheral bridge clock periods.
9. Total receiver startup time from power down to sleep mode is t_{PD2SM_RX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
10. Absolute min = 0.15 V – (285 mV/2) = 0 V
11. Absolute max = 1.6 V + (285 mV/2) = 1.743 V
12. Value valid for LFAST mode. The LXRXOP[0] bit in the LFAST LVDS Control Register (LCR) must be set to one to ensure proper LFAST receive timing.
13. Total internal capacitance including receiver and termination, co-bonded GPIO pads, and package contributions. For bare die devices, subtract the package value given in *Figure 12*.

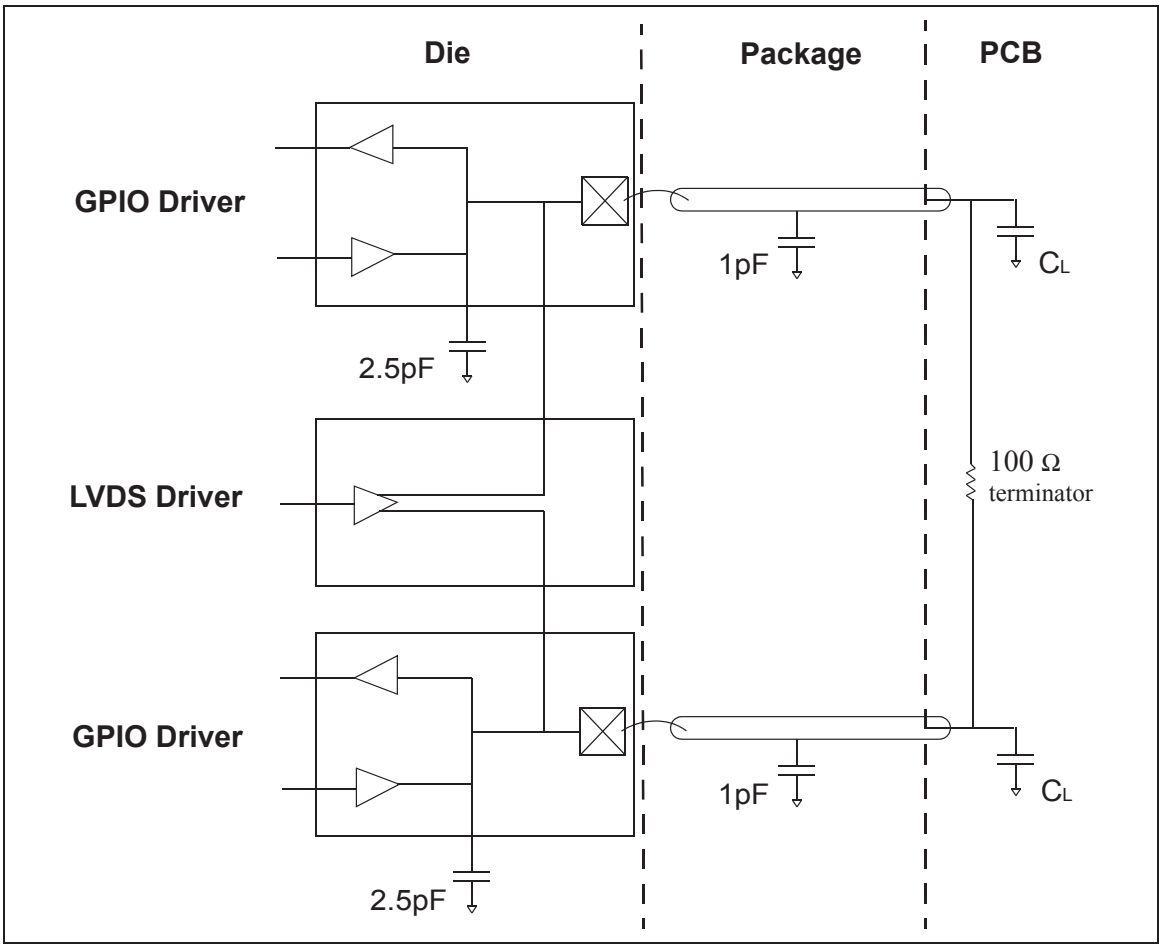
Table 32. LFAST transmitter electrical characteristics(1),(2),(3)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{DATA}	SR	D	Data rate	—	—	—	320	Mbps
V_{OS}	CC	P	Common mode voltage	—	1.08	—	1.32	V
$\|\Delta_{VOD}\|$	CC	P	Differential output voltage swing (terminated)(4),(5)	—	110	—	285	mV
t_{TR}	CC	T	Rise time from -|ΔVOD(min)| to +|ΔVOD(min)|. Fall time from +|ΔVOD(min)| to -|ΔVOD(min)|	—	0.26	—	1.25	ns
C_L	SR	D	External lumped differential load capacitance4	$V_{DD_HV_IO}$ = 4.5 V	—	—	6.0	pF
				$V_{DD_HV_IO}$ = 3.0 V	—	—	4.0	
I_{LVDS_TX}	CC	C	Transmitter DC current consumption	Enabled	—	—	3.6	mA
I_{PIN_TX}	CC	D	Transmitter DC current sourced through output pin	—	1.1		2.85	mA

1. This table is applicable to LFAST LVDS pads used in LFAST configuration (SIUL2_MSCR_IO_n.ODC=101).
2. The LFAST and High-Speed Debug LFAST pad electrical characteristics are based on worst case internal capacitance values shown in *Figure 12*.
3. All LFAST and High-Speed Debug LVDS pad electrical characteristics are valid from -40 °C to 165 °C.
4. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in *Figure 12*.
5. Valid for maximum external load C_L.

3. All MSC and DSPI LVDS pad electrical characteristics are valid from -40 °C to 165 °C.
4. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in *Figure 12*.
5. Valid for maximum external load C_L.
6. The transition time is measured from 10% to 90% of the voltage transition from -|ΔVOD|(min) to +|ΔVOD|(min).

Figure 12. LVDS pad external load diagram



3.14.3 LFAST PLL electrical characteristics

The following table contains the electrical characteristics for the LFAST PLL.

Table 35. LFAST PLL electrical characteristics(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{RF_REF}	SR	D	PLL reference clock frequency (CLKIN)	—	10(2)	—	30	MHz
ERR_{REF}	CC	D	PLL reference clock frequency error	—	-1	—	1	%

Table 38. External components integration (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
R_{LVn}	SR	D	Stability capacitor equivalent serial resistance	—	—	—	50	mΩ
C_{BV}	SR	D	Bulk capacitance for HV supply[2]	—	—	4.7	—	µF
C_{HVn}	SR	D	Decoupling capacitance for ballast and IOs[2]	on all $V_{DD_HV_IO}/V_{SS}$ and $V_{DD_HV_ADR}/V_{SS}$ pairs	—	100	—	nF
C_{FLA}	SR	D	Decoupling capacitance for flash supply[6]	—	—	10	—	nF
C_{ADC}	SR	D	ADC supply external capacitance[2]	$V_{DD_HV_ADV}/V_{SS_HV_ADV}$ pair.	—	2.2	—	µF
Internal Linear Regulator with External Ballast Mode								
Q_{EXT}	SR	D	Recommended external NPN transistors	NJD2873T4, BCP68				
V_Q	SR	D	External NPN transistor collector voltage	—	2.0	—	$V_{DD_HV_IO_MAIN}$	V
C_B	SR	D	Internal voltage regulator stability external capacitance on ballast base[5] [7]	—	—	2.2	—	µF
R_B	SR	D	Stability capacitor equivalent serial resistance	Total resistance including board track	—	—	50	mΩ
SMPS Regulator Mode								
Common Configuration[8]								
PMOS	SR	D	Recommended PMOS transistor for SMPS mode	PMPB100XPEA				
NMOS	SR	D	Recommended NMOS transistor for SMPS mode	PMPB55XNEA				
C_{S2}	SR	D	SMPS External capacitance on HV supply[2]	—	-50%	47[9]	+35	µF
Option A								
C_{S1_A}	SR	D	SMPS External capacitance on LV supply[2]	—	-50%	2x10	+35	µF
L_{S_A}	SR	D	SMPS External inductance	—	-30%	10	+30%	µH
Option B								
C_{S1_B}	SR	D	SMPS External capacitance on LV supply[10]	—	-35%	3x10	+35%	µF
L_{S_B}	SR	D	SMPS External inductance	—	-30%	4.7	+30%	µH

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_J = –40 / 165 °C, unless otherwise specified.
2. Recommended X7R or X5R ceramic –50% / +35% variation across process, temperature, voltage and after aging.
3. CE capacitance is required both in internal and external regulator mode.
4. For noise filtering, add a high frequency bypass capacitance of 10 nF.

5. For BGA and KGD applications it is recommended to implement at least 5 C_{LV} capacitances.
6. Recommended X7R capacitors. For noise filtering, add a high frequency bypass capacitance of 100 nF.
7. CB capacitance is required if only the external ballast is implemented.
8. The application has to implement one of the two recommended combinations of external components for the SMPS regulator:
   PMOS, NMOS and CS2 (common), plus CS1_A and LS_A (option A), or
   PMOS, NMOS and CS2 (common), plus CS1_B and LS_B (option B).
9. The value of the capacitance on the HV supply reported in the datasheet is a general recommendation. The application can select a different number, based on the external regulator and emc requirements.
10. Recommended X7R or X5R ceramic –35% / +35% variation across process, temperature, voltage and after aging.

3.16.3 Voltage monitors

The monitors and their associated levels for the device are given in Table 44. Figure 17 illustrates the workings of voltage monitoring threshold.

Figure 17. Voltage monitor threshold definition

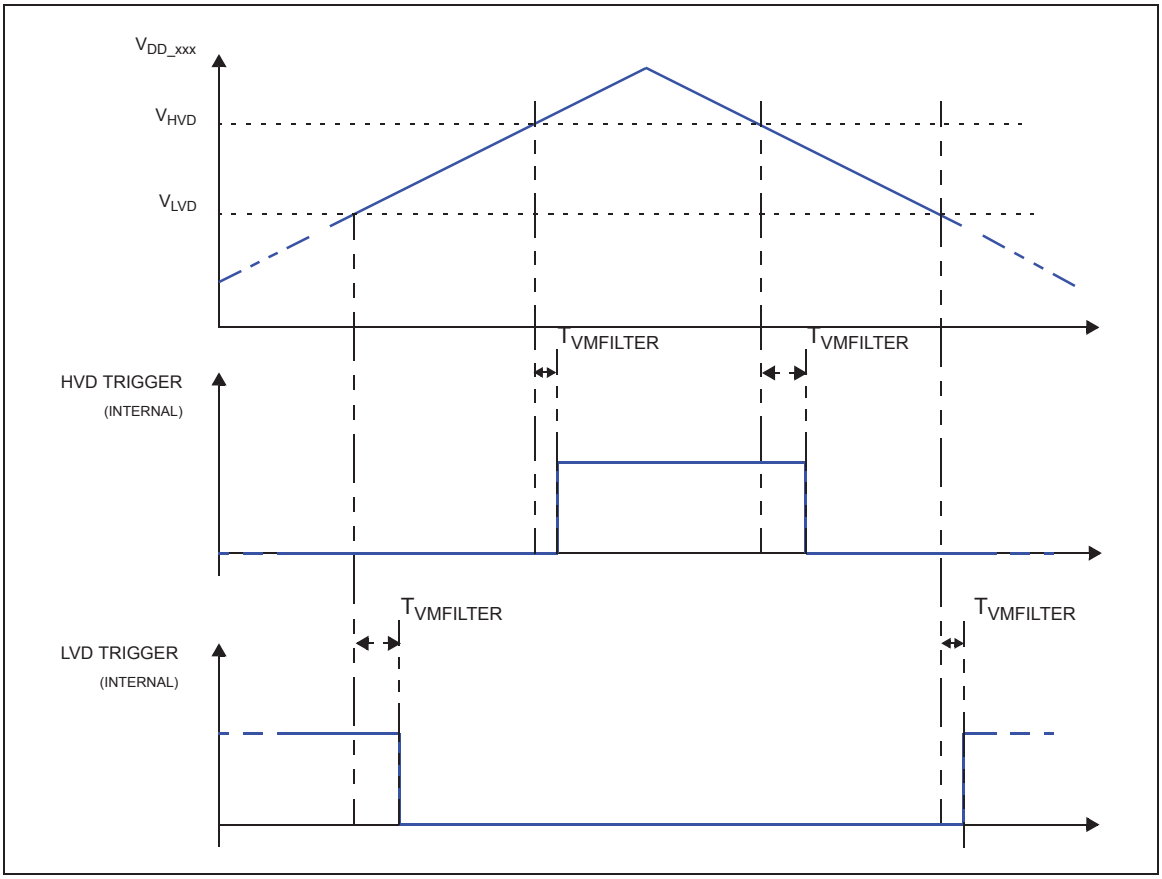


Table 44. Voltage monitor electrical characteristics

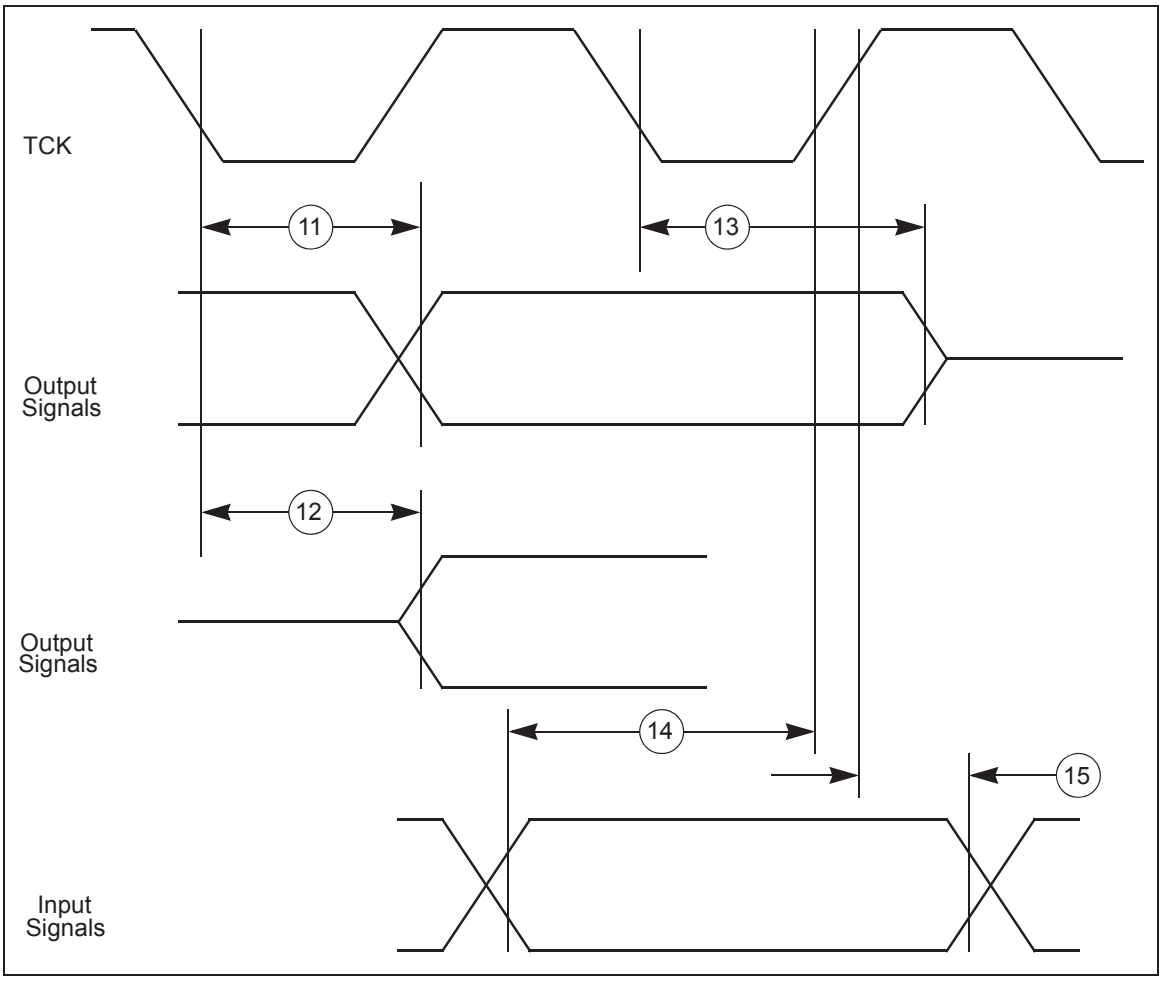
Symbol	C		Supply/Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
PowerOn Reset HV								
V_{POR200_C}	CC	P	$V_{DD_HV_IO_MAIN}$	—	1.80	2.18	2.40	V
Minimum Voltage Detectors HV								
V_{MVD270_C}	CC	P	$V_{DD_HV_IO_MAIN}$	—	2.71	2.76	2.80	V
V_{MVD270_F}	CC	P	$V_{DD_HV_FLA}$	—	2.71	2.76	2.80	V
V_{MVD270_SBY}	CC	P	$V_{DD_HV_IO_MAIN}$ (in Standby)	—	2.71	2.76	2.80	V
Low Voltage Detectors HV								
V_{LVD290_C}	CC	P	$V_{DD_HV_IO_MAIN}$	—	2.89	2.94	2.99	V

Table 47. Flash memory Life Specification

Symbol	Characteristics(1) (2)	Value				Unit
		Min	C	Typ	C	
N_{CER16K}	16 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER32K}	32 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER64K}	64 KB CODE Flash endurance	10	—	100	—	Kcycles
$N_{CER256K}$	256 KB CODE Flash endurance	1	—	100	—	Kcycles
	256 KB CODE Flash endurance(3)	10	—	100	—	Kcycles
N_{DER64K}	64 KB DATA EEPROM Flash endurance	250	—	—	—	Kcycles
t_{DR1k}	Minimum data retention Blocks with 0 - 1,000 P/E cycles	25	—	—	—	Years
t_{DR10k}	Minimum data retention Blocks with 1,001 - 10,000 P/E cycles	20	—	—	—	Years
t_{DR100k}	Minimum data retention Blocks with 10,001 - 100,000 P/E cycles	15	—	—	—	Years
t_{DR250k}	Minimum data retention Blocks with 100,001 - 250,000 P/E cycles	10	—	—	—	Years

1. Program and erase cycles supported across specified temperature specs.
2. It is recommended that the application enables the core chace memory.
3. 10K cycles on 4-256 KB blocks is not intended for production. Reduced reliability and degraded erase time are possible.

Figure 21. JTAG boundary scan timing



3.18.1.2 Nexus interface timing

Table 49. Nexus debug port timing(1)

#	Symbol		C		Characteristic	Value		Unit
						Min	Max	
7	t_{EVTIPW}	CC	D		$\overline{EVTI}$ pulse width	4	—	t_{CYC}(2)
8	t_{EVTOPW}	CC	D		$\overline{EVTO}$ pulse width	40	—	ns
9	t_{TCYC}	CC	D		TCK cycle time	2(3),(4)	—	t_{CYC}(2)
9	t_{TCYC}	CC	D		Absolute minimum TCK cycle time(5) (TDO sampled on posedge of TCK)	40(6)	—	ns
					Absolute minimum TCK cycle time(7) (TDO sampled on negedge of TCK)	20(6)	—	
11	t_{NTDIS}	CC	D		TDI data setup time	5	—	ns

Table 54. DSPI CMOS master classic timing (full duplex and output only) — MTFE = 0, CPHA = 0 or 1[1] (continued)

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	(N[4] × t_{SYS}[5]) – 16	—	ns
					Strong	50 pF	(N[4] × t_{SYS}[5]) – 16	—	
					Medium	50 pF	(N[4] × t_{SYS}[5]) – 16	—	
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	(N[4] × t_{SYS}[5]) – 29	—	
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	(M[6] × t_{SYS}[5]) – 35	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	(M[6] × t_{SYS}[5]) – 35	—	
					Medium	PCS = 0 pF SCK = 50 pF	(M[6] × t_{SYS}[5]) – 35	—	
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	(M[6] × t_{SYS}[5]) – 35	—	
4	t_{SDC}	CC	D	SCK duty cycle[7]	SCK drive strength				
					Very strong	0 pF	$^1/_2 t_{SCK} - 2$	$^1/_2 t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2 t_{SCK} - 2$	$^1/_2 t_{SCK} + 2$	
					Medium	0 pF	$^1/_2 t_{SCK} - 5$	$^1/_2 t_{SCK} + 5$	
PCS strobe timing									
5	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time[8]	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
6	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time[8]	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
SIN setup time									
7	t_{SUI}	CC	D	SIN setup time to SCK[9]	SCK drive strength				
					Very strong	25 pF	25.0	—	ns
					Strong	50 pF	31.0	—	
					Medium	50 pF	52.0	—	
SIN hold time									

mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

When board temperature is perfectly defined below the device, it is possible to use the thermal characterization parameter (Ψ_{JPB}) to determine the junction temperature by measuring the temperature at the bottom center of the package case (exposed pad) using the following equation:

Equation 5

$$T_J = T_B + (\Psi_{JPB} \times P_D)$$

where:

T_T = thermocouple temperature on bottom of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

Table 82. Document revision history (continued)

Date	Revision	Changes
03-April-2017	2	*Table 28: ADC-Comparator electrical specification*: – Classification for parameter "$I_{ADCREFH}$" changed from "C" to "T" – Removed table footnote "Values are subject to change (possibly improved to ±2 LSB) after characterization" – For parameter f_{ADCK} , replaced the min value "7.5" with ">13.33" *Table 26: ADC pin specification,*: For I_{LKG}, changed condition "C" to "—". *Table 29: SDn ADC electrical specification*: – Added footnote "When using a GAIN ... resolution of 15 bits" to parameter "RESOLUTION". – Added footnote "Conversion offset ... offset error" to parameter V_{OFFSET}. – Removed footnote "SNR value guaranteed ... frequency range" from parameters- $SNR_{DIFF150}$ and $SNR_{DIFF333}$. – In V_{cmrr}, changed "SR" to "CC" and "D" to "T" – Changed min value from "1.5" to "—" in parameter "I_{ADV_D}" – Changed min value from "3" to "—" in parameter "ΣI_{ADR_D}". – Added footnote "Consumption is given ... set-up" to parameter "ΣI_{ADR_D}" – Removed footnote "Sampling is .... $f_{ADCD_M}/2$" – Updated footnote "S/D ADC is ...12 dB" – Added table footnote "This parameter ...3 dB less" to parameters - $SNR_{DIFF150}$, $SNR_{DIFF333}$, and SNR_{SE150} – Replaced the max value of ΣI_{ADR_D} of "16" with "80". *Figure 8: Input equivalent circuit (Fast SARn and SARB channels)*: Updated the figure. *Table 30: Temperature sensor electrical characteristics*: For "temperature monitoring range", classification removed (was C) *Table 35: LFAST PLL electrical characteristics*: – Min and Max value of parameter "ERR_{REF}" updated from "TBD" to "-1" and "+1" respectively – Max value of parameter "PN" updated from "TBD" to "-58" – Frequency of parameter "ΔPER_{REF}" updated from "10MHz" to "20MHz". – Max value of parameter "ΔPER_{REF}" for condition "Single period" updated from "TBD" to "350" – Min and Max value of parameter "ΔPER_{REF}" for condition "Long period" updated from "TBD" to "-500" and "+500" respectively. *Table 36: Aurora LVDS electrical characteristics,*: – For parameter $\lvert\Delta V_{I_L}\rvert$, changed classification to "T" – For parameter $\lvert\Delta V_{OD_LVDS}\rvert$, changed the classification to "T".