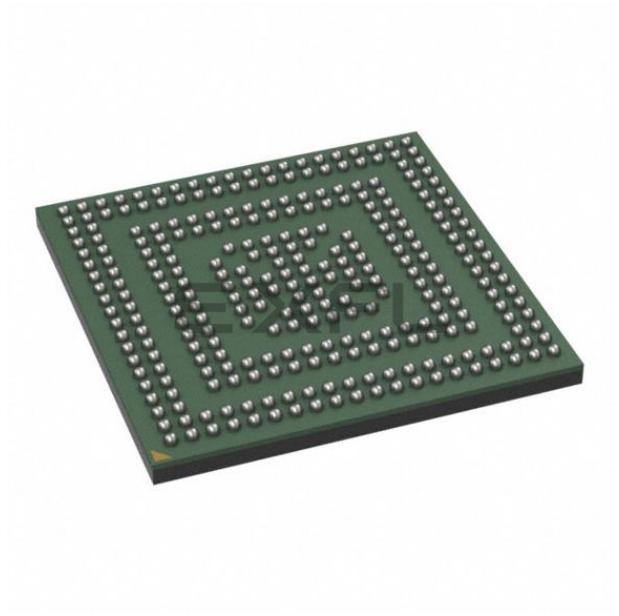

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Program Memory Type	FLASH
EEPROM Size	256K x 8
RAM Size	608K x 8
Voltage - Supply (Vcc/Vdd)	1.2V, 3.3V, 5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	292-FBGA
Supplier Device Package	292-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc58ne84c3qmhar

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Table 5. Operating conditions (continued)

Symbol		C	Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
$V_{SS\_HV\_ADR\_D}$-$V_{SS\_HV\_ADV}$	SR	D	$V_{SS\_HV\_ADR\_D}$ differential voltage	—	–25	—	25	mV
$V_{DD\_HV\_ADR\_S}$	SR	P	SAR ADC reference voltage	—	3.0	—	5.5	V
$V_{DD\_HV\_ADR\_S}$-$V_{DD\_HV\_ADV}$	SR	D	SAR ADC reference differential voltage	—	$V_{DD\_HV\_ADV}$ -10%	—	25	mV
$V_{SS\_HV\_ADR\_S}$	SR	P	SAR ADC ground reference voltage	—	$V_{SS\_HV\_ADV}$			V
$V_{SS\_HV\_ADR\_S}$-$V_{SS\_HV\_ADV}$	SR	D	$V_{SS\_HV\_ADR\_S}$ differential voltage	—	–25	—	25	mV
V_{RAMP_LV}	SR	D	Slew rate on core power supply pins	V_{DD_LV} $V_{DD\_LV\_BD}$	—	—	20	V/ms
V_{RAMP_HV}	SR	D	Slew rate on HV power supply	—	—	—	100	V/ms
V_{IN}	SR	P	I/O input voltage range	—	0	—	5.5	V
I_{INJ1}	SR	T	DC Injection current (per pin) without performance degradation(8) (9) (10)	Digital pins and analog pins	–3.0	—	3.0	mA
I_{INJ2}	SR	D	Dynamic Injection current (per pin) with performance degradation(10) (11)	Digital pins and analog pins	–10	—	10	mA

1. The ranges in this table are design targets and actual data may vary in the given range.
2. The maximum number of PRAM wait states has to be configured according to the system clock frequency. Refer to *Table 6*.
3. Core voltage as measured on device pin to guarantee published silicon performance.
4. In the range [1.14-1.08]V, the device functionality and specifications are granted and the device is expected to receive a flag by the internal LVD100 monitors to warn that the regulator (internal or external), providing the V_{DD_LV} supply, exited the expected operating conditions. If the internal LVD100 monitors are disabled by the application, then an external voltage monitor with minimum threshold of V_{DD_LV}(min) = 1.08 V measured at the device pad, has to be implemented. Please refer to *Section 3.16.3: Voltage monitors* for the list of available internal monitors and to the Reference Manual for the configurability of the monitors.

5. Core voltage can exceed 1.26 V with the limitations provided in *Section 3.2: Absolute maximum ratings*, provided that HVD134_C monitor reset is disabled.
6. 1.260 V - 1.290 V range allowed periodically for supply with sinusoidal shape and average supply value below or equal to 1.236 V at the given temperature profile.
7. S/D ADC is functional in the range 3.0 V < $V_{DD\_HV\_ADV}$ < 4.0 V and 3.0 V < $V_{DD\_HV\_ADR\_D}$ < 4.0 V, but precision of conversion is not guaranteed.
8. Full device lifetime. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See *Section 3.2: Absolute maximum ratings* for maximum input current for reliability requirements.
9. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pins is above the supply rail, current will be injected through the clamp diode to the supply rails. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
10. The limits for the sum of all normal and injected currents on all pads within the same supply segment can be found in *Section 3.8.3: I/O pad current specifications*.
11. Positive and negative Dynamic current injection pulses are allowed up to this limit, with different specifications for I/O, ADC accuracy and analog input. See the dedicated chapters for the different specification limits. See the Absolute Maximum Ratings table for maximum input current for reliability requirements. Refer to the following pulses definitions: Pulse1 (ISO 7637-2:2011), Pulse 2a(ISO 7637-2:2011 5.6.2), Pulse 3a (ISO 7637-2:2011 5.6.3), Pulse 3b (ISO 7637-2:2011 5.6.3).

Table 6. PRAM wait states configuration

PRAMC WS	Clock Frequency (MHz)
1	≤ 180
0	≤ 120

3.3.1 Power domains and power up/down sequencing

The following table shows the constraints and relationships for the different power domains. Supply1 (on rows) can exceed Supply2 (on columns), only if the cell at the given row and column is reporting ‘ok’. This limitation is valid during power-up and power-down phases, as well as during normal device operation.

Table 7. Device supply relation during power-up/power-down sequence

		Supply2							
		V_{DD_LV}	**$V_{DD\_HV\_IO\_FLEX}$**	**$V_{DD\_HV\_IO\_JTAG}$**	**$V_{DD\_HV\_IO\_MAIN}$ $V_{DD\_HV\_FLA}$**	**$V_{DD\_HV\_ADV}$**	**$V_{DD\_HV\_ADR}$**	**$V_{DD\_LV\_BD}$**	**$V_{DD\_HV\_BD}$**
Supply1	V_{DD_LV}(1)		ok	ok	ok	ok	ok	ok	ok
	$V_{DD\_HV\_IO\_FLEX}$	ok		ok	not allowed	ok	ok	ok	ok
	$V_{DD\_HV\_IO\_JTAG}$	ok	ok		not allowed	ok	ok	ok	ok
	$V_{DD\_HV\_IO\_MAIN}$ $V_{DD\_HV\_FLA}$	ok	ok	ok		ok	ok	ok	ok
	$V_{DD\_HV\_ADV}$	ok	ok	ok	not allowed		ok	ok	ok
	$V_{DD\_HV\_ADR}$	ok	ok	ok	not allowed	not allowed		ok	ok
	$V_{DD\_LV\_BD}$	ok	ok	ok	ok	ok	ok		ok
	$V_{DD\_HV\_BD}$	ok	ok	ok	ok	ok	ok	ok	

1. V_{DD_LV} can be higher than V_{DD_HV} supplies only during power-up/down transient ramps, in case of external LV regulator and if V_{DD_HV} supply voltage level is lower than V_{DD_LV} allowed max operating condition.

During power-up, all functional terminals are maintained in a known state as described in the device pin out IO definition excel file table.

Table 9. Device consumption(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$I_{DD\_LV\_BD}$	CC	P	Buddy Device Consumption on V_{DD_LV} supply(12)	T_J = 150 °C	—	—	500	mA
		D		T_J = 165 °C	—	—	600	
$I_{DD\_HV\_BD}$	CC	T	Buddy Device Consumption on V_{DD_HV} supply(12)	—	—	—	130	mA
I_{SPIKE}	SR	T	Maximum short term current spike(13)	< 20 µs observation window	—	—	100	mA
dI	SR	D	Current difference ratio to average current (dI/avg(I))(14)	20 µs observation window	—	—	20	%
I_{SR}(15)	CC	D	Current variation during power up/down	See footnote(16)	—	—	200	mA
I_{DDOFF}	CC	T	Power-off current on high voltage supply rails(17)	V_{DD_HV} = 2.5 V	100	—	—	µA

1. The ranges in this table are design targets and actual data may vary in the given range.
2. The leakage considered is the sum of core logic and RAM memories. The contribution of analog modules is not considered, and they are computed in the dynamic I_{DD_LV} and I_{DD_HV} parameters.
3. IDD_LKG (leakage current) and IDD_LV (dynamic current) are reported as separate parameters, to give an indication of the consumption contributors. The tests used in validation, characterization and production are verifying that the total consumption (leakage+dynamic) is lower or equal to the sum of the maximum values provided (IDD_LKG+IDD_LV). The two parameters, measured separately, may exceed the maximum reported for each, depending on the operative conditions and the software profile used.
4. Use case: The switching activity estimated for dynamic consumption is: 7% cores (fMAX), 4% fast platform (fMAX), 2% slow platform (fMAX/2) and IPs (fMAX/2). Consumption does not include I/O toggling, which is highly dependent on the application. ADC and other analog modules are included; Flash consumption includes parallel read and program/erase. Details of the SW configuration are available separately. The total device consumption is I_{DD_LV} + I_{DD_HV} + I_{DD_LKG} for the selected temperature.
5. Transmission use case: Three cores running at fMAX with all locksteps on, DMA, PLL, FLASH, 2xCAN, GTM (50% idle, 40% at fMAX/4, 10% at fMAX/2), HSM, 3xSAR.
6. Powertrain use case: Three cores running at fMAX with 2 core locksteps on, DMA, PLL, FLASH, 3xCAN, 1xFlexray, GTM (50% idle, 40% at fMAX/4, 10% at fMAX/2), HSM, 3xSAR, 2xADCSD.
7. Dynamic consumption of one core, including the dedicated I/D-caches and I/D-MEMS contribution.
8. Dynamic consumption of the HSM module, including the dedicated memories, during the execution of Electronic Code Book crypto algorithm on 1 block of 16 byte of shared RAM
9. Dynamic consumption of the AMU module standalone.
10. Flash in Low Power. Sysclk at 160 MHz, PLL0_PHI at 160 MHz, XTAL at 40 MHz, FIRC 16 MHz ON, RCOSC1M off. FlexCAN: instances: 0, 1, 2, 3, 4, 5, 6, 7 ON (configured but no reception or transmission), Ethernet ON (configured but no reception or transmission), ADC ON (continuously converting). All others IPs clock-gated.
11. Sysclk = RC16 MHz, RC16 MHz ON, RC1 MHz ON, PLL OFF. All possible peripherals off and clock gated. Flash in power down mode.
12. Worst case usage (data trace, data overlay, full Aurora utilization). If Aurora and JTAGM/LFAST not used, $V_{DD\_LV\_BD}$ current is reduced by ~20mA.
13. Current spike may occur during normal operation that are above average current, measured on application specific pattern. Internal schemes must be used (eg frequency ramping, feature enable) to ensure that incremental demands are made on the external power supply. An internal auxiliary and clamp regulator can be enabled, in order to support internal current variations. Please refer to the Power Management chapter for the details and the external component requirements.
14. Moving window, measured on application specific pattern, with a maximum of 100 mA for the worst case application.

15. This specification is the maximum value and is a boundary for the dI specification.
16. Condition1: For power on period from 0 V up to normal operation with reset asserted. Condition 2: From reset asserted until PLL running free. Condition 3: Increasing PLL from free frequency to full frequency. Condition 4: reverse order for power down to 0 V.
17. I_{DDOFF} is the minimum guaranteed consumption of the device during power-up. It can be used to correctly size power-off ballast in case of current injection during power-off state.

3.8.3 I/O pad current specifications

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in the device pin out IO definition excel file.

Table 17 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{RMSSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Pad mapping on each segment can be optimized using the pad usage information provided on the I/O Signal Description table.

Note: In order to ensure the correct functionality for SENT, the sum of all pad usage ratio within the SENT segment should remain below 10%.

Table 17. I/O consumption(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Average consumption(2)								
I_{RMSSEG}	SR	D	Sum of all the DC I/O current within a supply segment	—	—	—	80	mA
I_{RMS_W}	CC	D	RMS I/O current for WEAK configuration	C_L = 25 pF, 2 MHz, V_{DD} = 5.0 V ± 10%	—	—	1.1	mA
				C_L = 50 pF, 1 MHz, V_{DD} = 5.0 V ± 10%	—	—	1.1	
				C_L = 25 pF, 2 MHz, V_{DD} = 3.3 V ± 10%	—	—	1.0	
				C_L = 25 pF, 1 MHz, V_{DD} = 3.3 V ± 10%	—	—	1.0	
I_{RMS_M}	CC	D	RMS I/O current for MEDIUM configuration	C_L = 25 pF, 12 MHz, V_{DD} = 5.0 V ± 10%	—	—	5.5	mA
				C_L = 50 pF, 6 MHz, V_{DD} = 5.0 V ± 10%	—	—	5.5	
				C_L = 25 pF, 12 MHz, V_{DD} = 3.3 V ± 10%	—	—	4.2	
				C_L = 25 pF, 6 MHz, V_{DD} = 3.3 V ± 10%	—	—	4.2	

3.11.4 Low power RC oscillator

Table 25. 1024 kHz internal RC oscillator electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
F_{sirc}	CC	T	Slow Internal RC oscillator frequency	—	—	1024	—	kHz
δf_{var_T}	CC	P	Frequency variation across temperature	–40 °C < T < 150 °C	–9	—	+9	%
δf_{var_V}	CC	P	Frequency variation across voltage	–40 °C < T < 150 °C	–5	—	+5	%
I_{sirc}	CC	T	Slow Internal RC oscillator current	T = 55 °C	—	—	6	µA
T_{sirc}	CC	T	Start up time, after switching ON the internal regulator.	—	—	—	12	µS

Table 28. ADC-Comparator electrical specification(1) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
ΔTUE_{10}	CC	D	TUE degradation due to $V_{DD\_HV\_ADR}$ offset with respect to $V_{DD\_HV\_ADV}$	$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	–1.0	1.0	LSB (10b)
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–2.0	2.0	
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–3.5	3.5	
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–6.0	6.0	
				$V_{DD\_HV\_ADV} < V_{IN} <$ $V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	–2.5	2.5	
				$V_{DD\_HV\_ADV} < V_{IN} <$ $V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–4.0	4.0	
				$V_{DD\_HV\_ADV} < V_{IN} <$ $V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–7.0	7.0	
				$V_{DD\_HV\_ADV} < V_{IN} <$ $V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–12.0	12.0	
TUE_{INJ2}	CC	T	TUE degradation addition, due to current injection in I_{INJ2} range.(5)	See *Table 5: Operating conditions*, I_{INJ2} parameter.	3		LSB
DNL(6)	CC	P	Differential non-linearity std. mode	Standard frequency mode, $V_{DD\_HV\_ADV} > 4$ V $V_{DD\_HV\_ADR\_S} > 4$ V	–1	2	LSB (10b)
		T		High frequency mode, $V_{DD\_HV\_ADV} > 4$ V $V_{DD\_HV\_ADR\_S} > 4$ V	–1	2	

1. Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Minimum ADC sample times are dependent on adequate charge transfer from the external driving circuit to the internal sample capacitor. The time constant of the entire circuit must allow the sampling capacitor to charge within 1/2 LSB within the sampling window. Please refer to Figure 8 for models of the internal ADC circuit, and the values to use in external RC sizing and calculating the sampling window duration.

13. SNR value guaranteed only if external noise on the ADC input pin is attenuated by the required SNR value in the frequency range of $f_{ADCD\_M} - f_{ADCD\_S}$ to $f_{ADCD\_M} + f_{ADCD\_S}$, where f_{ADCD_M} is the input sampling frequency, and f_{ADCD_S} is the output sample frequency. A proper external input filter should be used to remove any interfering signals in this frequency range.
14. The ±1% passband ripple specification is equivalent to $20 * \log_{10}(0.99) = 0.087$ dB.
15. Propagation of the information from the pin to the register CDR[CDATA] and flags SFR[DFEF], SFR[DFFF] is given by the different modules that need to be crossed: delta/sigma filters, high pass filter, fifo module, clock domain synchronizers. The time elapsed between data availability at pin and internal S/D module registers is given by the below formula: REGISTER LATENCY = $t_{LATENCY} + 0.5/f_{ADCD\_S} + 2\ (\sim+1)/f_{ADCD\_M} + 2(\sim+1)f_{PBRIDGEx\_CLK}$ where f_{ADCD_S} is the frequency of the sampling clock, f_{ADCD_M} is the frequency of the modulator, and $f_{PBRIDGEx\_CLK}$ is the frequency of the peripheral bridge clock feeds to the ADC S/D module. The (~+1) symbol refers to the number of clock cycles uncertainty (from 0 to 1 clock cycle) to be added due to resynchronization of the signal during clock domain crossing. Some further latency may be added by the target module (core, DMA, interrupt) controller to process the data received from the ADC S/D module.
16. This capacitance does not include pin capacitance, that can be considered together with external capacitance, before sampling switch.
17. Consumption is given after power-up, when steady state is reached. Extra consumption up to 2 mA may be required during internal circuitry set-up.

Figure 16. Standby regulator with external ballast mode

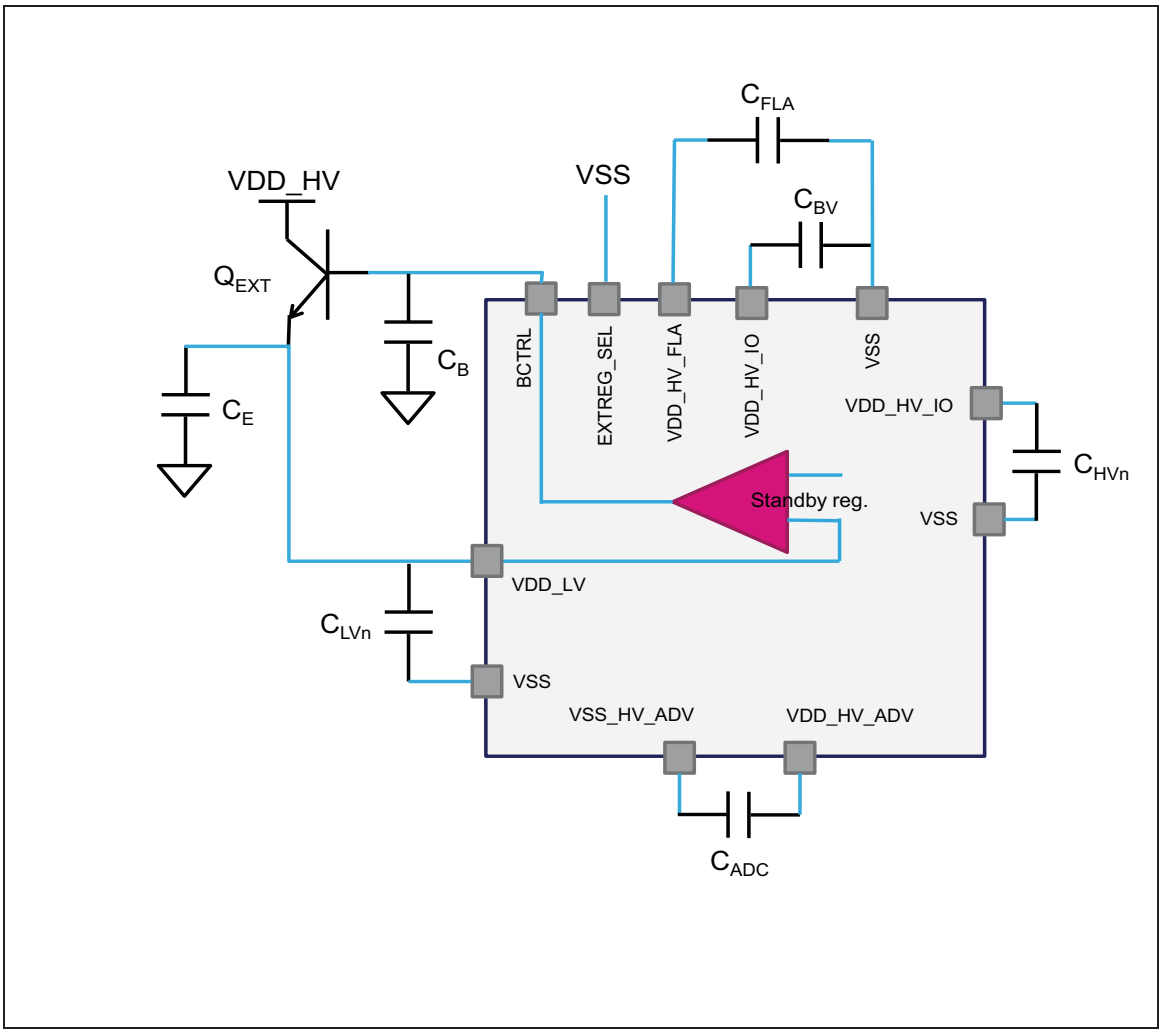


Table 38. External components integration

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
Common Components								
C_E	SR	D	Internal voltage regulator stability external capacitance.[2] [3]		—	2x2.2	—	µF
R_E	SR	D	Stability capacitor equivalent serial resistance	Total resistance including board track	—	—	50	mΩ
C_{LVn}	SR	D	Internal voltage regulator decoupling external capacitance[2] [4] [5]	Each V_{DD_LV}/V_{SS} pair	—	47	—	nF

5. For BGA and KGD applications it is recommended to implement at least 5 C_{LV} capacitances.
6. Recommended X7R capacitors. For noise filtering, add a high frequency bypass capacitance of 100 nF.
7. CB capacitance is required if only the external ballast is implemented.
8. The application has to implement one of the two recommended combinations of external components for the SMPS regulator:
   PMOS, NMOS and CS2 (common), plus CS1_A and LS_A (option A), or
   PMOS, NMOS and CS2 (common), plus CS1_B and LS_B (option B).
9. The value of the capacitance on the HV supply reported in the datasheet is a general recommendation. The application can select a different number, based on the external regulator and emc requirements.
10. Recommended X7R or X5R ceramic –35% / +35% variation across process, temperature, voltage and after aging.

3.16.2 Voltage regulators

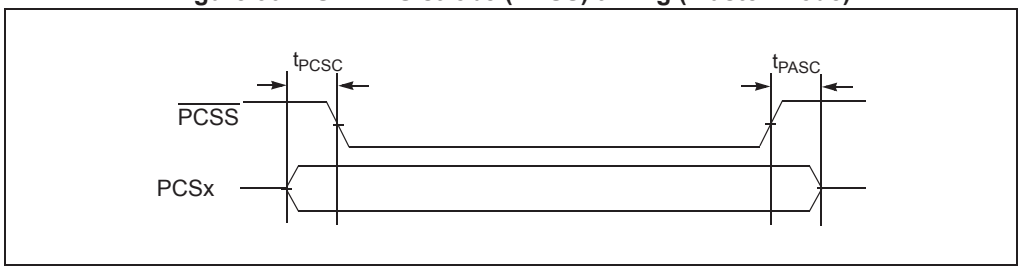
Table 39. Linear regulator specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{MREG}	CC	P	Main regulator output voltage	Power-up, before trimming, no load	1.12	1.20	1.28	V
	CC	P		After trimming, maximum load	1.08	1.18	1.23	
IDD_{MREG}	CC	T	Main regulator current provided to V_{DD_LV} domain The maximum current required by the device (I_{DD_LV}) may exceed the maximum current which can be provided by the internal linear regulator. In this case, the internal regulator mode cannot be used.	—	—	—	700	mA
IDD_{CLAMP}	CC	D	Main regulator rush current sinked from $V_{DD\_HV\_IO\_MAIN}$ domain during V_{DD_LV} domain loading	Power-up condition	—	—	400	mA
ΔIDD_{MREG}	CC	T	Main regulator current variation	20 µs observation window	—	—	—	mA
$I_{MREGINT}$	CC	D	Main regulator current consumption	I_{MREG} = max	—	—	22	mA
		D		I_{MREG} = 0 mA	—	—	—	

Table 40. Auxiliary regulator specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{AUX}	CC	P	Aux regulator output voltage	After trimming, internal regulator mode	1.08	1.18	1.21	V
	CC	P		After trimming, external regulator mode	1.03	1.12	1.16	
IDD_{AUX}	CC	T	Aux regulator current provided to V_{DD_LV} domain	—	—	—	250	mA
ΔIDD_{AUX}	CC	T	Aux regulator current variation	20 µs observation window	–100	—	100	mA
I_{AUXINT}	CC	D	Aux regulator current consumption	I_{MREG} = max	—	—	1.1	mA
		D		I_{MREG} = 0 mA	—	—	1.1	

Figure 30. DSPI PCS strobe ($\overline{PCSS}$) timing (master mode)



3.18.2.1.2 DSPI CMOS master mode — modified timing

Table 55. DSPI CMOS master modified timing (full duplex and output only) — MTFE = 1, CPHA = 0 or 1(1)

#	Symbol		C	Characteristic	Condition		Value(2)		Unit
					Pad drive(3)	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	33.0	—	ns
					Strong	50 pF	80.0	—	
					Medium	50 pF	200.0	—	
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	ns
					Strong	50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	
					Medium	50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 29$	—	
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
					Medium	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
4	t_{SDC}	CC	D	SCK duty cycle(7)	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	
					Medium	0 pF	$^1/_2t_{SCK} - 5$	$^1/_2t_{SCK} + 5$	

3.18.4.2 TxD

Figure 48. TxD signal

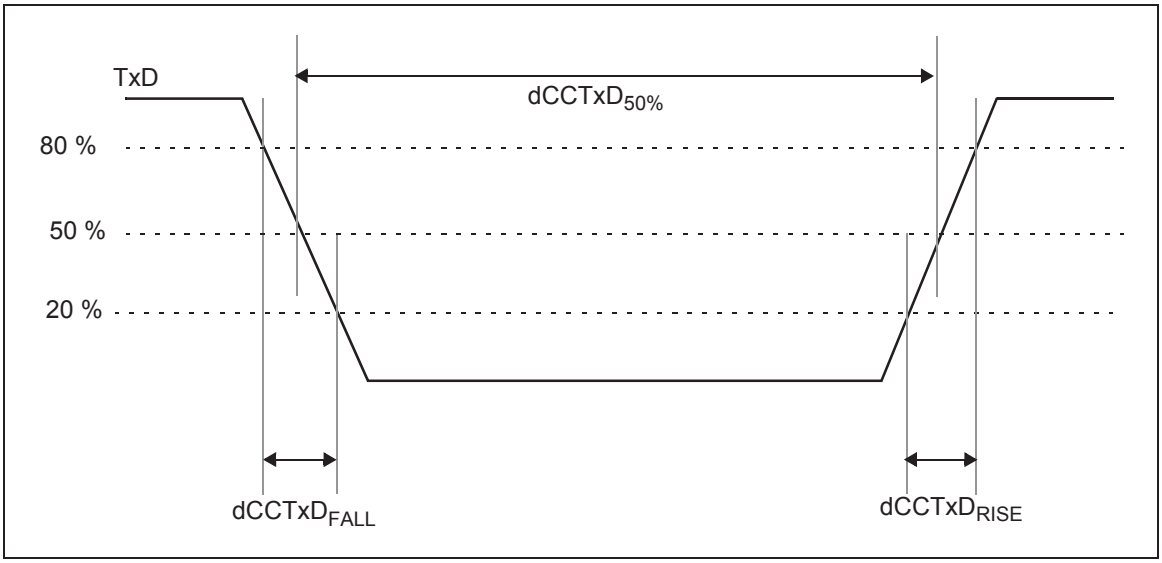


Table 68. TxD output characteristics(1),(2)

Symbol		C	Characteristic	Value		Unit
				Min	Max	
dCCTxAsym	CC	D	Asymmetry of sending CC at 25 pF load (= $dCCTxD_{50\%}$ – 100 ns)	–2.45	2.45	ns
$dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$	CC	D	Sum of Rise and Fall time of TxD signal at the output pin(3),(4)	—	9(5)	ns
		D		—	9(6)	
$dCCTxD_{01}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxD_{10}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. TxD pin load maximum 25 pF.
2. Specifications valid according to FlexRay EPL 3.0.1 standard with 20%–80% levels and a 10 pF load at the end of a 50 Ohm, 1 ns stripline. Please refer to the Very Strong I/O pad specifications.
3. Pad configured as VERY STRONG.
4. Sum of transition time simulation is performed according to Electrical Physical Layer Specification 3.0.1 and the entire temperature range of the device has been taken into account.
5. $V_{DD\_HV\_IO}$ = 5.0 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 1 ns, C_L = 10 pF.
6. $V_{DD\_HV\_IO}$ = 3.3 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 0.6 ns, C_L = 10 pF.

Table 76. eLQFP176 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09	—	0.20	0.003	—	0.008
D	25.80	26.00	26.20	1.016	1.023	1.031
D1	23.90	24.00	24.10	0.941	0.945	0.949
D2[2]	7.30	—	8.95	0.287	—	0.352
D3	—	21.5	—	—	0.846	—
E	25.80	26.00	26.20	1.016	1.023	1.031
E1	23.90	24.00	24.10	0.941	0.945	0.949
E2	7.30	—	8.95	0.287	—	0.352
E3[2]	—	21.50	—	—	0.846	—
e	—	0.50	—	—	0.019	—
L	0.45	0.60	0.75		0.024	
L1	—	1.00	—	—	0.039	—
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	—	—	0.08	—	—	0.003

1. Values in inches are converted from millimeters (mm) and rounded to four decimal digits.
2. The size of exposed pad is variable depending on leadframe design pad size.

mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

When board temperature is perfectly defined below the device, it is possible to use the thermal characterization parameter (Ψ_{JPB}) to determine the junction temperature by measuring the temperature at the bottom center of the package case (exposed pad) using the following equation:

Equation 5

$$T_J = T_B + (\Psi_{JPB} \times P_D)$$

where:

T_T = thermocouple temperature on bottom of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

Table 81. RAM options[1] (continued)

SPC58NE84	SPC58EE84	SPC58NE80	SPC58EE80	Type	Start address	End address
768	768	768	768			
64	64	64	64	D_MEM CPU_0	0x50800000	0x5080FFFF
64	64	64	64	D_MEM CPU_1	0x51800000	0x5180FFFF
32	32	32	32	D_MEM CPU_2	0x52800000	0x52807FFF

1. RAM size is the sum of TCM and SRAM.