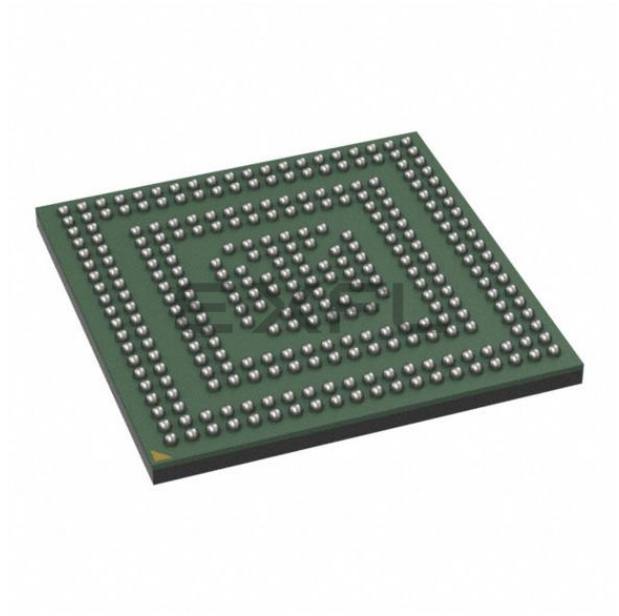

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Tri-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA
Number of I/O	64
Program Memory Size	6MB (6M x 8)
Program Memory Type	FLASH
EEPROM Size	256K x 8
RAM Size	608K x 8
Voltage - Supply (Vcc/Vdd)	1.2V, 3.3V, 5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	292-BGA
Supplier Device Package	292-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc58ne84c3qmhay

Table 2. SPC58xEx feature summary

Feature	Description
Interrupt controller	> 710 sources
ADC (SAR)	8
ADC (SD)	6
Temp. sensor	Yes
Self Test Controller	Yes
PLL	Dual PLL with FM
Integrated linear voltage regulator	Yes(1)
Integrated switch mode voltage regulator (SMPS)	Yes(2)
External Power Supplies	3.3 V - 5 V, 1.2 V
Low Power Modes	Stop Mode
	Halt Mode
	Smart Standby with output controller, analog and digital inputs(1)
	Standby Mode(1)

1. Except eLQFP176.
2. Except LFBGA292.

1.4 Block diagram

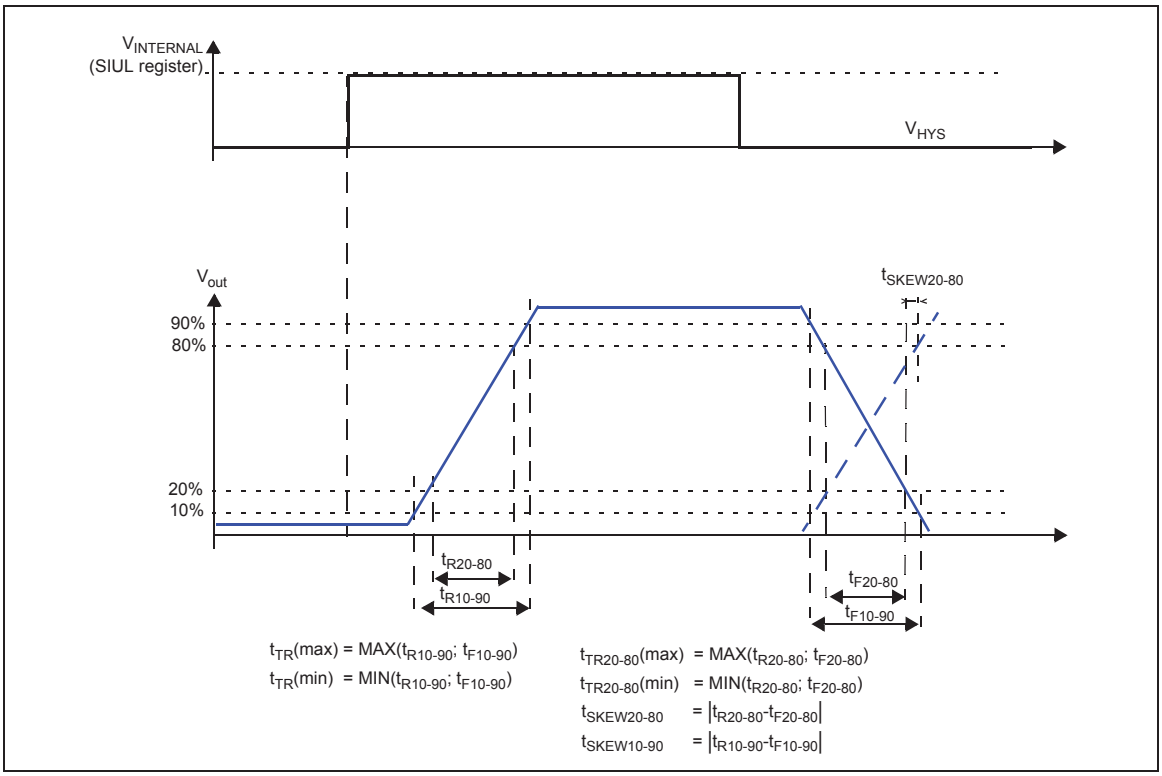
Figure 1 and *Figure 2* show the top-level block diagrams.

3.7 Device consumption

Table 9. Device consumption(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{DD_LKG}(2),(3)	CC	C	Leakage current on the V_{DD_LV} supply	T_J = 40 °C	—	—	40	mA
		D		T_J = 120 °C	—	—	180	
		P		T_J = 150 °C	—	—	320	
		D		T_J = 165 °C	—	—	500	
I_{DD_LV}(3)	CC	P	Dynamic current on the V_{DD_LV} supply, very high consumption profile(4)	—	—	—	489	mA
I_{DD_HV}	CC	P	Total current on the V_{DD_HV} supply(4)	f_{MAX}	—	—	97	mA
$I_{DD\_LV\_TCU}$	CC	T	Dynamic current on the V_{DD_LV} supply, transmission profile(5)	—	—	—	404	mA
$I_{DD\_HV\_TCU}$	CC	T	Dynamic current on the V_{DD_HV} supply, transmission profile(5)	—	—	—	80	mA
$I_{DD\_LV\_ECU}$	CC	T	Dynamic current on the V_{DD_LV} supply, powertrain profile(6)	—	—	—	396	mA
$I_{DD\_HV\_ECU}$	CC	T	Dynamic current on the V_{DD_HV} supply, powertrain profile(6)	—	—	—	83	mA
$I_{DD\_MAIN\_CORE\_AC}$	CC	T	Main Core dynamic current(7)	f_{MAX}	—	—	50	mA
$I_{DD\_CHKR\_CORE\_AC}$	CC	T	Checker Core dynamic operating current	f_{MAX}	—	—	30	mA
$I_{DD\_HSM\_AC}$	CC	T	HSM platform dynamic operating current(8)	$f_{MAX}/2$	—	—	20	mA
$I_{DD\_AMU\_AC}$	CC	T	AMU dynamic operating current(9)	f_{MAX}	—	—	20	mA
I_{DDHALT}(10)	CC	T	Dynamic current on the V_{DD_LV} supply +Total current on the V_{DD_HV} supply	—	—	110	180	mA
I_{DDSTOP}(11)	CC	T	Dynamic current on the V_{DD_LV} supply +Total current on the V_{DD_HV} supply	—	—	21	40	mA

Figure 4. I/O output DC electrical characteristics definition



The following tables provide DC characteristics for bidirectional pads:

- *Table 13* provides output driver characteristics for I/O pads when in WEAK/SLOW configuration.
- *Table 14* provides output driver characteristics for I/O pads when in MEDIUM configuration.
- *Table 15* provides output driver characteristics for I/O pads when in STRONG/FAST configuration.
- *Table 16* provides output driver characteristics for I/O pads when in VERY STRONG/VERY FAST configuration.

Note: 10%/90% is the default condition for any parameter if not explicitly mentioned differently.

Table 13. WEAK/SLOW I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ol_W}	CC	D	Output low voltage for Weak type PADs	I_{ol} = 0.5 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	0.1*V_{DD}	V
V_{oh_W}	CC	D	Output high voltage for Weak type PADs	Ioh = 0.5 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	0.9*V_{DD}	—	—	V

Table 28. ADC-Comparator electrical specification(1) (continued)

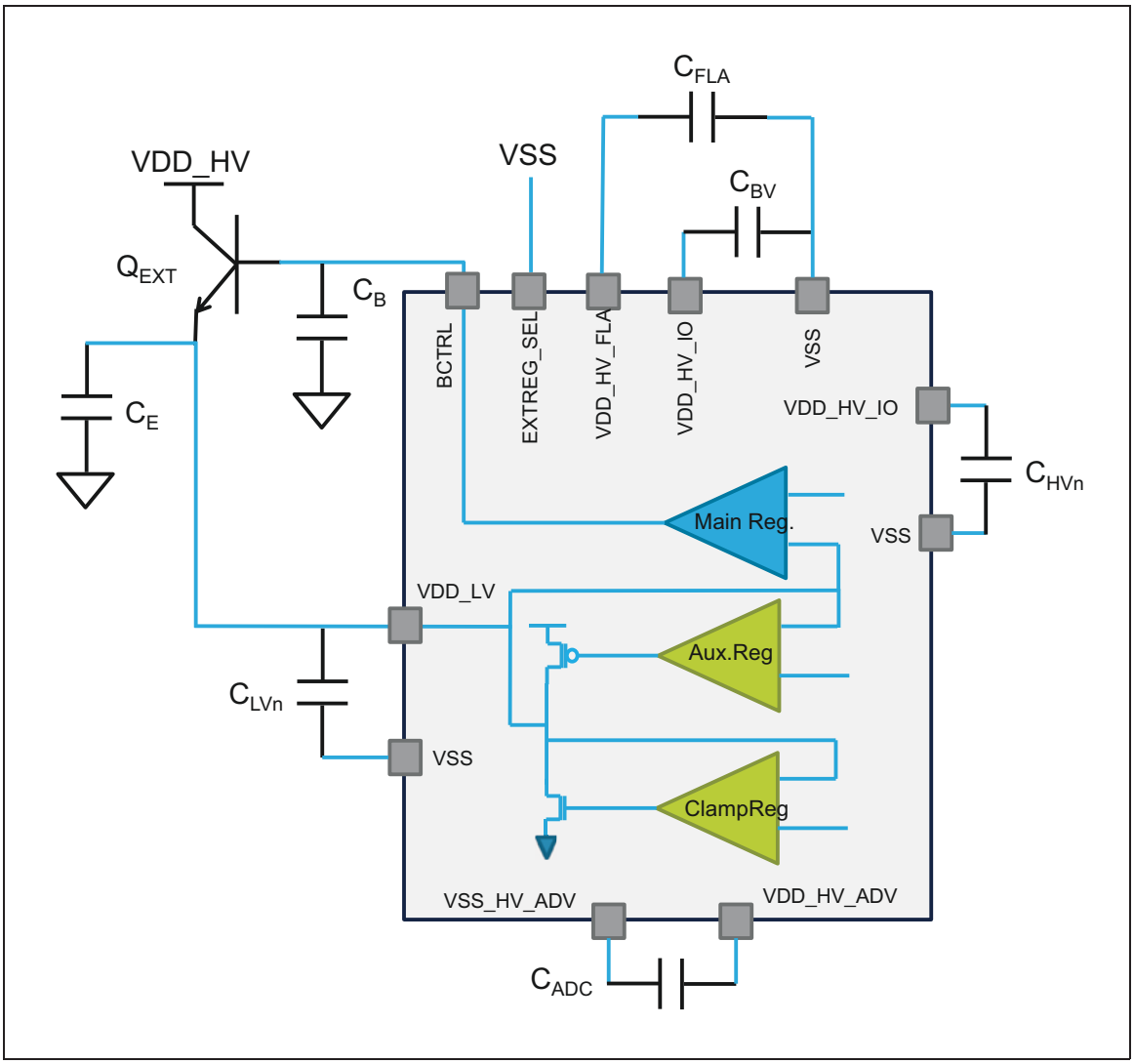
Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
TUE_{10}	CC	T	Total unadjusted error in 10-bit configuration(6)	T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V, $V_{DD\_HV\_ADR\_S}$ > 3 V	–2	2	LSB (10b)
		P		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V, $V_{DD\_HV\_ADR\_S}$ > 3 V	–3	3	
		T		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V, 3 V > $V_{DD\_HV\_ADR\_S}$ > 2 V	–3	3	
		T		T_J < 165 °C, $V_{DD\_HV\_ADV}$ > 3 V, $V_{DD\_HV\_ADR\_S}$ > 3 V	–3	3	
		T		T_J < 165 °C, $V_{DD\_HV\_ADV}$ > 3 V, 3 V > $V_{DD\_HV\_ADR\_S}$ > 2 V	–4	4	
		D		High frequency mode, T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 3 V, $V_{DD\_HV\_ADR\_S}$ > 3 V	–3	3	

Table 35. LFAST PLL electrical characteristics[1] (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
DC_{REF}	CC	D	PLL reference clock duty cycle (CLKIN)	—	30	—	70	%
PN	CC	D	Integrated phase noise (single side band)	f_{RF_REF} = 20 MHz	—	—	-58	dBc
f_{VCO}	CC	P	PLL VCO frequency	—	312	—	320[3]	MHz
t_{LOCK}	CC	D	PLL phase lock	—	—	—	150[4]	µs
ΔPER_{REF}	SR	T	Input reference clock jitter (peak to peak)	Single period, f_{RF_REF} = 20 MHz	—	—	350	ps
		T		Long term, f_{RF_REF} = 20 MHz	-500	—	500	ps
ΔPER_{EYE}	CC	T	Output Eye Jitter (peak to peak)[5]	—	—	—	400	ps

1. The specifications in this table apply to both the interprocessor bus and debug LFAST interfaces.
2. If the input frequency is lower than 20 MHz, it is required to set a input division factor of 1.
3. The 320 MHz frequency is achieved with a 20 MHz reference clock.
4. The total lock time is the sum of the coarse lock time plus the programmable lock delay time 2 clock cycles of the peripheral bridge clock that is connected to the PLL on the device (to set the PLL enable bit).
5. Measured at the transmitter output across a 100 Ω termination resistor on a device evaluation board. See *Figure 12*.

Figure 14. Internal regulator with external ballast mode



3.17 Flash memory

The following table shows the Wait State configuration.

Table 45. Wait State configuration

APC	RWSC	Frequency range (MHz)
000(1)	0	f≤30
	1	f≤60
	2	f≤90
	3	f≤120
	4	f≤150
	5	f≤180
100(2)	0	f≤30
	1	f≤60
	2	f≤90
	3	f≤120
	4	f≤150
	5	f≤180
001(3)	2	40<f≤80
	3	40<f≤120
	4	40<f≤160
	5	40<f≤180

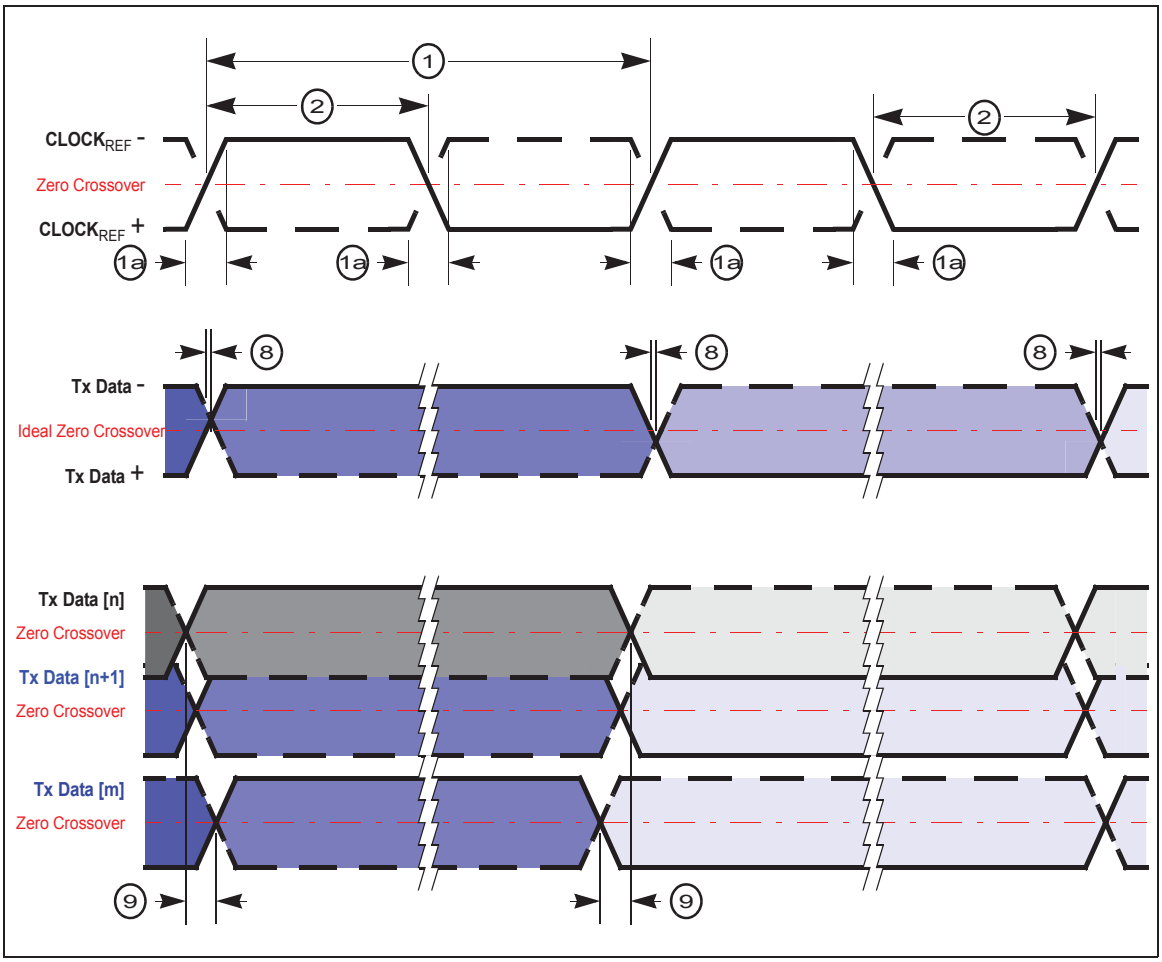
1. STD pipelined, no address anticipation.
2. No pipeline (STD + 1 Tck).
3. Pipeline with 1 Tck address anticipation.

The following table shows the Program/Erase Characteristics.

Table 46. Flash memory program and erase specifications

Symbol	Characteristics(1)(2)	Value								Unit
		Typ(3)	C	Initial max			Typical end of life(4)	Lifetime max(5)	C	
				25 °C (6)	All temp (7)	C		< 1 K cycles / ≤ 250 K cycles		
$t_{dwprogram}$	Double Word (64 bits) program time EEPROM (partitions 2, 3, 4) [KGD]	55	C	130	—	—	140	650	C	µs
$t_{pprogram}$	Page (256 bits) program time	76	C	240	—	—	255	1000	C	µs

Figure 25. Aurora timings



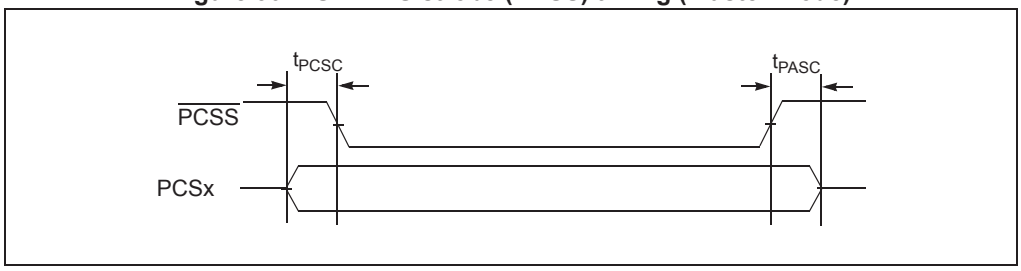
3.18.1.5 External interrupt timing (IRQ pin)

Table 52. External interrupt timing

Characteristic	Symbol	Min	Max	Unit
IRQ Pulse Width Low	t_{IPWL}	3	—	t_{cyc}
IRQ Pulse Width High	t_{IPWH}	3	—	t_{cyc}
IRQ Edge to Edge Time(1)	t_{ICYC}	6	—	t_{cyc}

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

Figure 30. DSPI PCS strobe ($\overline{PCSS}$) timing (master mode)

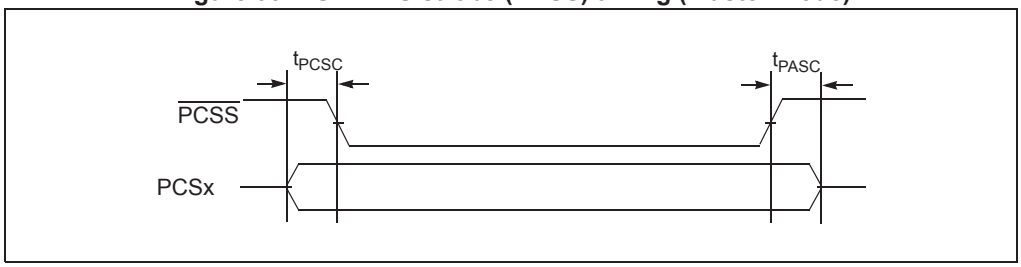


3.18.2.1.2 DSPI CMOS master mode — modified timing

Table 55. DSPI CMOS master modified timing (full duplex and output only) — MTFE = 1, CPHA = 0 or 1(1)

#	Symbol		C	Characteristic	Condition		Value(2)		Unit
					Pad drive(3)	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	33.0	—	ns
					Strong	50 pF	80.0	—	
					Medium	50 pF	200.0	—	
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	ns
					Strong	50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	
					Medium	50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 29$	—	
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
					Medium	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
4	t_{SDC}	CC	D	SCK duty cycle(7)	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	
					Medium	0 pF	$^1/_2t_{SCK} - 5$	$^1/_2t_{SCK} + 5$	

Figure 33. DSPI PCS strobe ($\overline{PCSS}$) timing (master mode)



3.18.2.1.3 DSPI LVDS master mode – modified timing

Table 56. DSPI LVDS master timing — full duplex — modified transfer format (MTFE = 1), CPHA = 0 or 1

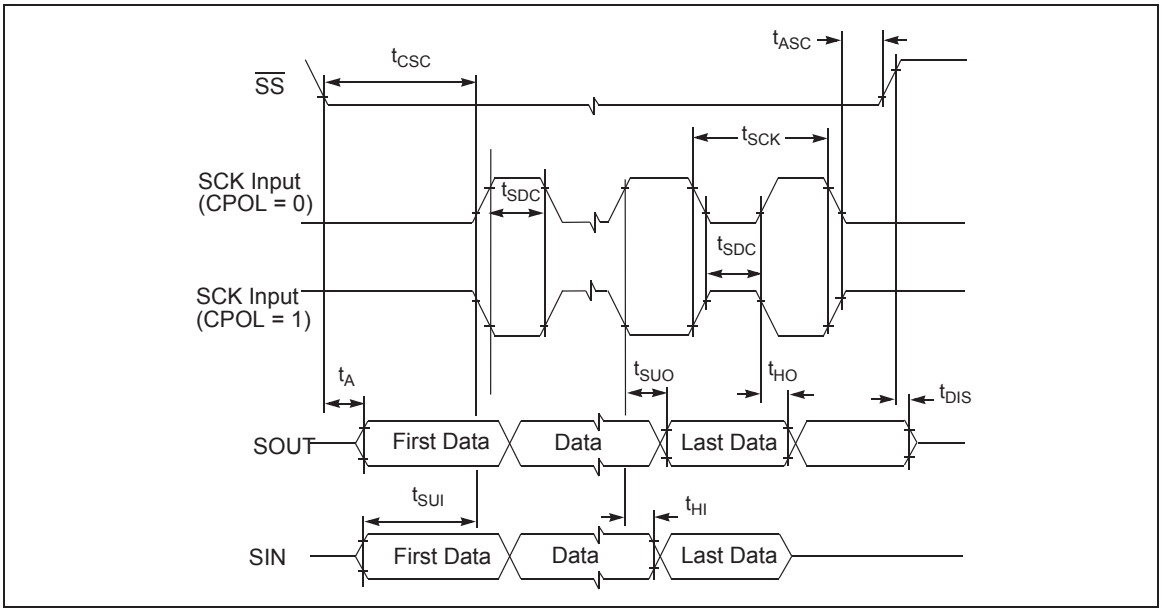
#	Symbol		C	Characteristic	Condition		Value(1)		Unit
					Pad drive	Load	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	LVDS	15 pF to 25 pF differential(2)	30.0	—	ns
2	t_{CSC}	CC	D	PCS to SCK delay (LVDS SCK)	PCS drive strength				
					Very strong	25 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 10$	—	ns
					Strong	50 pF	$(N^2 \times t_{SYS}^{(4)}) - 10$	—	ns
					Medium	50 pF	$(N^2 \times t_{SYS}^{(4)}) - 32$	—	ns
3	t_{ASC}	CC	D	After SCK delay (LVDS SCK)	Very strong	PCS = 0 pF SCK = 25 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 8$	—	ns
					Strong	PCS = 0 pF SCK = 25 pF	$(M^4 \times t_{SYS}^{(4)}) - 8$	—	ns
					Medium	PCS = 0 pF SCK = 25 pF	$(M^4 \times t_{SYS}^{(4)}) - 8$	—	ns
4	t_{SDC}	CC	D	SCK duty cycle(6)	LVDS	15 pF to 25 pF differential	$^1/_2 t_{SCK} - 2$	$^1/_2 t_{SCK} + 2$	ns
7	t_{SUI}	CC	D	SIN setup time					
				SIN setup time to SCK CPHA = 0(7)	SCK drive strength				
					LVDS	15 pF to 25 pF differential	$23 - (P^{(8)} \times t_{SYS}^{(4)})$	—	ns
				SIN setup time to SCK CPHA = 1(7)	SCK drive strength				
					LVDS	15 pF to 25 pF differential	23	—	ns

Table 59. DSPI CMOS slave timing — full duplex — normal and modified transfer formats (MTFE = 0/1) (continued)

#	Symbol		C	Characteristic	Condition		Min	Max	Unit
					Pad Drive	Load			
6	t_{DIS}	CC	D	Slave SOUT Disable Time(1) (2) (3) ($\overline{SS}$ inactive to SOUT High-Z or invalid)	Very strong	25 pF	—	5	ns
					Strong	50 pF	—	5	ns
					Medium	50 pF	—	10	ns
9	t_{SUI}	CC	D	Data Setup Time for Inputs(1)	—	—	10	—	ns
10	t_{HI}	CC	D	Data Hold Time for Inputs(1)	—	—	10	—	ns
11	t_{SUO}	CC	D	SOUT Valid Time(1) (2) (3) (after SCK edge)	Very strong	25 pF	—	30	ns
					Strong	50 pF	—	30	ns
					Medium	50 pF	—	50	ns
12	t_{HO}	CC	D	SOUT Hold Time(1) (2) (3) (after SCK edge)	Very strong	25 pF	2.5	—	ns
					Strong	50 pF	2.5	—	ns
					Medium	50 pF	2.5	—	ns

1. Input timing assumes an input slew rate of 1 ns (10% - 90%) and uses TTL / Automotive voltage thresholds.
2. All timing values for output signals in this table, are measured to 50% of the output voltage.
3. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

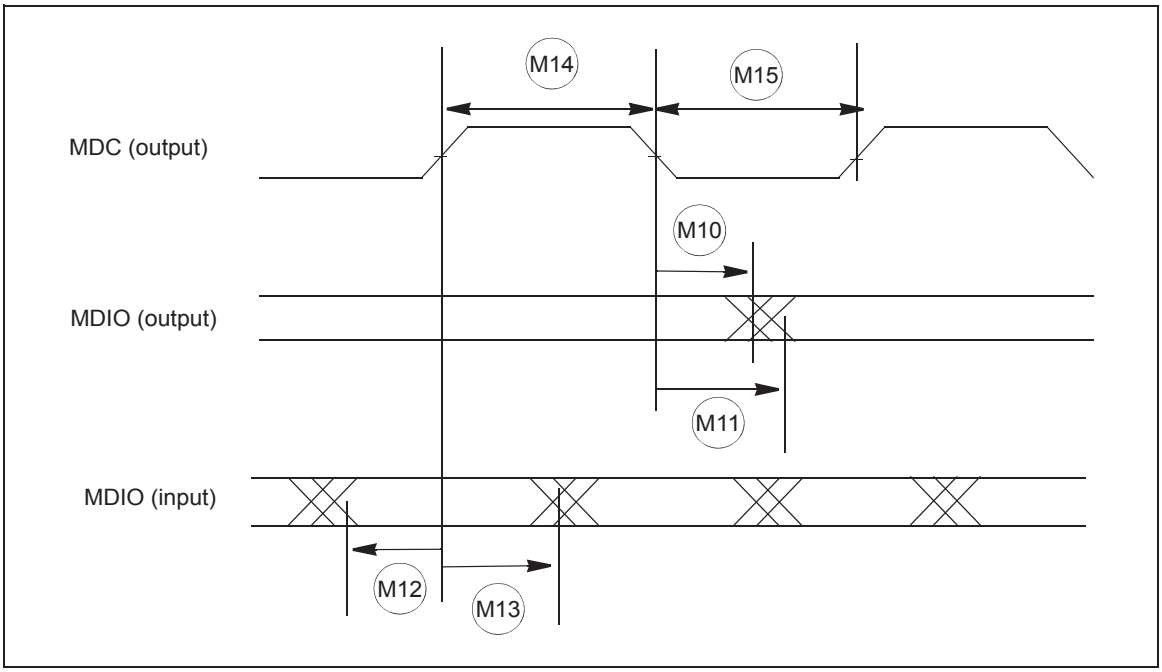
Figure 37. DSPI slave mode — modified transfer format timing (MFTE = 0/1) CPHA = 0



3.18.3.4 MII and RMII serial management channel timing (MDIO and MDC)

The Ethernet functions correctly with a maximum MDC frequency of 2.5 MHz.

Figure 42. MII serial management channel timing diagram



3.18.3.5 MII and RMII serial management channel timing (MDIO and MDC)

The Ethernet functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 63. MII serial management channel timing(1)

Symbol		C	Characteristic	Value		Unit
				Min	Max	
M10	CC	D	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	CC	D	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	CC	D	MDIO (input) to MDC rising edge setup	10	—	ns
M13	CC	D	MDIO (input) to MDC rising edge hold	0	—	ns
M14	CC	D	MDC pulse width high	40%	60%	MDC period
M15	CC	D	MDC pulse width low	40%	60%	MDC period

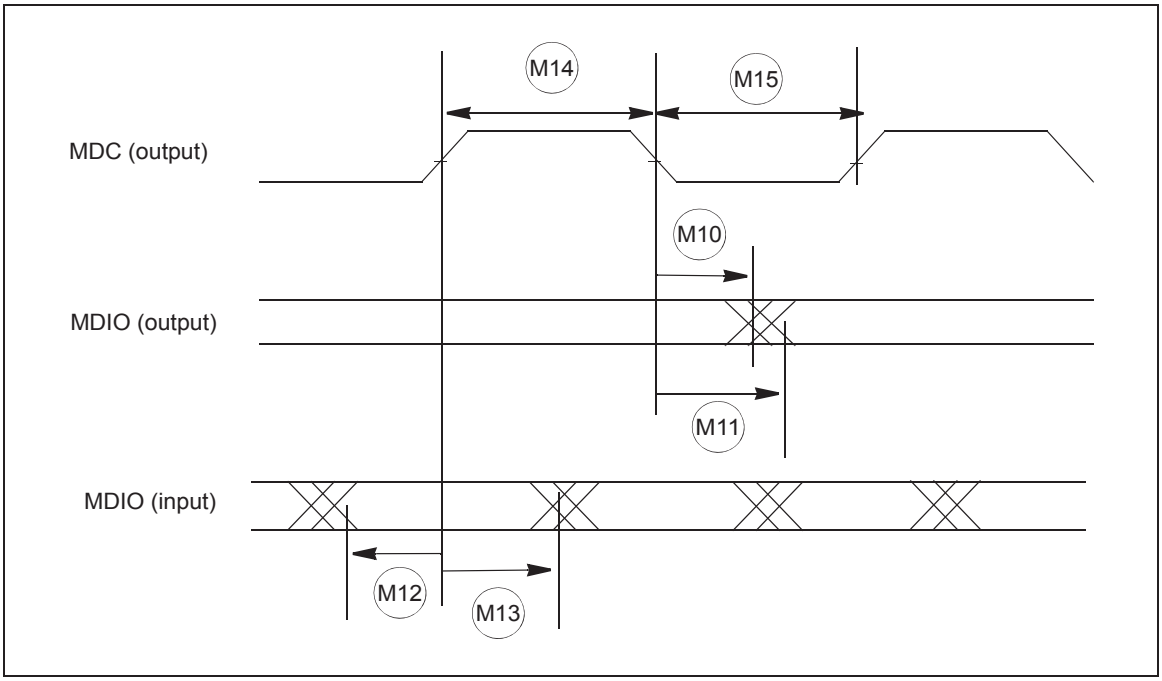
1. All timing specifications are referenced from MDC = 1.4 V (TTL levels) to the valid input and output levels, 0.8 V and 2.0 V (TTL levels). For 5 V operation, timing is referenced from MDC = 50% to 2.2 V/3.5 V input and output levels.

Table 64. RMII serial management channel timing[1]

Symbol		C	Characteristic	Value		Unit
				Min	Max	
M10	CC	D	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	CC	D	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	CC	D	MDIO (input) to MDC rising edge setup	10	—	ns
M13	CC	D	MDIO (input) to MDC rising edge hold	0	—	ns
M14	CC	D	MDC pulse width high	40%	60%	MDC period
M15	CC	D	MDC pulse width low	40%	60%	MDC period

1. All timing specifications are referenced from MDC = 1.4 V (TTL levels) to the valid input and output levels, 0.8 V and 2.0 V (TTL levels). For 5 V operation, timing is referenced from MDC = 50% to 2.2 V/3.5 V input and output levels.

Figure 43. MII serial management channel timing diagram



3.18.3.6 RMII receive signal timing (RXD[1:0], CRS_DV)

The receiver functions correctly up to a REF_CLK maximum frequency of 50 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency, which is half that of the REF_CLK frequency.

Table 74. I2C output timing specifications — SCL and SDA(1),(2),(3),(4)

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	—	CC	D	Start condition hold time	6	—	PER_CLK Cycle(5)
2	—	CC	D	Clock low time	10	—	PER_CLK Cycle
3	—	CC	D	Bus free time between Start and Stop condition	4.7	—	µs
4	—	CC	D	Data hold time	7	—	PER_CLK Cycle
5	—	CC	D	Clock high time	10	—	PER_CLK Cycle
6	—	CC	D	Data setup time	2	—	PER_CLK Cycle
7	—	CC	D	Start condition setup time (for repeated start condition only)	20	—	PER_CLK Cycle
8	—	CC	D	Stop condition setup time	10	—	PER_CLK Cycle

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device (lumped). The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.
3. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
4. Programming the IBFD register (I^2C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I^2C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the pre-scale and division values programmed in the IBC field of the IBFD register.
5. PER_CLK is the SoC peripheral clock, which drives the I^2C BIU and module clock inputs. See the Clocking chapter in the device reference manual for more detail.

Figure 50. I^2C input/output timing

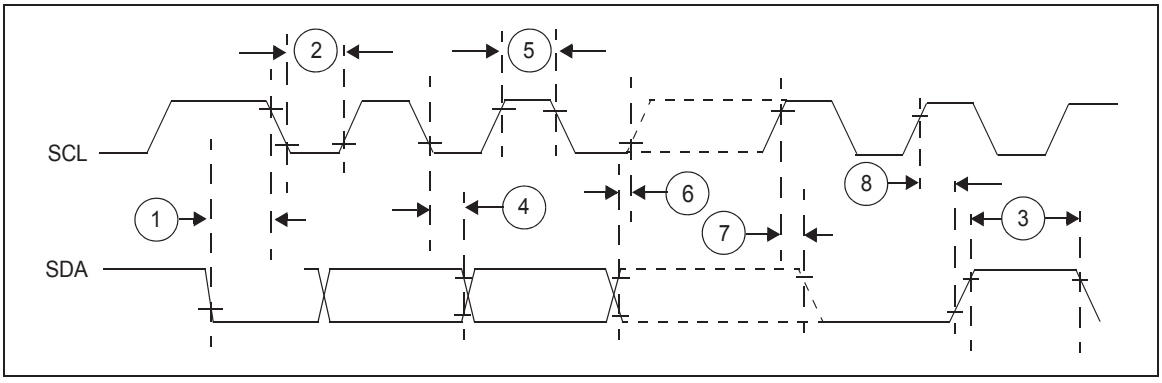


Table 80. Code Flash options (continued)

SPC58xE84 (6M)	SPC58xE80 (4M)	Partition	Start address	End address
64	64	0	0x00FE0000	0x00FEFFFF
64	64	0	0x00FF0000	0x00FFFFFF
128	128	0	0x01000000	0x0101FFFF
128	128	1	0x01020000	0x0103FFFF
256	256	0	0x01040000	0x0107FFFF
256	256	0	0x01080000	0x010BFFFF
256	256	0	0x010C0000	0x010FFFFF
256	256	0	0x01100000	0x0113FFFF
256	256	0	0x01140000	0x0117FFFF
256	256	0	0x01180000	0x011BFFFF
256	256	0	0x011C0000	0x011FFFFF
256	256	1	0x01200000	0x0123FFFF
256	256	1	0x01240000	0x0127FFFF
256	256	1	0x01280000	0x012BFFFF
256	256	1	0x012C0000	0x012FFFFF
256	256	1	0x01300000	0x0133FFFF
256	256	1	0x01340000	0x0137FFFF
256	256	1	0x01380000	0x013BFFFF
256	NA	5	0x013C0000	0x013FFFFF
256	NA	5	0x01400000	0x0143FFFF
256	NA	5	0x01440000	0x0147FFFF
256	NA	5	0x01480000	0x014BFFFF
256	NA	5	0x014C0000	0x014FFFFF
256	NA	5	0x01500000	0x0153FFFF
256	NA	5	0x01540000	0x0157FFFF
256	NA	5	0x01580000	0x015BFFFF

Table 81. RAM options(1)

SPC58NE84	SPC58EE84	SPC58NE80	SPC58EE80	Type	Start address	End address
768	768	768	768			
128	128	128	128	PRAMC_0	0x40060000	0x4007FFFF
160	160	160	160	PRAMC_1	0x40080000	0x400A7FFF
256	256	256	256	PRAMC_2 (STBY)	0x400A8000	0x400E7FFF
64	64	64	64	PRAMC_3	0x400E8000	0x400F7FFF

Table 81. RAM options[1] (continued)

SPC58NE84	SPC58EE84	SPC58NE80	SPC58EE80	Type	Start address	End address
768	768	768	768			
64	64	64	64	D_MEM CPU_0	0x50800000	0x5080FFFF
64	64	64	64	D_MEM CPU_1	0x51800000	0x5180FFFF
32	32	32	32	D_MEM CPU_2	0x52800000	0x52807FFF

1. RAM size is the sum of TCM and SRAM.

6 Revision history

Table 82. Document revision history

Date	Revision	Changes
10-Jun-2016	1	Initial release.
03-April-2017	2	Following are the changes for this release of the document: Editorial and formatting updates throughout the document. Updated the cover page. *Section 1.2: Description*: Replaced “SPC58NE84x” with “SPC58xEx”. *Table 2: SPC58xEx feature summary*:: Updated table. *Section 1.5: Features*: Updated the feature bullet points. *Section 2.1: Pad dimensions/ KGD coordinates*: Added this section. *Section 3.1: Introduction*: – Removed text “The IPs and...for the details”. – Removed the two notes. *Section 3.2: Absolute maximum ratings*: – Added text “Exposure to absolute ... reliability” – Added text “even momentarily” *Table 4: Absolute maximum ratings*: – Updated values in conditions column. – Added parameter T_{TRIN}. – For parameter “T_{STG}”, maximum value updated from “175” to “125” – Added new parameter “T_{PAS}” – For parameter “I_{INJ}”, description updated from “maximum...PAD” to “maximum DC...pad” *Table 5: Operating conditions*: – For parameter “V_{DD_LV}”, added footnote “In the range...” – For parameter “V_{DD_LV}”, changed the classification from “D” to “P” – For parameter “$V_{DD\_HV\_ADR\_S}$”, removed the second row. – For parameter $V_{DD\_HV\_ADR\_S}$-$V_{DD\_HV\_ADV}$, updated the min value. – Added footnote “The maximum number...” to parameter F_{SYS}. – For parameter “$V_{DD\_HV\_ADR\_S}$-$V_{DD\_HV\_ADV}$”, swapped the “conditions” and “Min” columns.

Table 82. Document revision history (continued)

Date	Revision	Changes
03-April-2017	2	*Section 3.17: Flash memory*: Updated the section. *Table 49: Nexus debug port timing*: Classification of parameters "t_{EVTIPW}" and "t_{EVTOPW}" changed from "P" to "D". *Table 55: DSPI CMOS master modified timing (full duplex and output only) — MTFE = 1, CPHA = 0 or 1*: Changed the Min value of t_{SCK} (very strong) from 33 to 59. *Table 56: DSPI LVDS master timing — full duplex — modified transfer format (MTFE = 1), CPHA = 0 or 1*: Added footnote "LVDS differential load considered is the capacitance on each terminal of the differential pair, as shown in *Figure 12*" to t_{SCK}. *Table 57: DSPI LVDS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock,*: Added footnote "LVDS differential load considered is the capacitance on each terminal of the differential pair, as shown in *Figure 12*" to t_{SCK}. *Table 53: DSPI channel frequency support*: Added column to show slower and faster frequencies. *Section 5: Ordering information*: Renamed figure "Ordering information scheme" to "Commercial product scheme" Added tables: *Table 80: Code Flash options*, and *Table 81: RAM options*

Table 82. Document revision history (continued)

Date	Revision	Changes
10-Oct-2017	3 (cont')	*Table 29: SDn ADC electrical specification*: – Added note "Propagation of the information..." to parameter $t_{LATENCY.}$ – For parameter $F_{rolloff}$ (Stop band attenuation, Modified bandwidth mode), updated all the conditions. *Table 31: LVDS pad startup and receiver electrical characteristics,*: – For parameter ILVDS_BIAS, changed the characteristics to "C" *Table 35: LFAST PLL electrical characteristics*: – Min and Max value of parameter "ERR_{REF}" updated from "TBD" to "-1" and "+1" respectively – Max value of parameter "PN" updated from "TBD" to "-58" – Frequency of parameter "ΔPER_{REF}" updated from "10MHz" to "20MHz". – Max value of parameter "ΔPER_{REF}" for condition "Single period" updated from "TBD" to "350" – Min and Max value of parameter "ΔPER_{REF}" for condition "Long period" updated from "TBD" to "-500" and "+500" respectively. *Figure 17: Voltage monitor threshold definition*: – Right blue line adjusted on the top figure *Table 38: External components integration*: – For parameter C_{S1_B}, replaced "HV supply" with "LV supply" in parameter description column. *Table 77: FPBGA292 package mechanical data*: – Updated the second table footnote. *Section 3.17: Flash memory*: – Updated the section. *Section 3.18.6: CAN timing*: – Added this section.