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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Tri-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA
Number of I/O	64
Program Memory Size	6MB (6M x 8)
Program Memory Type	FLASH
EEPROM Size	256K x 8
RAM Size	608K x 8
Voltage - Supply (Vcc/Vdd)	1.2V, 3.3V, 5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-eLQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc58ne84e7qmhar

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List of tables

- Eighteen LIN and UART communication interface (LINFlexD) modules
  - LINFlexD_0 is a Master/Slave
  - All others are Masters
- 8 MCAN interfaces with advanced shared memory scheme and ISO CAN-FD support, one supporting time-triggered controller area network (TTCAN)
- Dual-channel FlexRay controller
- Two ethernet controllers 10/100 Mbps, compliant IEEE 802.3-2008
  - IEEE 1588-2008 Time stamping (internal 64-bit time stamp)
  - IEEE 802.1AS and IEEE 802.1Qav (AVB-Feature)
  - IEEE 802.1Q VLAN tag detection
  - IPv4 and IPv6 checksum modules
- Flexible Power Supply options:
  - External Regulators (1.2V core, 3.3V–5V IO)
  - Single internal SMPS regulator (eLQFP176, KGD)
  - Single internal Linear Regulator with external ballast (FPBGA292, KGD)
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard.
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1)
- Standby power domain with smart wake-up sequence (LFBGA292, KGD)

3.2 Absolute maximum ratings

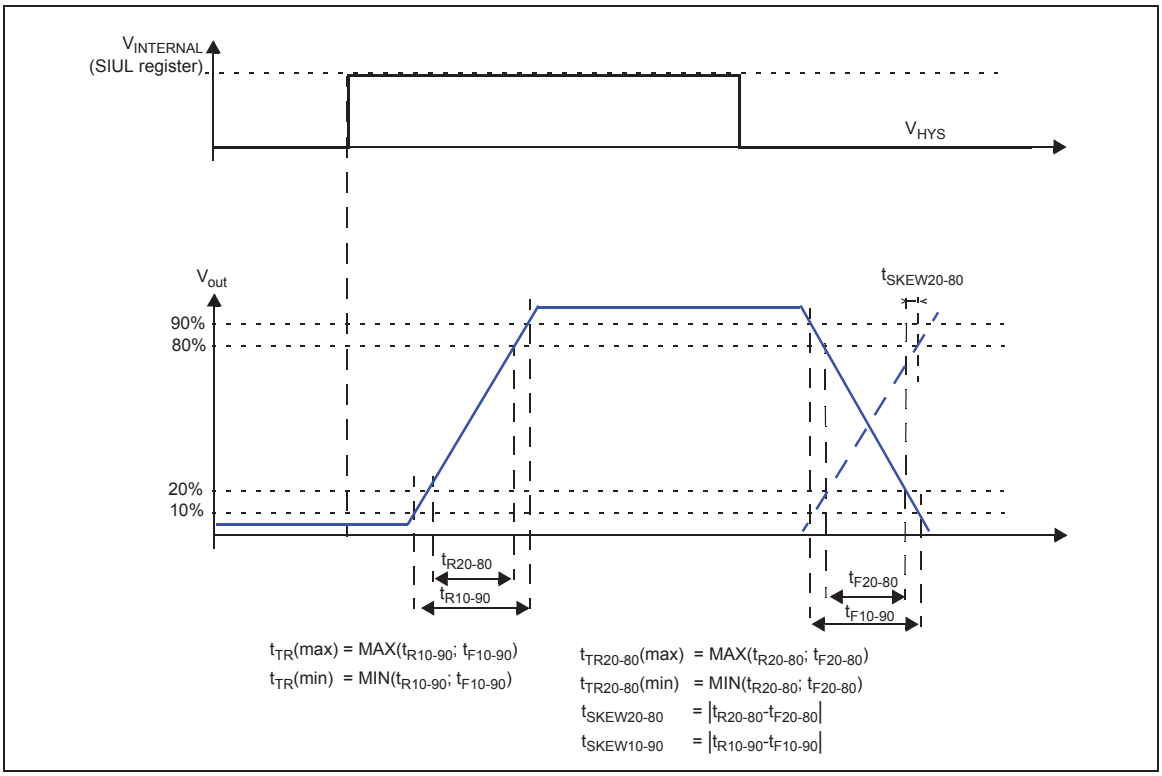
Table 4 describes the maximum ratings for the device. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Stress beyond the listed maxima, even momentarily, may affect device reliability or cause permanent damage to the device.

Table 4. Absolute maximum ratings

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{DD_LV}	SR	D	Core voltage operating life range(1)	—	–0.3	—	1.4	V
$V_{DD\_LV\_BD}$	SR	D	Buddy device voltage operating life range(2)	—	–0.3	—	1.5	V
$V_{DD\_HV\_IO\_MAIN}$ $V_{DD\_HV\_IO\_JTAG}$ $V_{DD\_HV\_IO\_FLEX}$ $V_{DD\_HV\_IO\_BD}$ $V_{DD\_HV\_FLA}$	SR	D	I/O supply voltage(3)	—	–0.3	—	6.0	V
$V_{SS\_HV\_ADV}$	SR	D	ADC ground voltage	Reference to digital ground	–0.3	—	0.3	V
$V_{DD\_HV\_ADV}$	SR	D	ADC Supply voltage	Reference to $V_{SS\_HV\_ADV}$	–0.3	—	6.0	V
$V_{SS\_HV\_ADR\_D}$	SR	D	SD ADC ground reference	—	–0.3	—	0.3	V
$V_{DD\_HV\_ADR\_D}$	SR	D	SD ADC voltage reference	Reference to $V_{SS\_HV\_ADR\_D}$	–0.3	—	6.0	V
V_{SS}-$V_{SS\_HV\_ADR\_D}$	SR	D	$V_{SS\_HV\_ADR\_D}$ differential voltage	—	–0.3	—	0.3	V
$V_{SS\_HV\_ADR\_S}$	SR	D	SAR ADC ground reference	—	–0.3	—	0.3	V
$V_{DD\_HV\_ADR\_S}$	SR	D	SAR ADC voltage reference	Reference to $V_{SS\_HV\_ADR\_S}$	–0.3	—	6.0	V
V_{SS}-$V_{SS\_HV\_ADR\_S}$	SR	D	$V_{SS\_HV\_ADR\_S}$ differential voltage	—	–0.3	—	0.3	V
V_{SS}-$V_{SS\_HV\_ADV}$	SR	D	$V_{SS\_HV\_ADV}$ differential voltage	—	–0.3	—	0.3	V

15. This specification is the maximum value and is a boundary for the dI specification.
16. Condition1: For power on period from 0 V up to normal operation with reset asserted. Condition 2: From reset asserted until PLL running free. Condition 3: Increasing PLL from free frequency to full frequency. Condition 4: reverse order for power down to 0 V.
17. I_{DDOFF} is the minimum guaranteed consumption of the device during power-up. It can be used to correctly size power-off ballast in case of current injection during power-off state.

Figure 4. I/O output DC electrical characteristics definition



The following tables provide DC characteristics for bidirectional pads:

- *Table 13* provides output driver characteristics for I/O pads when in WEAK/SLOW configuration.
- *Table 14* provides output driver characteristics for I/O pads when in MEDIUM configuration.
- *Table 15* provides output driver characteristics for I/O pads when in STRONG/FAST configuration.
- *Table 16* provides output driver characteristics for I/O pads when in VERY STRONG/VERY FAST configuration.

Note: 10%/90% is the default condition for any parameter if not explicitly mentioned differently.

Table 13. WEAK/SLOW I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ol_W}	CC	D	Output low voltage for Weak type PADs	I_{ol} = 0.5 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	0.1*V_{DD}	V
V_{oh_W}	CC	D	Output high voltage for Weak type PADs	Ioh = 0.5 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	0.9*V_{DD}	—	—	V

Table 13. WEAK/SLOW I/O output characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$R_{\_W}$	CC	P	Output impedance for Weak type PADs	V_{DD} = 5.0 V ± 10%	380	—	1040	Ω
				V_{DD} = 3.3 V ± 10%	250	—	700	
F_{max_W}	CC	T	Maximum output frequency for Weak type PADs	CL = 25 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	2	MHz
				CL = 50 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	1	MHz
t_{TR_W}	CC	T	Transition time output pin weak configuration, 10%-90%	CL = 25 pF V_{DD} = 5.0 V + 10% V_{DD} = 3.3 V + 10%	25	—	120	ns
				CL = 50 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	50	—	240	ns
$\lvert t_{SKEW\_W} \rvert$	CC	T	Difference between rise and fall time, 90%-10%	—	—	—	25	%
I_{DCMAX_W}	CC	D	Maximum DC current	V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	0.5	mA

Table 14. MEDIUM I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ol_M}	CC	D	Output low voltage for Medium type PADs	I_{ol} = 2.0 mA V_{DD} =5.0 V ± 10% V_{DD} =3.3 V ± 10%	—	—	0.1*V_{DD}	V
V_{oh_M}	CC	D	Output high voltage for Medium type PADs	I_{oh}=2.0 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	0.9*V_{DD}	—	—	V
$R_{\_M}$	CC	P	Output impedance for Medium type PADs	V_{DD} = 5.0 V ± 10%	90	—	260	Ω
				V_{DD} = 3.3 V ± 10%	60	—	170	

Figure 6. Noise filtering on reset signal

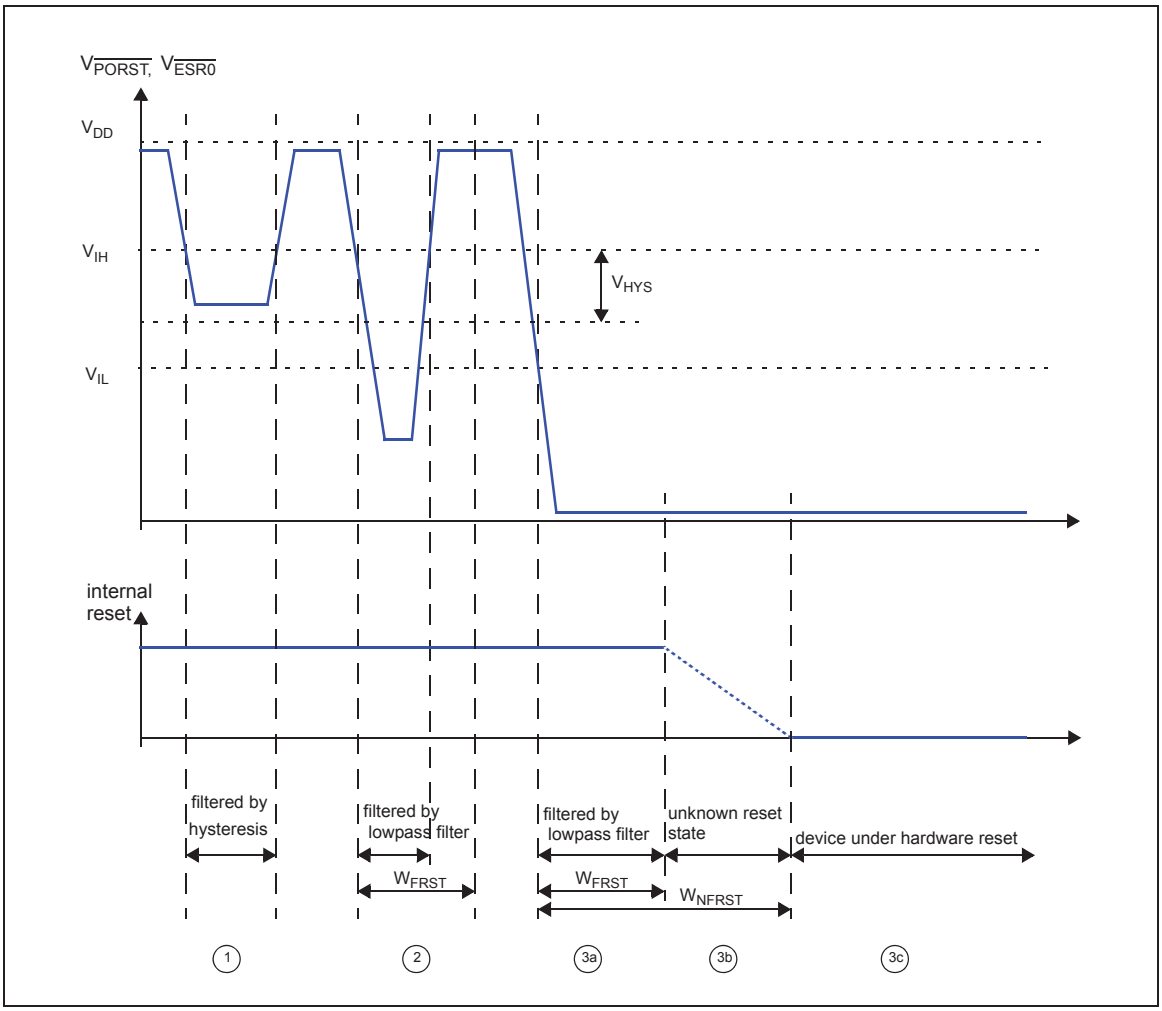


Table 18. Reset PAD electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IHRES}	SR	P	Input high level TTL	V_{DD_HV} = 5.0 V ± 10%	2	—	$V_{DD\_HV\_IO}$ +0.3	V
V_{ILRES}	SR	P	Input low level TTL	V_{DD_HV} = 5.0 V ± 10%	-0.3	—	0.8	V
V_{HYSRES}	CC	C	Input hysteresis TTL	V_{DD_HV} = 5.0 V ± 10%	0.3	—	—	V
V_{DD_POR}	CC	D	Minimum supply for strong pull-down activation	V_{DD_HV} = 5.0 V ± 10%	—	—	1.6	V

Table 20. PLL0 electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$\lvert\Delta_{PLL0PHI1SPJ}\rvert^{(3)}$	CC	T	PLL0_PHI1 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI1}$ = 40 MHz, 6-sigma	—	—	300(4)	ps
$\Delta_{PLL0LTJ}$(3)	CC	T	PLL0 output long term jitter(4) f_{PLL0IN} = 20 MHz (resonator), VCO frequency = 800 MHz	10 periods accumulated jitter (80 MHz equivalent frequency), 6-sigma pk-pk	—	—	±250	ps
				16 periods accumulated jitter (50 MHz equivalent frequency), 6-sigma pk-pk	—	—	±300	ps
				long term jitter (< 1 MHz equivalent frequency), 6-sigma pk-pk)	—	—	±500	ps
I_{PLL0}	CC	T	PLL0 consumption	FINE LOCK state	—	—	6	mA

1. PLL0IN clock retrieved directly from either internal RCOSC or external FXOSC clock. Input characteristics are granted when using internal RCOSC or external oscillator is used in functional mode.
2. If the PLL0_PHI1 is used as an input for PLL1, then the PLL0_PHI1 frequency shall obey the maximum input frequency limit set for PLL1 (87.5 MHz, according to *Table 21*).
3. Jitter values reported in this table refer to the internal jitter, and do not include the contribution of the divider and the path to the output CLKOUT pin.
4. V_{DD_LV} noise due to application in the range V_{DD_LV} = 1.20 V±5%, with frequency below PLL bandwidth (40 kHz) will be filtered.

Table 28. ADC-Comparator electrical specification(1) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
ΔTUE_{10}	CC	D	TUE degradation due to $V_{DD\_HV\_ADR}$ offset with respect to $V_{DD\_HV\_ADV}$	$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	–1.0	1.0	LSB (10b)
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–2.0	2.0	
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–3.5	3.5	
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–6.0	6.0	
				$V_{DD\_HV\_ADV} < V_{IN} <$ $V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	–2.5	2.5	
				$V_{DD\_HV\_ADV} < V_{IN} <$ $V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–4.0	4.0	
				$V_{DD\_HV\_ADV} < V_{IN} <$ $V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–7.0	7.0	
				$V_{DD\_HV\_ADV} < V_{IN} <$ $V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–12.0	12.0	
TUE_{INJ2}	CC	T	TUE degradation addition, due to current injection in I_{INJ2} range.(5)	See *Table 5: Operating conditions*, I_{INJ2} parameter.	3		LSB
DNL(6)	CC	P	Differential non-linearity std. mode	Standard frequency mode, $V_{DD\_HV\_ADV} > 4$ V $V_{DD\_HV\_ADR\_S} > 4$ V	–1	2	LSB (10b)
		T		High frequency mode, $V_{DD\_HV\_ADV} > 4$ V $V_{DD\_HV\_ADR\_S} > 4$ V	–1	2	

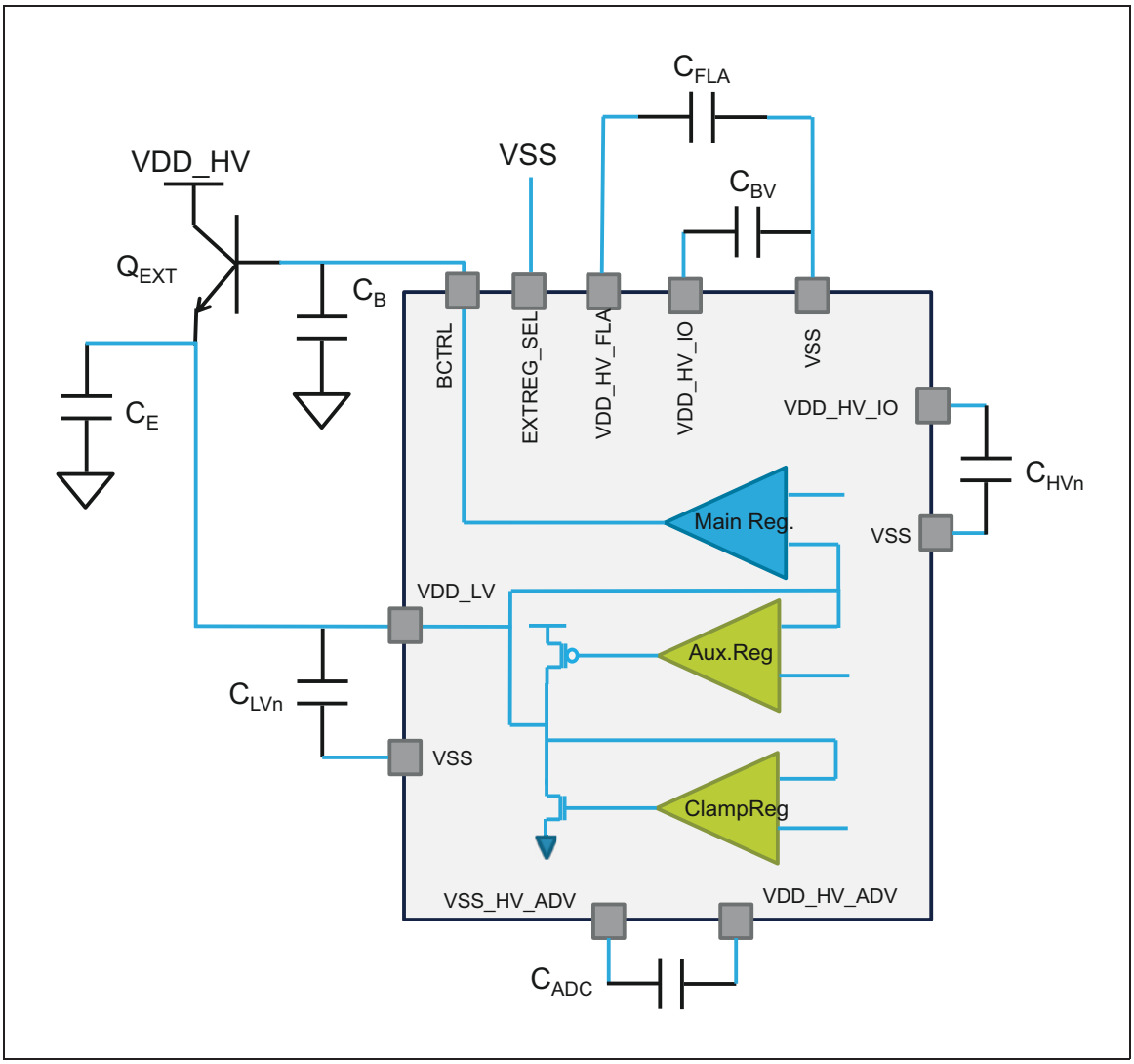
1. Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Minimum ADC sample times are dependent on adequate charge transfer from the external driving circuit to the internal sample capacitor. The time constant of the entire circuit must allow the sampling capacitor to charge within 1/2 LSB within the sampling window. Please refer to Figure 8 for models of the internal ADC circuit, and the values to use in external RC sizing and calculating the sampling window duration.

Table 35. LFAST PLL electrical characteristics[1] (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
DC_{REF}	CC	D	PLL reference clock duty cycle (CLKIN)	—	30	—	70	%
PN	CC	D	Integrated phase noise (single side band)	f_{RF_REF} = 20 MHz	—	—	-58	dBc
f_{VCO}	CC	P	PLL VCO frequency	—	312	—	320[3]	MHz
t_{LOCK}	CC	D	PLL phase lock	—	—	—	150[4]	µs
ΔPER_{REF}	SR	T	Input reference clock jitter (peak to peak)	Single period, f_{RF_REF} = 20 MHz	—	—	350	ps
		T		Long term, f_{RF_REF} = 20 MHz	-500	—	500	ps
ΔPER_{EYE}	CC	T	Output Eye Jitter (peak to peak)[5]	—	—	—	400	ps

1. The specifications in this table apply to both the interprocessor bus and debug LFAST interfaces.
2. If the input frequency is lower than 20 MHz, it is required to set a input division factor of 1.
3. The 320 MHz frequency is achieved with a 20 MHz reference clock.
4. The total lock time is the sum of the coarse lock time plus the programmable lock delay time 2 clock cycles of the peripheral bridge clock that is connected to the PLL on the device (to set the PLL enable bit).
5. Measured at the transmitter output across a 100 Ω termination resistor on a device evaluation board. See *Figure 12*.

Figure 14. Internal regulator with external ballast mode



3.18 AC Specifications

All AC timing specifications are valid up to 150 °C, except where explicitly noted.

3.18.1 Debug and calibration interface timing

3.18.1.1 JTAG interface timing

Table 48. JTAG pin AC electrical characteristics[1],[2]

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
1	t_{JCYC}	CC	D	TCK cycle time	100	—	ns
2	t_{JDC}	CC	T	TCK clock pulse width	40	60	%
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40%–70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	5	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	15[3]	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	15	ns
9	t_{JCMPPW}	CC	D	JCOMP assertion time	100	—	ns
10	t_{JCMPS}	CC	D	JCOMP setup time to TCK low	40	—	ns
11	t_{BSDV}	CC	D	TCK falling edge to output valid	—	600[4]	ns
12	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	600	ns
13	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	600	ns
14	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	15	—	ns
15	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only. See Table 49 for functional specifications.
2. JTAG timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 4.0 to 5.5 V and max. loading per pad type as specified in the I/O section of the datasheet.
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

3.18.1.3 Aurora LVDS interface timing

Table 50. Aurora LVDS interface timing specifications

Symbol		C	Parameter	Value			Unit
				Min	Typ	Max	
Data Rate							
—	SR	T	Data rate	—	—	1250	Mbps
STARTUP							
t_{STRT_BIAS}	CC	T	Bias startup time(1)	—	—	5	µs
t_{STRT_TX}	CC	T	Transmitter startup time(2)	—	—	5	µs
t_{STRT_RX}	CC	T	Receiver startup time(3)	—	—	4	µs

1. Startup time is defined as the time taken by LVDS current reference block for settling bias current after its pwr_down (power down) has been deasserted. LVDS functionality is guaranteed only after the startup time.
2. Startup time is defined as the time taken by LVDS transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.
3. Startup time is defined as the time taken by LVDS receiver for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.

3.18.1.4 Aurora debug port timing

Table 51. Aurora debug port timing

#	Symbol		C	Characteristic		Value		Unit
						Min	Max	
1	t_{REFCLK}	CC	T	Reference clock frequency		625	1250	MHz
1a	t_{MCYC}	CC	T	Reference clock rise/fall time		—	400	ps
2	t_{RCDC}	CC	D	Reference clock duty cycle		45	55	%
3	J_{RC}	CC	D	Reference clock jitter		—	40	ps
4	$t_{STABILITY}$	CC	D	Reference clock stability		50	—	PPM
5	BER	CC	D	Bit error rate		—	10^{-12}	—
6	J_D	SR	D	Transmit lane deterministic jitter		—	0.17	OUI
7	J_T	SR	D	Transmit lane total jitter		—	0.35	OUI
8	S_O	CC	T	Differential output skew		—	20	ps
9	S_{MO}	CC	T	Lane to lane output skew		—	1000	ps
10	OUI	CC	D	Aurora lane unit interval(1)	625 Mbps	1600	1600	ps
			D		1.25 Gbps	800	800	

1. ± +/-100 PPM

Table 58. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock[1],[2]

#	Symbol		C	Characteristic	Condition		Value[3]		Unit
					Pad drive[4]	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	33.0	—	ns
					Strong	50 pF	80.0	—	ns
					Medium	50 pF	200.0	—	ns
2	t_{CSV}	CC	D	PCS valid after SCK[5]	SCK and PCS drive strength				
					Very strong	25 pF	7	—	ns
					Strong	50 pF	8	—	ns
					Medium	50 pF	16	—	ns
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	29	—	ns
3	t_{CSH}	CC	D	PCS hold after SCK[5]	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	–14	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	–14	—	ns
					Medium	PCS = 0 pF SCK = 50 pF	–33	—	ns
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	–35	—	ns
4	t_{SDC}	CC	D	SCK duty cycle[6]	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Medium	0 pF	$^1/_2t_{SCK} - 5$	$^1/_2t_{SCK} + 5$	ns
SOUT data valid time (after SCK edge)									
9	t_{SUO}	CC	D	SOUT data valid time from SCK CPHA = 1[7]	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	8.0	ns
					Medium	50 pF	—	16.0	ns
SOUT data hold time (after SCK edge)									
10	t_{HO}	CC	D	SOUT data hold time after SCK CPHA = 1[7]	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	ns
					Medium	50 pF	–15.0	—	ns

3.18.4.2 TxD

Figure 48. TxD signal

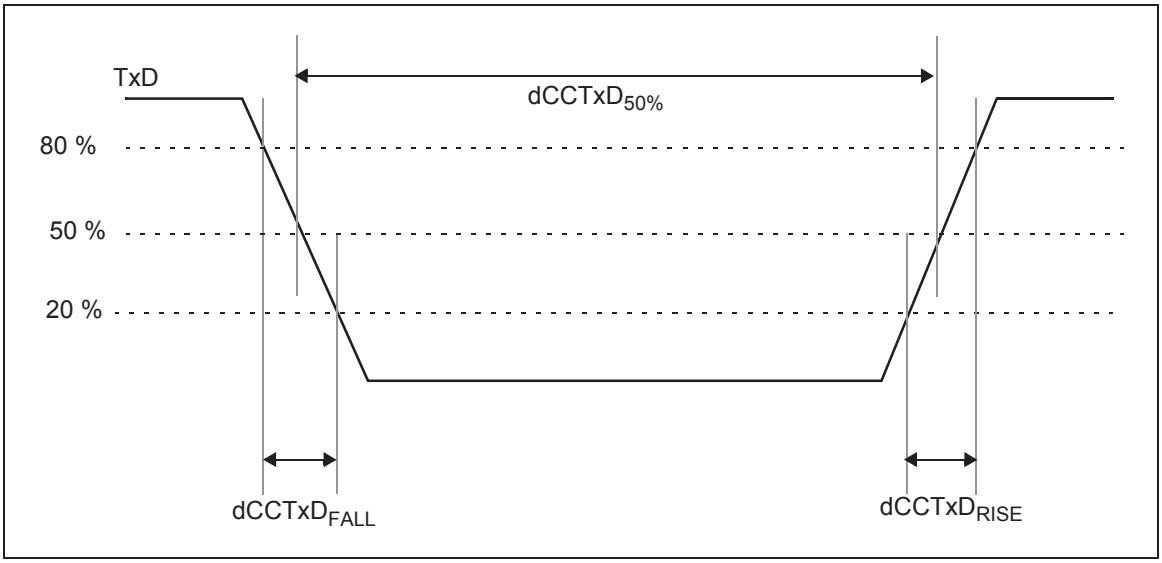


Table 68. TxD output characteristics(1),(2)

Symbol		C	Characteristic	Value		Unit
				Min	Max	
dCCTxAsym	CC	D	Asymmetry of sending CC at 25 pF load (= $dCCTxD_{50\%}$ – 100 ns)	–2.45	2.45	ns
$dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$	CC	D	Sum of Rise and Fall time of TxD signal at the output pin(3),(4)	—	9(5)	ns
		D		—	9(6)	
$dCCTxD_{01}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxD_{10}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. TxD pin load maximum 25 pF.
2. Specifications valid according to FlexRay EPL 3.0.1 standard with 20%–80% levels and a 10 pF load at the end of a 50 Ohm, 1 ns stripline. Please refer to the Very Strong I/O pad specifications.
3. Pad configured as VERY STRONG.
4. Sum of transition time simulation is performed according to Electrical Physical Layer Specification 3.0.1 and the entire temperature range of the device has been taken into account.
5. $V_{DD\_HV\_IO}$ = 5.0 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 1 ns, C_L = 10 pF.
6. $V_{DD\_HV\_IO}$ = 3.3 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 0.6 ns, C_L = 10 pF.

Table 70. PSI5 timing

Symbol		C	Parameter	Value		Unit
				Min	Max	
t_{MSG_DLY}	CC	D	Delay from last bit of frame (CRC0) to assertion of new message received interrupt	—	3	µs
t_{SYNC_DLY}	CC	D	Delay from internal sync pulse to sync pulse trigger at the SDOUT_PSI5_n pin	—	2	µs
t_{MSG_JIT}	CC	D	Delay jitter from last bit of frame (CRC0) to assertion of new message received interrupt	—	1	cycles(1)
t_{SYNC_JIT}	CC	D	Delay jitter from internal sync pulse to sync pulse trigger at the SDOUT_PSI5_n pin	—	+/-±(1 PSI5_1µs_CLK + 1 PBRIDGEn_CLK)	cycles

1. Measured in PSI5 clock cycles (PBRIDGEn_CLK on the device). Minimum PSI5 clock period is 20 ns.

3.18.6 CAN timing

The following table describes the CAN timing.

Table 71. CAN timing

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$t_{P(RX:TX)}$	CAN controller propagation delay time standard pads	Medium type pads 25pF load	—	—	70	ns
		Medium type pads 50pF load	—	—	80	
		STRONG, VERY STRONG type pads 25pFload	—	—	60	
		STRONG, VERY STRONG type pads 50pF load	—	—	65	
$t_{PLP(RX:TX)}$	CAN controller propagation delay time low power pads	Medium type pads 25pF load	—	—	90	ns
		Medium type pads 50pF load	—	—	100	
		STRONG, VERY STRONG type pads 25pF load	—	—	80	
		STRONG, VERY STRONG type pads 50pF load	—	—	85	

3.18.7 UART timing

UART channel frequency support is shown in the following table.

4.1 eLQFP176 package information

Figure 51. eLQFP176 package outline

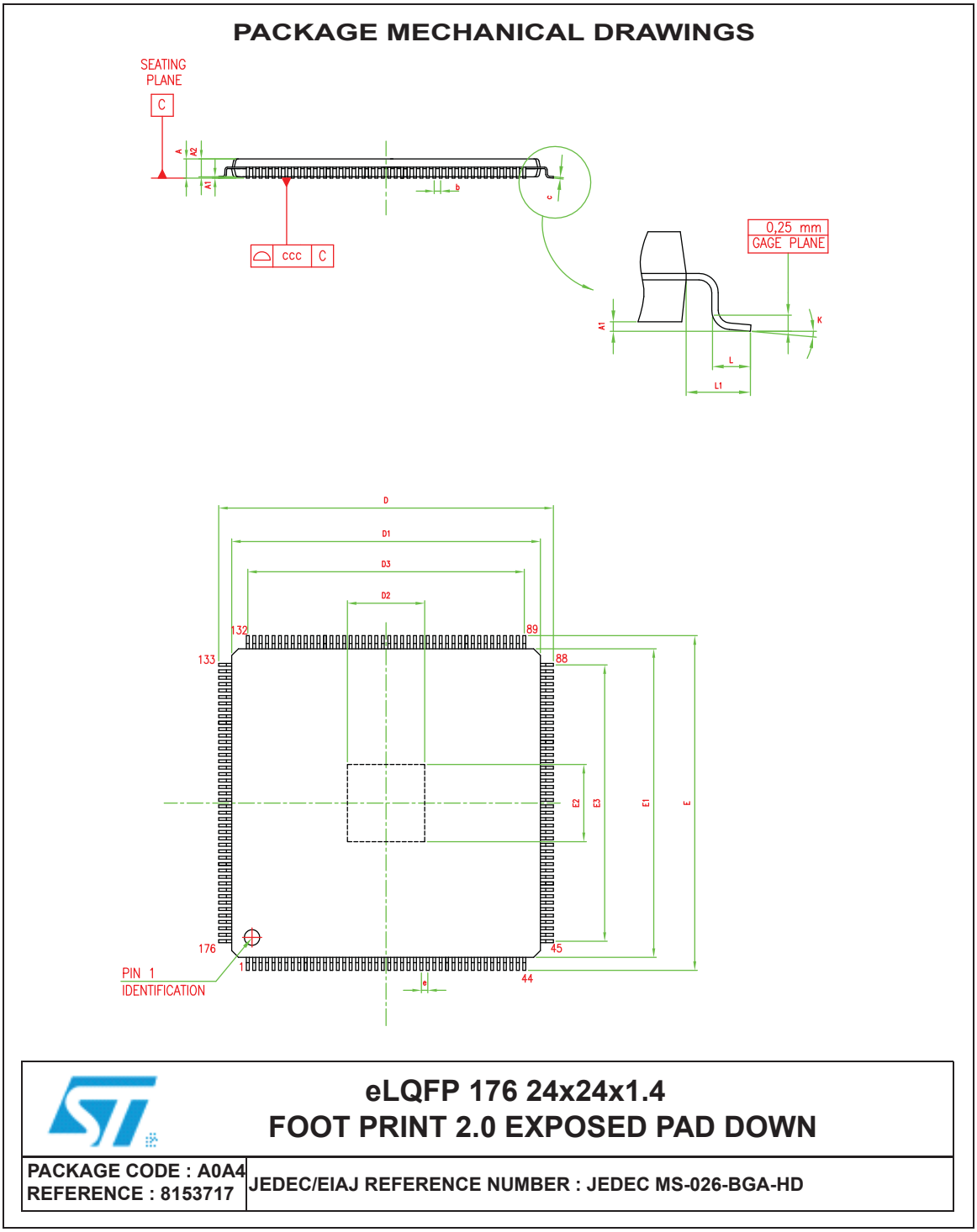


Table 82. Document revision history (continued)

Date	Revision	Changes
03-April-2017	2	*Table 28: ADC-Comparator electrical specification*: – Classification for parameter "$I_{ADCREFH}$" changed from "C" to "T" – Removed table footnote "Values are subject to change (possibly improved to ±2 LSB) after characterization" – For parameter f_{ADCK} , replaced the min value "7.5" with ">13.33" *Table 26: ADC pin specification,*: For I_{LKG}, changed condition "C" to "—". *Table 29: SDn ADC electrical specification*: – Added footnote "When using a GAIN ... resolution of 15 bits" to parameter "RESOLUTION". – Added footnote "Conversion offset ... offset error" to parameter V_{OFFSET}. – Removed footnote "SNR value guaranteed ... frequency range" from parameters- $SNR_{DIFF150}$ and $SNR_{DIFF333}$. – In V_{cmrr}, changed "SR" to "CC" and "D" to "T" – Changed min value from "1.5" to "—" in parameter "I_{ADV_D}" – Changed min value from "3" to "—" in parameter "ΣI_{ADR_D}". – Added footnote "Consumption is given ... set-up" to parameter "ΣI_{ADR_D}" – Removed footnote "Sampling is .... $f_{ADCD\_M}/2$" – Updated footnote "S/D ADC is ...12 dB" – Added table footnote "This parameter ...3 dB less" to parameters - $SNR_{DIFF150}$, $SNR_{DIFF333}$, and SNR_{SE150} – Replaced the max value of ΣI_{ADR_D} of "16" with "80". *Figure 8: Input equivalent circuit (Fast SARn and SARB channels)*: Updated the figure. *Table 30: Temperature sensor electrical characteristics*: For "temperature monitoring range", classification removed (was C) *Table 35: LFAST PLL electrical characteristics*: – Min and Max value of parameter "ERR_{REF}" updated from "TBD" to "-1" and "+1" respectively – Max value of parameter "PN" updated from "TBD" to "-58" – Frequency of parameter "ΔPER_{REF}" updated from "10MHz" to "20MHz". – Max value of parameter "ΔPER_{REF}" for condition "Single period" updated from "TBD" to "350" – Min and Max value of parameter "ΔPER_{REF}" for condition "Long period" updated from "TBD" to "-500" and "+500" respectively. *Table 36: Aurora LVDS electrical characteristics,*: – For parameter $\lvert\Delta V_{I\_L}\rvert$, changed classification to "T" – For parameter $\lvert\Delta V_{OD\_LVDS}\rvert$, changed the classification to "T".