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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Tri-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA
Number of I/O	64
Program Memory Size	6MB (6M x 8)
Program Memory Type	FLASH
EEPROM Size	256K x 8
RAM Size	608K x 8
Voltage - Supply (Vcc/Vdd)	1.2V, 3.3V, 5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-eLQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc58ne84e7qmhay

Figure 2. Periphery allocation

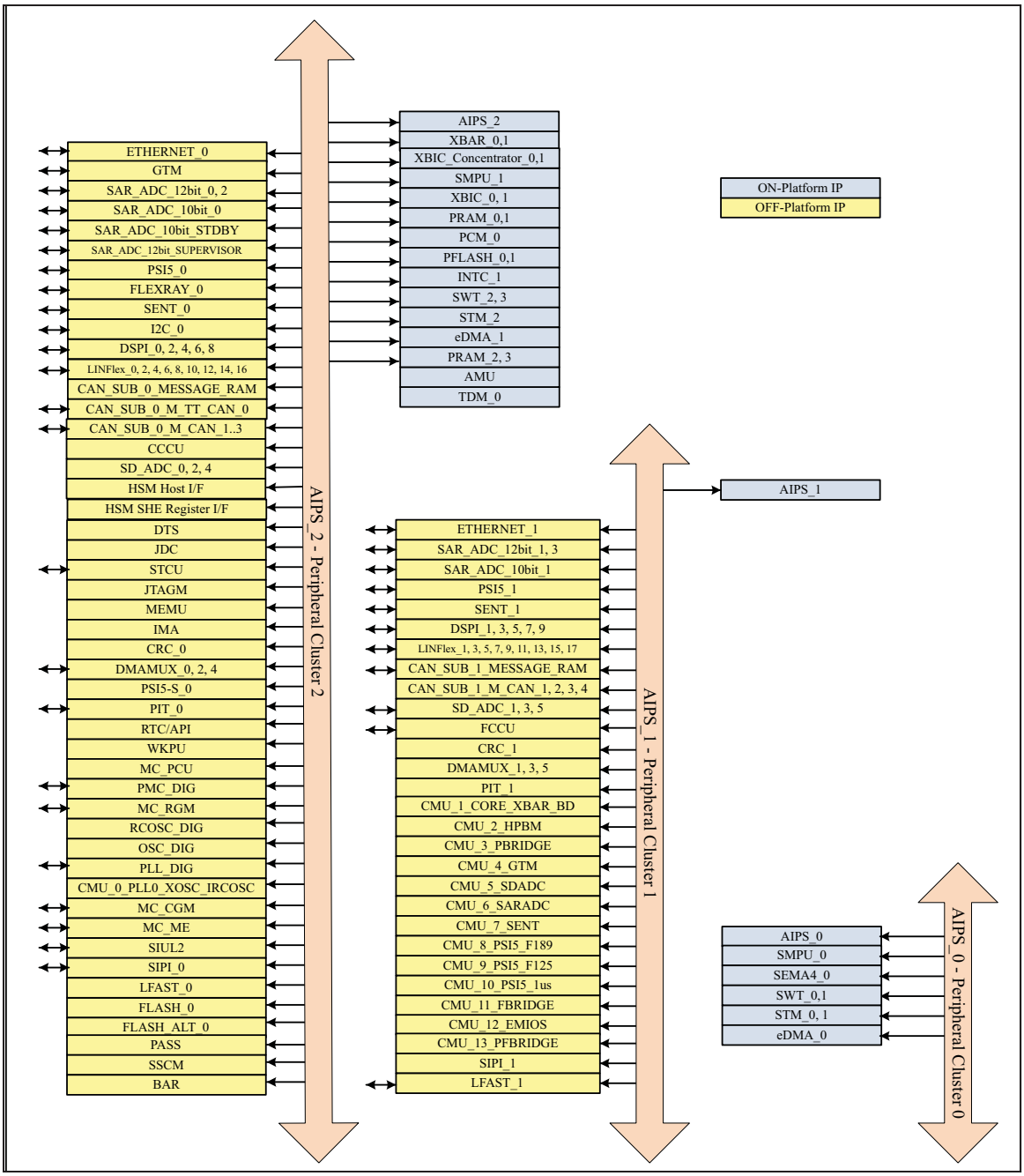


Table 4. Absolute maximum ratings (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IN}	SR	D	I/O input voltage range(4) (5)	—	–0.3	—	6.0	V
				Relative to V_{ss}	–0.3	—	—	
				Relative to $V_{DD\_HV\_IO}$ and $V_{DD\_HV\_ADV}$	—	—	0.3	
T_{TRIN}	SR	D	Digital Input pad transition time(6)	—	—	—	1	ms
I_{INJ}	SR	T	Maximum DC injection current for each analog/digital PAD(7)	—	–5	—	5	mA
T_{STG}	SR	T	Maximum non-operating Storage temperature range	—	–55	—	125	°C
T_{PAS}	SR	C	Maximum nonoperating temperature during passive lifetime	—	–55	—	150(8)	°C
$T_{STORAGE}$	SR	—	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range –40 °C to 60 °C	—	—	20	years
T_{SDR}	SR	T	Maximum solder temperature Pb-free packaged(9)	—	—	—	260	°C
MSL	SR	T	Moisture sensitivity level(10)	—	—	—	3	—
T_{XRAY} dose	SR	T	Maximum cumulated XRAY dose	Typical range for X-rays source during inspection:80 ÷ 130 KV; 20 ÷ 50 µA	—	—	1	grey

1. V_{DD_LV}: allowed 1.335 V - 1.400 V for 60 seconds cumulative time at the given temperature profile. Remaining time allowed 1.260 V - 1.335 V for 10 hours cumulative time at the given temperature profile. Remaining time as defined in *Section 3.3: Operating conditions*. In the range [1.26-1.33] V and if the above-mentioned cumulative times are not exceeded, the device functionality is granted and is expected to receive a flag by the internal HVD134 monitors to warn that the regulator (internal or external), providing the VDD_LV supply, exited the expected operating conditions. If the internal HVD134 monitors are disabled by the application, then an external voltage monitor with equivalent thresholds measured at the device pad, has to be implemented. Please refer to *Section 3.16.3: Voltage monitors* for the list of available internal monitors and to the Reference Manual for the configurability of the monitors. In this range, the device may exceed the maximum consumptions reported in *Table 9: Device consumption*.
2. $V_{DD\_LV\_BD}$: allowed 1.450 V - 1.500 V for 60 seconds cumulative time at the given temperature profile. Remaining time allowed 1.375 V - 1.450 V for 10 hours cumulative time at maximum T_J = 125 °C. Remaining time as defined in *Section 3.3: Operating conditions*.
3. V_{DD_HV}: allowed 5.5 V–6.0 V for 60 seconds cumulative time at the given temperature profile, for 10 hours cumulative time with the device in reset at the given temperature profile. Remaining time as defined in *Section 3.3: Operating conditions*.
4. The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage will be equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3 V can be used for nominal calculations.
5. Relative value can be exceeded if design measures are taken to ensure injection current limitation (parameter IINJ).
6. This limitation applies to pads with digital input buffer enabled. If the digital input buffer is disabled, there are no maximum limits to the transition time.
7. The limits for the sum of all normal and injected currents on all pads within the same supply segment can be found in *Section 3.8.3: I/O pad current specifications*.
8. 175°C are allowed for limited time. Mission profile with passive lifetime temperature >150°C have to be evaluated by ST to confirm that are granted by product qualification.
9. Solder profile per IPC/JEDEC J-STD-020D.
10. Moisture sensitivity per JDEC test method A112.

Table 5. Operating conditions (continued)

Symbol		C	Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
$V_{SS\_HV\_ADR\_D}$-$V_{SS\_HV\_ADV}$	SR	D	$V_{SS\_HV\_ADR\_D}$ differential voltage	—	–25	—	25	mV
$V_{DD\_HV\_ADR\_S}$	SR	P	SAR ADC reference voltage	—	3.0	—	5.5	V
$V_{DD\_HV\_ADR\_S}$-$V_{DD\_HV\_ADV}$	SR	D	SAR ADC reference differential voltage	—	$V_{DD\_HV\_ADV}$ -10%	—	25	mV
$V_{SS\_HV\_ADR\_S}$	SR	P	SAR ADC ground reference voltage	—	$V_{SS\_HV\_ADV}$			V
$V_{SS\_HV\_ADR\_S}$-$V_{SS\_HV\_ADV}$	SR	D	$V_{SS\_HV\_ADR\_S}$ differential voltage	—	–25	—	25	mV
V_{RAMP_LV}	SR	D	Slew rate on core power supply pins	V_{DD_LV} $V_{DD\_LV\_BD}$	—	—	20	V/ms
V_{RAMP_HV}	SR	D	Slew rate on HV power supply	—	—	—	100	V/ms
V_{IN}	SR	P	I/O input voltage range	—	0	—	5.5	V
I_{INJ1}	SR	T	DC Injection current (per pin) without performance degradation(8) (9) (10)	Digital pins and analog pins	–3.0	—	3.0	mA
I_{INJ2}	SR	D	Dynamic Injection current (per pin) with performance degradation(10) (11)	Digital pins and analog pins	–10	—	10	mA

1. The ranges in this table are design targets and actual data may vary in the given range.
2. The maximum number of PRAM wait states has to be configured according to the system clock frequency. Refer to *Table 6*.
3. Core voltage as measured on device pin to guarantee published silicon performance.
4. In the range [1.14-1.08]V, the device functionality and specifications are granted and the device is expected to receive a flag by the internal LVD100 monitors to warn that the regulator (internal or external), providing the V_{DD_LV} supply, exited the expected operating conditions. If the internal LVD100 monitors are disabled by the application, then an external voltage monitor with minimum threshold of V_{DD_LV}(min) = 1.08 V measured at the device pad, has to be implemented. Please refer to *Section 3.16.3: Voltage monitors* for the list of available internal monitors and to the Reference Manual for the configurability of the monitors.

5. Core voltage can exceed 1.26 V with the limitations provided in *Section 3.2: Absolute maximum ratings*, provided that HVD134_C monitor reset is disabled.
6. 1.260 V - 1.290 V range allowed periodically for supply with sinusoidal shape and average supply value below or equal to 1.236 V at the given temperature profile.
7. S/D ADC is functional in the range 3.0 V < $V_{DD\_HV\_ADV}$ < 4.0 V and 3.0 V < $V_{DD\_HV\_ADR\_D}$ < 4.0 V, but precision of conversion is not guaranteed.
8. Full device lifetime. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See *Section 3.2: Absolute maximum ratings* for maximum input current for reliability requirements.
9. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pins is above the supply rail, current will be injected through the clamp diode to the supply rails. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
10. The limits for the sum of all normal and injected currents on all pads within the same supply segment can be found in *Section 3.8.3: I/O pad current specifications*.
11. Positive and negative Dynamic current injection pulses are allowed up to this limit, with different specifications for I/O, ADC accuracy and analog input. See the dedicated chapters for the different specification limits. See the Absolute Maximum Ratings table for maximum input current for reliability requirements. Refer to the following pulses definitions: Pulse1 (ISO 7637-2:2011), Pulse 2a(ISO 7637-2:2011 5.6.2), Pulse 3a (ISO 7637-2:2011 5.6.3), Pulse 3b (ISO 7637-2:2011 5.6.3).

Table 6. PRAM wait states configuration

PRAMC WS	Clock Frequency (MHz)
1	≤ 180
0	≤ 120

3.3.1 Power domains and power up/down sequencing

The following table shows the constraints and relationships for the different power domains. Supply1 (on rows) can exceed Supply2 (on columns), only if the cell at the given row and column is reporting ‘ok’. This limitation is valid during power-up and power-down phases, as well as during normal device operation.

Figure 14. Internal regulator with external ballast mode

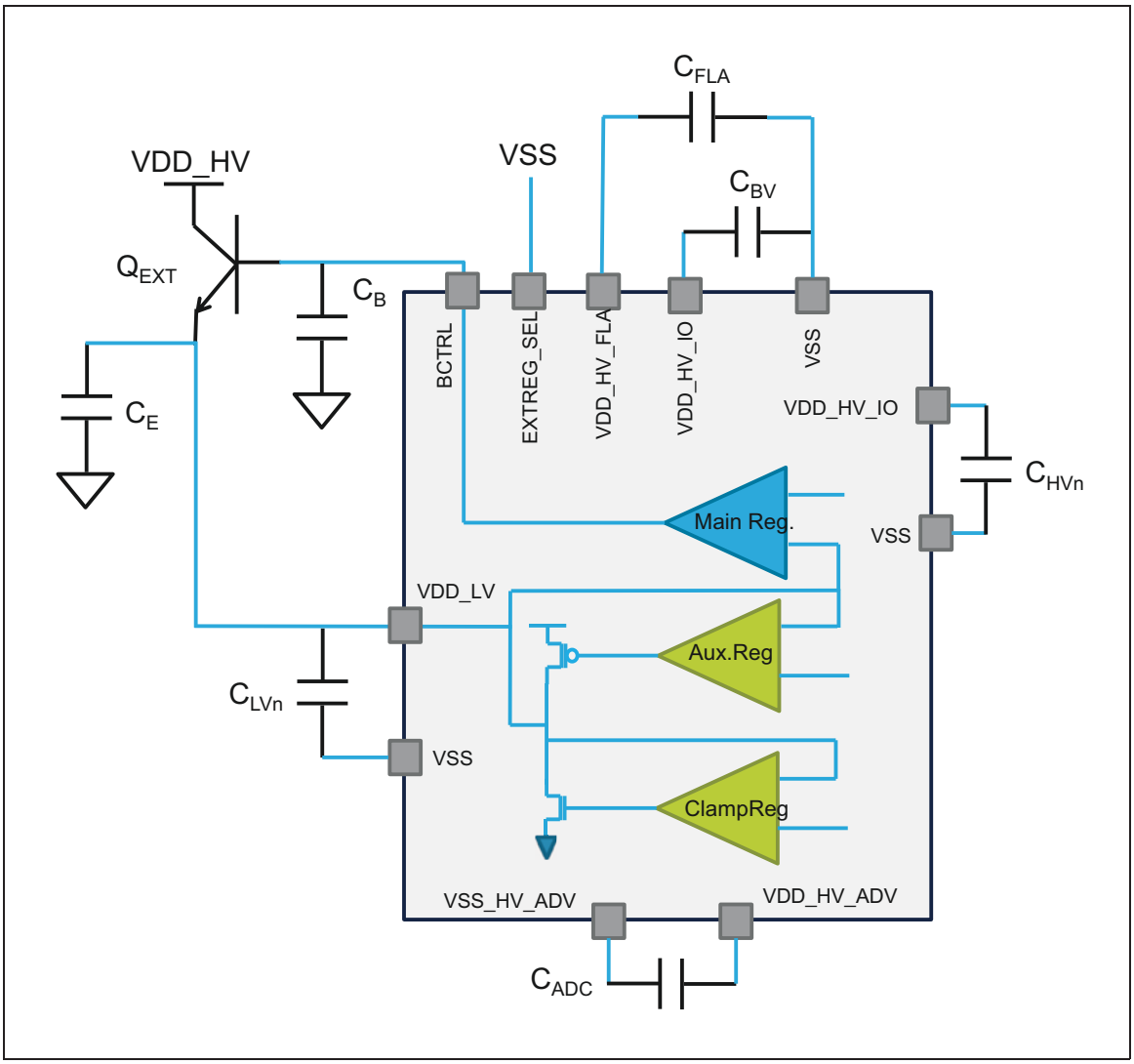


Table 38. External components integration (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
R_{LVn}	SR	D	Stability capacitor equivalent serial resistance	—	—	—	50	mΩ
C_{BV}	SR	D	Bulk capacitance for HV supply[2]	—	—	4.7	—	µF
C_{HVn}	SR	D	Decoupling capacitance for ballast and IOs[2]	on all $V_{DD\_HV\_IO}/V_{SS}$ and $V_{DD\_HV\_ADR}/V_{SS}$ pairs	—	100	—	nF
C_{FLA}	SR	D	Decoupling capacitance for flash supply[6]	—	—	10	—	nF
C_{ADC}	SR	D	ADC supply external capacitance[2]	$V_{DD\_HV\_ADV}/V_{SS\_HV\_ADV}$ pair.	—	2.2	—	µF
Internal Linear Regulator with External Ballast Mode								
Q_{EXT}	SR	D	Recommended external NPN transistors	NJD2873T4, BCP68				
V_Q	SR	D	External NPN transistor collector voltage	—	2.0	—	$V_{DD\_HV\_IO\_MAIN}$	V
C_B	SR	D	Internal voltage regulator stability external capacitance on ballast base[5] [7]	—	—	2.2	—	µF
R_B	SR	D	Stability capacitor equivalent serial resistance	Total resistance including board track	—	—	50	mΩ
SMPS Regulator Mode								
Common Configuration[8]								
PMOS	SR	D	Recommended PMOS transistor for SMPS mode	PMPB100XPEA				
NMOS	SR	D	Recommended NMOS transistor for SMPS mode	PMPB55XNEA				
C_{S2}	SR	D	SMPS External capacitance on HV supply[2]	—	-50%	47[9]	+35	µF
Option A								
C_{S1_A}	SR	D	SMPS External capacitance on LV supply[2]	—	-50%	2x10	+35	µF
L_{S_A}	SR	D	SMPS External inductance	—	-30%	10	+30%	µH
Option B								
C_{S1_B}	SR	D	SMPS External capacitance on LV supply[10]	—	-35%	3x10	+35%	µF
L_{S_B}	SR	D	SMPS External inductance	—	-30%	4.7	+30%	µH

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_J = –40 / 165 °C, unless otherwise specified.
2. Recommended X7R or X5R ceramic –50% / +35% variation across process, temperature, voltage and after aging.
3. CE capacitance is required both in internal and external regulator mode.
4. For noise filtering, add a high frequency bypass capacitance of 10 nF.

5. For BGA and KGD applications it is recommended to implement at least 5 C_{LV} capacitances.
6. Recommended X7R capacitors. For noise filtering, add a high frequency bypass capacitance of 100 nF.
7. CB capacitance is required if only the external ballast is implemented.
8. The application has to implement one of the two recommended combinations of external components for the SMPS regulator:
   PMOS, NMOS and CS2 (common), plus CS1_A and LS_A (option A), or
   PMOS, NMOS and CS2 (common), plus CS1_B and LS_B (option B).
9. The value of the capacitance on the HV supply reported in the datasheet is a general recommendation. The application can select a different number, based on the external regulator and emc requirements.
10. Recommended X7R or X5R ceramic –35% / +35% variation across process, temperature, voltage and after aging.

3.16.3 Voltage monitors

The monitors and their associated levels for the device are given in Table 44. Figure 17 illustrates the workings of voltage monitoring threshold.

Figure 17. Voltage monitor threshold definition

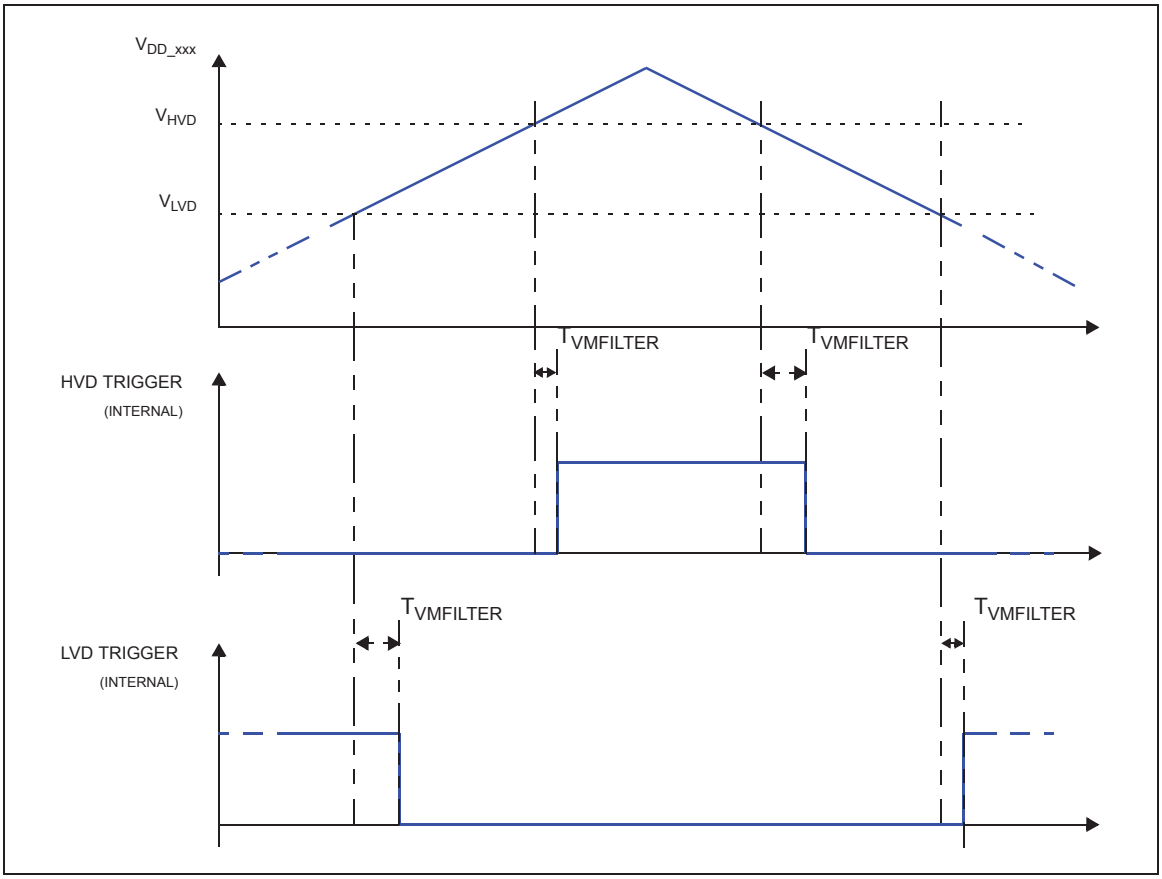


Table 44. Voltage monitor electrical characteristics

Symbol	C		Supply/Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
PowerOn Reset HV								
V_{POR200_C}	CC	P	$V_{DD\_HV\_IO\_MAIN}$	—	1.80	2.18	2.40	V
Minimum Voltage Detectors HV								
V_{MVD270_C}	CC	P	$V_{DD\_HV\_IO\_MAIN}$	—	2.71	2.76	2.80	V
V_{MVD270_F}	CC	P	$V_{DD\_HV\_FLA}$	—	2.71	2.76	2.80	V
V_{MVD270_SBY}	CC	P	$V_{DD\_HV\_IO\_MAIN}$ (in Standby)	—	2.71	2.76	2.80	V
Low Voltage Detectors HV								
V_{LVD290_C}	CC	P	$V_{DD\_HV\_IO\_MAIN}$	—	2.89	2.94	2.99	V

Table 46. Flash memory program and erase specifications (continued)

Symbol	Characteristics[1][2]	Value									Unit
		Typ[3]	C	Initial max			Typical end of life[4]	Lifetime max[5]		C	
				25 °C [6]	All temp [7]	C		< 1 K cycles	≤ 250 K cycles		
t_{AMRT}	Array Integrity Check - Margin Read suspend request rate	15	T	—	—	—	—	—		—	µs
t_{PSUS}	Program suspend latency[11]	—	—	—	—	—	—	12		T	µs
t_{ESUS}	Erase suspend latency[11]	—	—	—	—	—	—	22		T	µs
t_{AIC0S}	Array Integrity Check (6.0 MB, sequential)[12]	40	T	—	—	—	—	—	—	—	ms
$t_{AIC256KS}$	Array Integrity Check (256 KB, sequential)[12]	1.5	T	—	—	—	—	—	—	—	ms
t_{AIC0P}	Array Integrity Check (6.0 MB, proprietary)[12]	4.0	T	—	—	—	—	—	—	—	s
t_{MR0S}	Margin Read (6.0 MB, sequential)[12]	120	T	—	—	—	—	—	—	—	ms
$t_{MR256KS}$	Margin Read (256 KB, sequential)[12]	4.0	T	—	—	—	—	—	—	—	ms

1. Characteristics are valid both for Data Flash and Code Flash, unless specified in the characteristics column.
2. Actual hardware operation times; this does not include software overhead.
3. Typical program and erase times assume nominal supply values and operation at 25 °C.
4. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations. These values are characteristic, but not tested.
5. Lifetime maximum program & erase times apply across the voltages and temperatures and occur after the specified number of program/erase cycles. These maximum values are characterized but not tested or guaranteed.
6. Initial factory condition: < 100 program/erase cycles, 25 °C typical junction temperature and nominal (± 5%) supply voltages.
7. Initial maximum “All temp” program and erase times provide guidance for time-out limits used in the factory and apply for less than or equal to 100 program or erase cycles, –40 °C < TJ < 150 °C junction temperature and nominal (± 5%) supply voltages.
8. Rate computed based on 256 KB sectors.
9. Only code sectors, not including EEPROM.
10. Time between suspend resume and next suspend. Value stated actually represents Min value specification.
11. Timings guaranteed by design.
12. AIC is done using system clock, thus all timing is dependant on system frequency and number of wait states. Timing in the table is calculated at max frequency.

All the Flash operations require the presence of the system clock for internal synchronization. About 50 synchronization cycles are needed: this means that the timings of the previous table can be longer if a low frequency system clock is used.

Figure 23. Nexus event trigger and test clock timings

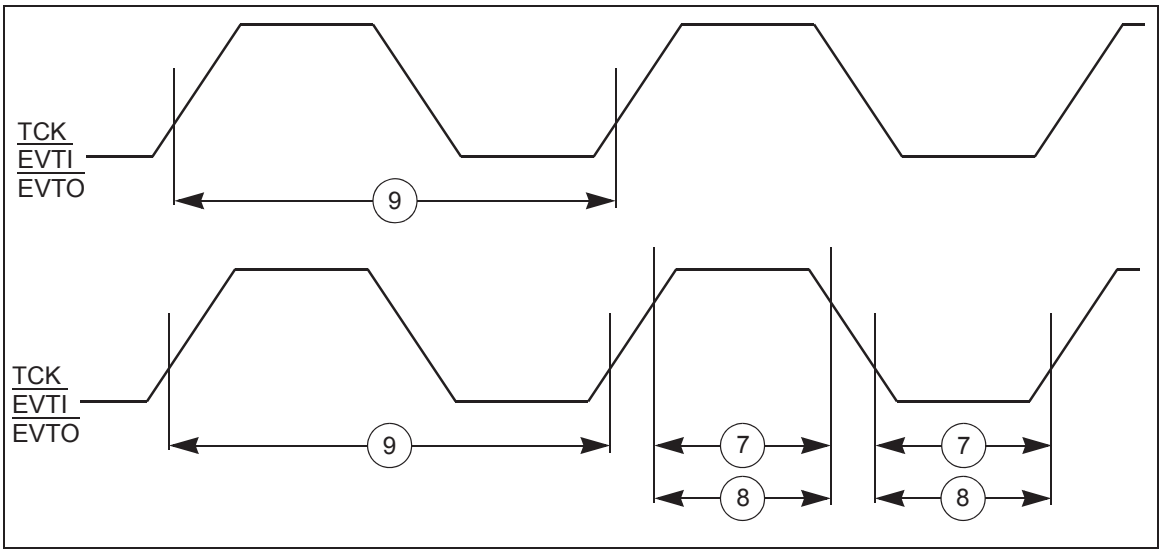


Figure 24. Nexus TDI, TMS, TDO timing

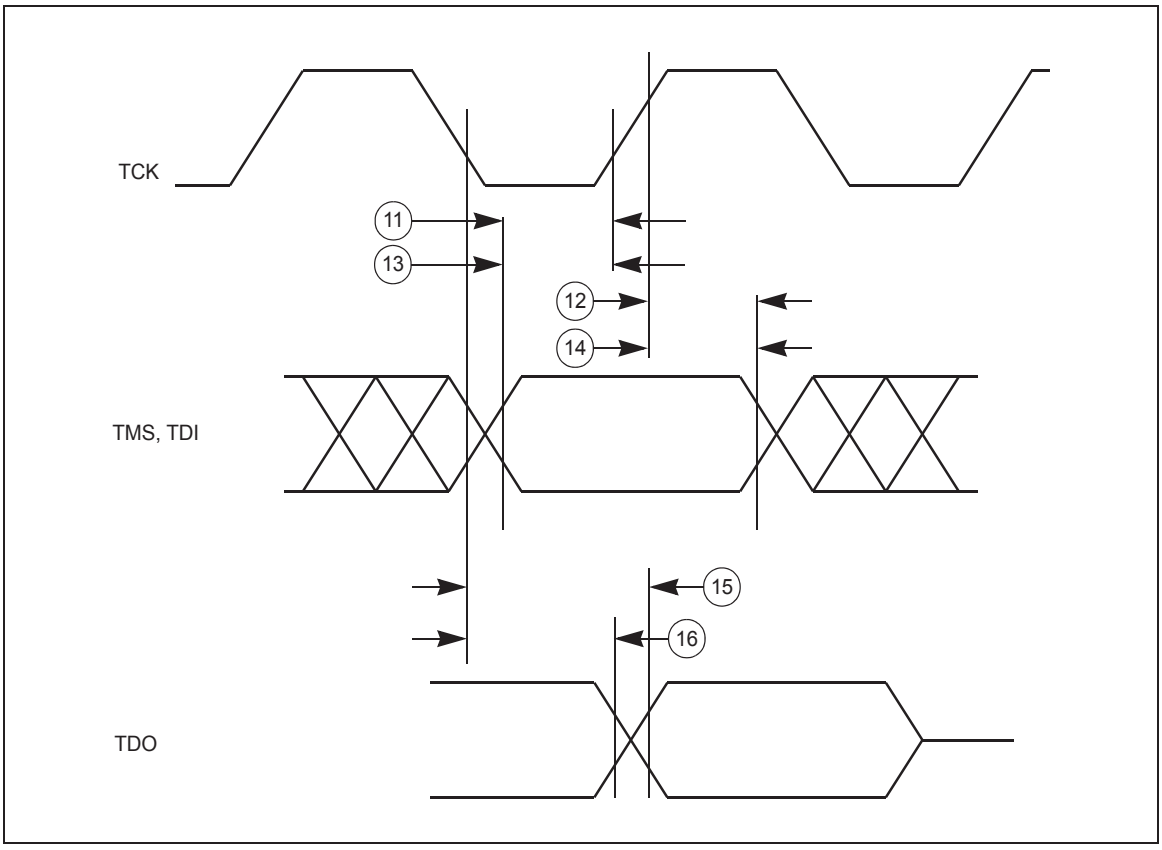


Table 53. DSPI channel frequency support[1]

DSPI use mode			Max usable frequency (MHz)[2],[3]
CMOS (Master mode)	Full duplex – Classic timing (Table 54)	DSPI_0, DSPI_3, DSPI_5, DSPI_7	12
		DSPI_8	5
		DSPI_1, DSPI_2, DSPI_4, DSPI_6, DSPI_9	17
	Full duplex – Modified timing (Table 55)	DSPI_0, DSPI_3, DSPI_5, DSPI_7	12
		DSPI_8	5
		DSPI_1, DSPI_2, DSPI_4, DSPI_6, DSPI_9	30
	Output only mode (SCK/SOUT/PCS) (Table 54 and Table 55)	—	30
	Output only mode TSB mode (SCK/SOUT/PCS)	—	30
LVDS (Master mode)	Full duplex – Modified timing (Table 56)	—	33
	Output only mode TSB mode (SCK/SOUT/PCS) (Table 57)	—	40
CMOS (Slave mode Full duplex) (Table 59)		—	16

1. Each DSPI module can be configured to use different pins for the interface. Please see the device pin out IO definition excel file, for the available combinations. It is not possible to reach the maximum performance with every possible combination of pins.
2. Maximum usable frequency can be achieved if used with fastest configuration of the highest drive pads.
3. Maximum usable frequency does not take into account external device propagation delay.

3.18.2.1 DSPI master mode full duplex timing with CMOS and LVDS pads

3.18.2.1.1 DSPI CMOS master mode — classic timing

Table 54. DSPI CMOS master classic timing (full duplex and output only) — MTFE = 0, CPHA = 0 or 1[1]

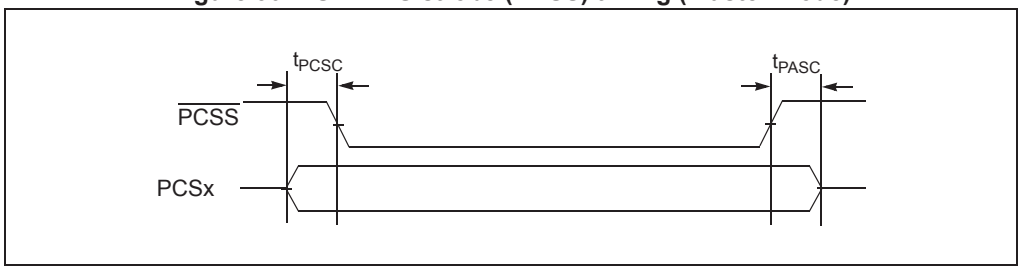
#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	59.0	—	ns
					Strong	50 pF	80.0	—	
					Medium	50 pF	200.0	—	

Table 54. DSPI CMOS master classic timing (full duplex and output only) — MTFE = 0, CPHA = 0 or 1[1] (continued)

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
8	t_{HI}	CC	D	SIN hold time from SCK[9]	SCK drive strength				
					Very strong	0 pF	–1.0	—	ns
					Strong	0 pF	–1.0	—	
					Medium	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)									
9	t_{SUO}	CC	D	SOUT data valid time from SCK[10]	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	8.0	
					Medium	50 pF	—	16.0	
SOUT data hold time (after SCK edge)									
10	t_{HO}	CC	D	SOUT data hold time after SCK[10]	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	
					Medium	50 pF	–15.0	—	

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. All timing values for output signals in this table are measured to 50% of the output voltage.
3. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
4. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
5. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
6. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
7. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
8. PCSx and PCSS using same pad configuration.
9. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
10. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances have the same value.

Figure 30. DSPI PCS strobe ($\overline{PCSS}$) timing (master mode)



3.18.2.1.2 DSPI CMOS master mode — modified timing

Table 55. DSPI CMOS master modified timing (full duplex and output only) — MTFE = 1, CPHA = 0 or 1(1)

#	Symbol		C	Characteristic	Condition		Value(2)		Unit
					Pad drive(3)	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	33.0	—	ns
					Strong	50 pF	80.0	—	
					Medium	50 pF	200.0	—	
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	ns
					Strong	50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	
					Medium	50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 29$	—	
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
					Medium	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
4	t_{SDC}	CC	D	SCK duty cycle(7)	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	
					Medium	0 pF	$^1/_2t_{SCK} - 5$	$^1/_2t_{SCK} + 5$	

Table 55. DSPI CMOS master modified timing (full duplex and output only) — MTFE = 1, CPHA = 0 or 1[1] (continued)

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
9	t_{SUO}	CC	D	SOUT data valid time from SCK CPHA = 0[10]	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0 + t_{SYS}[5]	ns
					Strong	50 pF	—	8.0 + t_{SYS}[5]	
					Medium	50 pF	—	16.0 + t_{SYS}[5]	
				SOUT data valid time from SCK CPHA = 1[10]	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	8.0	
					Medium	50 pF	—	16.0	
SOUT data hold time (after SCK edge)									
10	t_{HO}	CC	D	SOUT data hold time after SCK CPHA = 0[11]	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7 + t_{SYS}[5]	—	ns
					Strong	50 pF	–11.0 + t_{SYS}[5]	—	
					Medium	50 pF	–15.0 + t_{SYS}[5]	—	
				SOUT data hold time after SCK CPHA = 1[11]	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	
					Medium	50 pF	–15.0	—	

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. All timing values for output signals in this table are measured to 50% of the output voltage.
3. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
4. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
5. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
6. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
7. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
8. PCSx and PCSS using same pad configuration.
9. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
10. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.

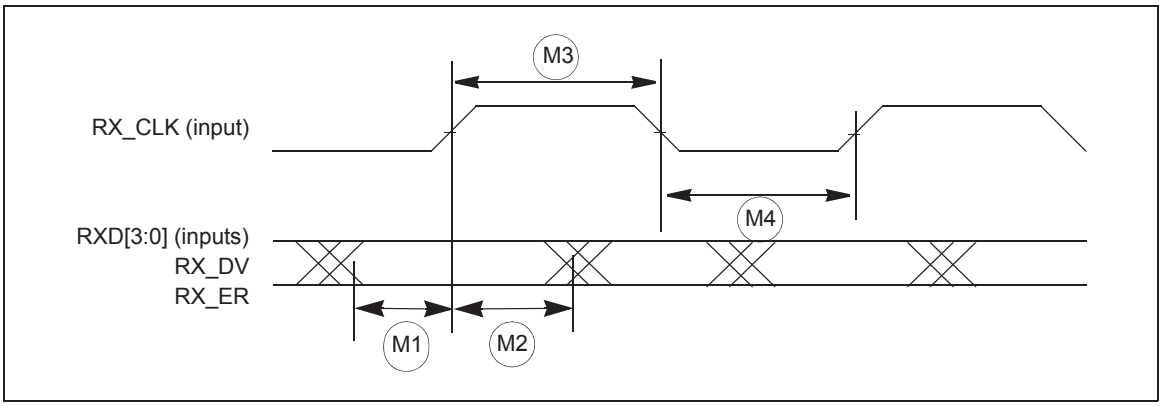
3.18.2.1.4 DSPI master mode – output only

Table 57. DSPI LVDS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock(1),(2)

#	Symbol		C	Characteristic	Condition		Value		Unit
					Pad drive	Load	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	LVDS	15 pF to 50 pF differential(3)	25.0	—	ns
2	t_{CSV}	CC	D	PCS valid after SCK(4) (SCK with 50 pF differential load cap.)	Very strong	25 pF	—	6.0	ns
					Strong	50 pF	—	10.5	ns
3	t_{CSH}	CC	D	PCS hold after SCK(4) (SCK with 50 pF differential load cap.)	Very strong	0 pF	–4.0	—	ns
					Strong	0 pF	–4.0	—	ns
4	t_{SDC}	CC	D	SCK duty cycle (SCK with 50 pF differential load cap.)	LVDS	15 pF to 50 pF differential	$^1/_2t_{SCK}$ – 2	$^1/_2t_{SCK}$ + 2	ns
SOUT data valid time (after SCK edge)									
5	t_{SUO}	CC	D	SOUT data valid time from SCK(5)	SOUT and SCK drive strength				
					LVDS	15 pF to 50 pF differential	—	3.5	ns
SOUT data hold time (after SCK edge)									
6	t_{HO}	CC	D	SOUT data hold time after SCK(5)	SOUT and SCK drive strength				
					LVDS	15 pF to 50 pF differential	–3.5	—	ns

1. All DSPI timing specifications apply to pins when using LVDS pads for SCK and SOUT and CMOS pad for PCS with pad driver strength as defined. Timing may degrade for weaker output drivers.
2. TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.
3. LVDS differential load considered is the capacitance on each terminal of the differential pair, as shown in *Figure 12*.
4. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
5. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances have the same value.

Figure 39. MII receive signal timing diagram



3.18.3.2 MII transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the *Microcontroller Reference Manual's* Ethernet chapter for details of this option and how to enable it.

Table 61. MII transmit signal timing(1)

Symbol		C	Characteristic	Value(2)		Unit
				Min	Max	
M5	CC	D	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
M6	CC	D	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
M7	CC	D	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	CC	D	TX_CLK pulse width low	35%	65%	TX_CLK period

1. All timing specifications are referenced from TX_CLK = 1.4 V to the valid output levels, 0.8 V and 2.0 V.
2. Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value

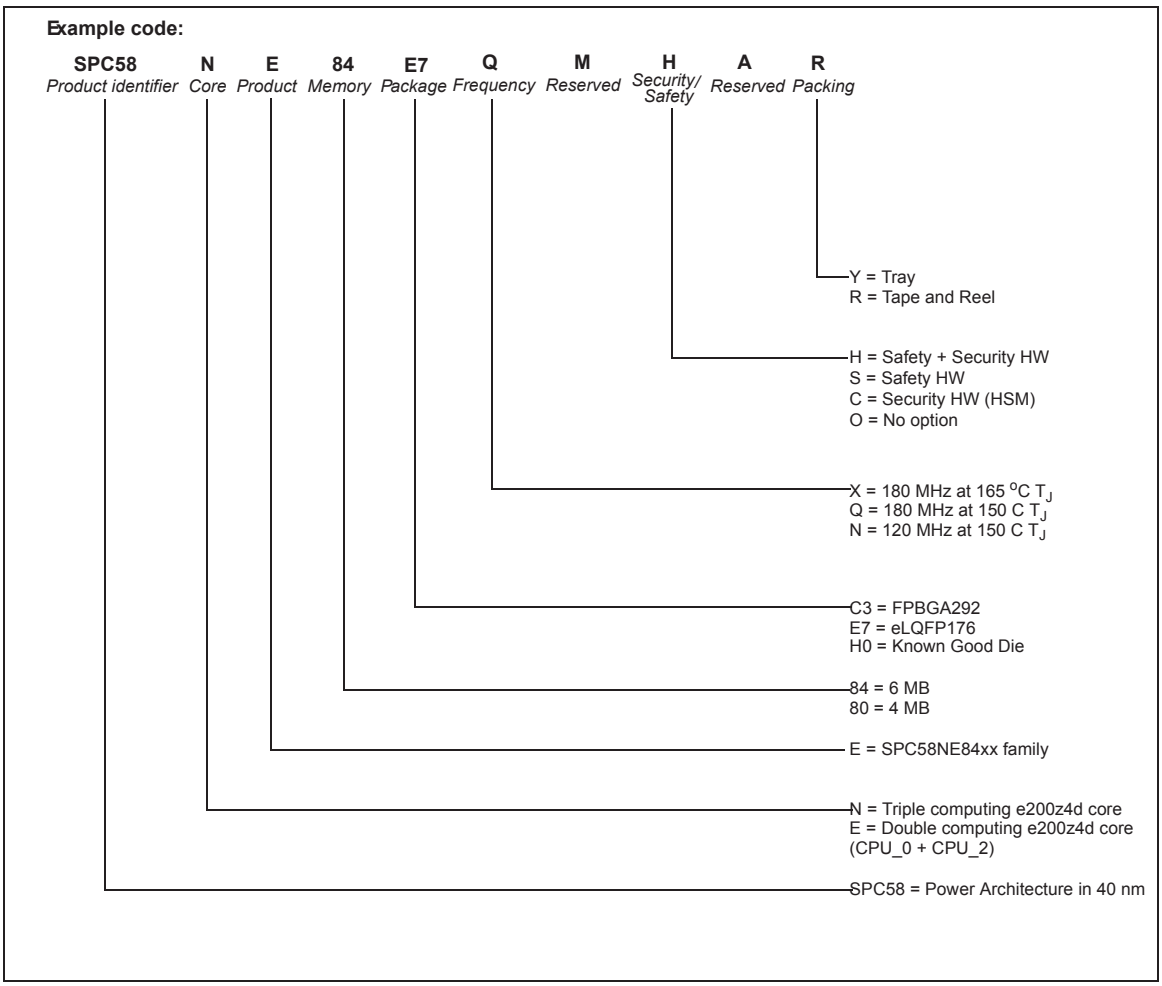
Table 76. eLQFP176 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09	—	0.20	0.003	—	0.008
D	25.80	26.00	26.20	1.016	1.023	1.031
D1	23.90	24.00	24.10	0.941	0.945	0.949
D2[2]	7.30	—	8.95	0.287	—	0.352
D3	—	21.5	—	—	0.846	—
E	25.80	26.00	26.20	1.016	1.023	1.031
E1	23.90	24.00	24.10	0.941	0.945	0.949
E2	7.30	—	8.95	0.287	—	0.352
E3[2]	—	21.50	—	—	0.846	—
e	—	0.50	—	—	0.019	—
L	0.45	0.60	0.75		0.024	
L1	—	1.00	—	—	0.039	—
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	—	—	0.08	—	—	0.003

1. Values in inches are converted from millimeters (mm) and rounded to four decimal digits.
2. The size of exposed pad is variable depending on leadframe design pad size.

5 Ordering information

Figure 53. Commercial product scheme



1. Please contact your ST sales office to ask for the availability of a particular commercial product.
2. Features (e.g. flash, RAM or peripherals) not included in the commercial product cannot be used. ST cannot be called to take any liability for features used outside the commercial product.

Table 80. Code Flash options

SPC58xE84 (6M)	SPC58xE80 (4M)	Partition	Start address	End address
16	16	0	0x00FC0000	0x00FC3FFF
16	16	0	0x00FC4000	0x00FC7FFF
16	16	1	0x00FC8000	0x00FCBFFF
16	16	1	0x00FCC000	0x00FCFFFF
32	32	0	0x00FD0000	0x00FD7FFF
32	32	1	0x00FD8000	0x00FDFFFF

Table 82. Document revision history (continued)

Date	Revision	Changes
03-April-2017	2	*Table 28: ADC-Comparator electrical specification*: – Classification for parameter "$I_{ADCREFH}$" changed from "C" to "T" – Removed table footnote "Values are subject to change (possibly improved to ±2 LSB) after characterization" – For parameter f_{ADCK} , replaced the min value "7.5" with ">13.33" *Table 26: ADC pin specification,*: For I_{LKG}, changed condition "C" to "—". *Table 29: SDn ADC electrical specification*: – Added footnote "When using a GAIN ... resolution of 15 bits" to parameter "RESOLUTION". – Added footnote "Conversion offset ... offset error" to parameter V_{OFFSET}. – Removed footnote "SNR value guaranteed ... frequency range" from parameters- $SNR_{DIFF150}$ and $SNR_{DIFF333}$. – In V_{cmrr}, changed "SR" to "CC" and "D" to "T" – Changed min value from "1.5" to "—" in parameter "I_{ADV_D}" – Changed min value from "3" to "—" in parameter "ΣI_{ADR_D}". – Added footnote "Consumption is given ... set-up" to parameter "ΣI_{ADR_D}" – Removed footnote "Sampling is .... $f_{ADCD\_M}/2$" – Updated footnote "S/D ADC is ...12 dB" – Added table footnote "This parameter ...3 dB less" to parameters - $SNR_{DIFF150}$, $SNR_{DIFF333}$, and SNR_{SE150} – Replaced the max value of ΣI_{ADR_D} of "16" with "80". *Figure 8: Input equivalent circuit (Fast SARn and SARB channels)*: Updated the figure. *Table 30: Temperature sensor electrical characteristics*: For "temperature monitoring range", classification removed (was C) *Table 35: LFAST PLL electrical characteristics*: – Min and Max value of parameter "ERR_{REF}" updated from "TBD" to "-1" and "+1" respectively – Max value of parameter "PN" updated from "TBD" to "-58" – Frequency of parameter "ΔPER_{REF}" updated from "10MHz" to "20MHz". – Max value of parameter "ΔPER_{REF}" for condition "Single period" updated from "TBD" to "350" – Min and Max value of parameter "ΔPER_{REF}" for condition "Long period" updated from "TBD" to "-500" and "+500" respectively. *Table 36: Aurora LVDS electrical characteristics,*: – For parameter $\lvert\Delta V_{I\_L}\rvert$, changed classification to "T" – For parameter $\lvert\Delta V_{OD\_LVDS}\rvert$, changed the classification to "T".