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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Tri-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA
Number of I/O	64
Program Memory Size	6MB (6M x 8)
Program Memory Type	FLASH
EEPROM Size	256K x 8
RAM Size	608K x 8
Voltage - Supply (Vcc/Vdd)	1.2V, 3.3V, 5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-eLQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc58ne84e7qmsar

Figure 1. Block diagram

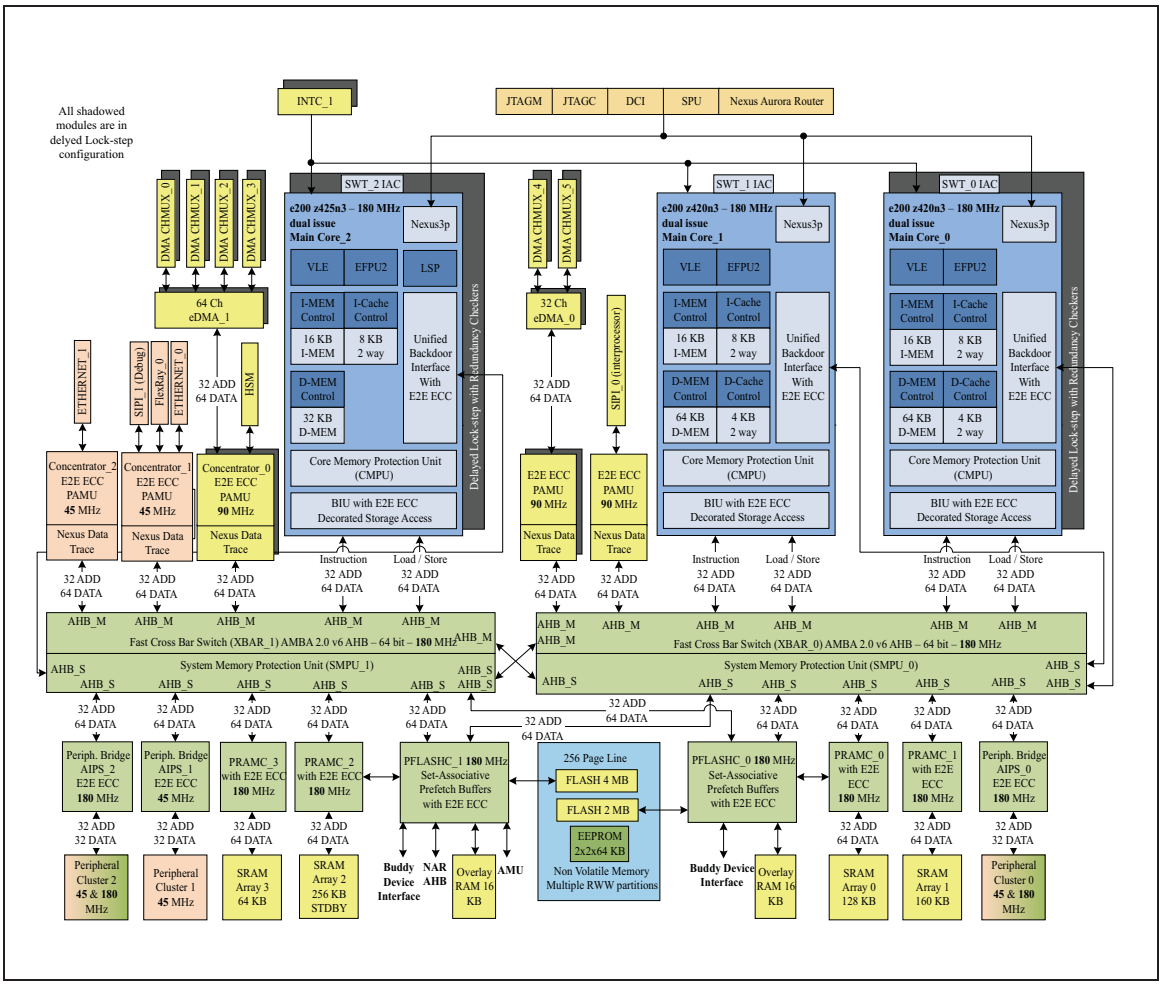


Table 5. Operating conditions (continued)

Symbol		C	Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
$V_{SS\_HV\_ADR\_D}$-$V_{SS\_HV\_ADV}$	SR	D	$V_{SS\_HV\_ADR\_D}$ differential voltage	—	–25	—	25	mV
$V_{DD\_HV\_ADR\_S}$	SR	P	SAR ADC reference voltage	—	3.0	—	5.5	V
$V_{DD\_HV\_ADR\_S}$-$V_{DD\_HV\_ADV}$	SR	D	SAR ADC reference differential voltage	—	$V_{DD\_HV\_ADV}$ -10%	—	25	mV
$V_{SS\_HV\_ADR\_S}$	SR	P	SAR ADC ground reference voltage	—	$V_{SS\_HV\_ADV}$			V
$V_{SS\_HV\_ADR\_S}$-$V_{SS\_HV\_ADV}$	SR	D	$V_{SS\_HV\_ADR\_S}$ differential voltage	—	–25	—	25	mV
V_{RAMP_LV}	SR	D	Slew rate on core power supply pins	V_{DD_LV} $V_{DD\_LV\_BD}$	—	—	20	V/ms
V_{RAMP_HV}	SR	D	Slew rate on HV power supply	—	—	—	100	V/ms
V_{IN}	SR	P	I/O input voltage range	—	0	—	5.5	V
I_{INJ1}	SR	T	DC Injection current (per pin) without performance degradation(8) (9) (10)	Digital pins and analog pins	–3.0	—	3.0	mA
I_{INJ2}	SR	D	Dynamic Injection current (per pin) with performance degradation(10) (11)	Digital pins and analog pins	–10	—	10	mA

1. The ranges in this table are design targets and actual data may vary in the given range.
2. The maximum number of PRAM wait states has to be configured according to the system clock frequency. Refer to *Table 6*.
3. Core voltage as measured on device pin to guarantee published silicon performance.
4. In the range [1.14-1.08]V, the device functionality and specifications are granted and the device is expected to receive a flag by the internal LVD100 monitors to warn that the regulator (internal or external), providing the V_{DD_LV} supply, exited the expected operating conditions. If the internal LVD100 monitors are disabled by the application, then an external voltage monitor with minimum threshold of V_{DD_LV}(min) = 1.08 V measured at the device pad, has to be implemented. Please refer to *Section 3.16.3: Voltage monitors* for the list of available internal monitors and to the Reference Manual for the configurability of the monitors.

5. Core voltage can exceed 1.26 V with the limitations provided in *Section 3.2: Absolute maximum ratings*, provided that HVD134_C monitor reset is disabled.
6. 1.260 V - 1.290 V range allowed periodically for supply with sinusoidal shape and average supply value below or equal to 1.236 V at the given temperature profile.
7. S/D ADC is functional in the range 3.0 V < $V_{DD\_HV\_ADV}$ < 4.0 V and 3.0 V < $V_{DD\_HV\_ADR\_D}$ < 4.0 V, but precision of conversion is not guaranteed.
8. Full device lifetime. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See *Section 3.2: Absolute maximum ratings* for maximum input current for reliability requirements.
9. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pins is above the supply rail, current will be injected through the clamp diode to the supply rails. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
10. The limits for the sum of all normal and injected currents on all pads within the same supply segment can be found in *Section 3.8.3: I/O pad current specifications*.
11. Positive and negative Dynamic current injection pulses are allowed up to this limit, with different specifications for I/O, ADC accuracy and analog input. See the dedicated chapters for the different specification limits. See the Absolute Maximum Ratings table for maximum input current for reliability requirements. Refer to the following pulses definitions: Pulse1 (ISO 7637-2:2011), Pulse 2a(ISO 7637-2:2011 5.6.2), Pulse 3a (ISO 7637-2:2011 5.6.3), Pulse 3b (ISO 7637-2:2011 5.6.3).

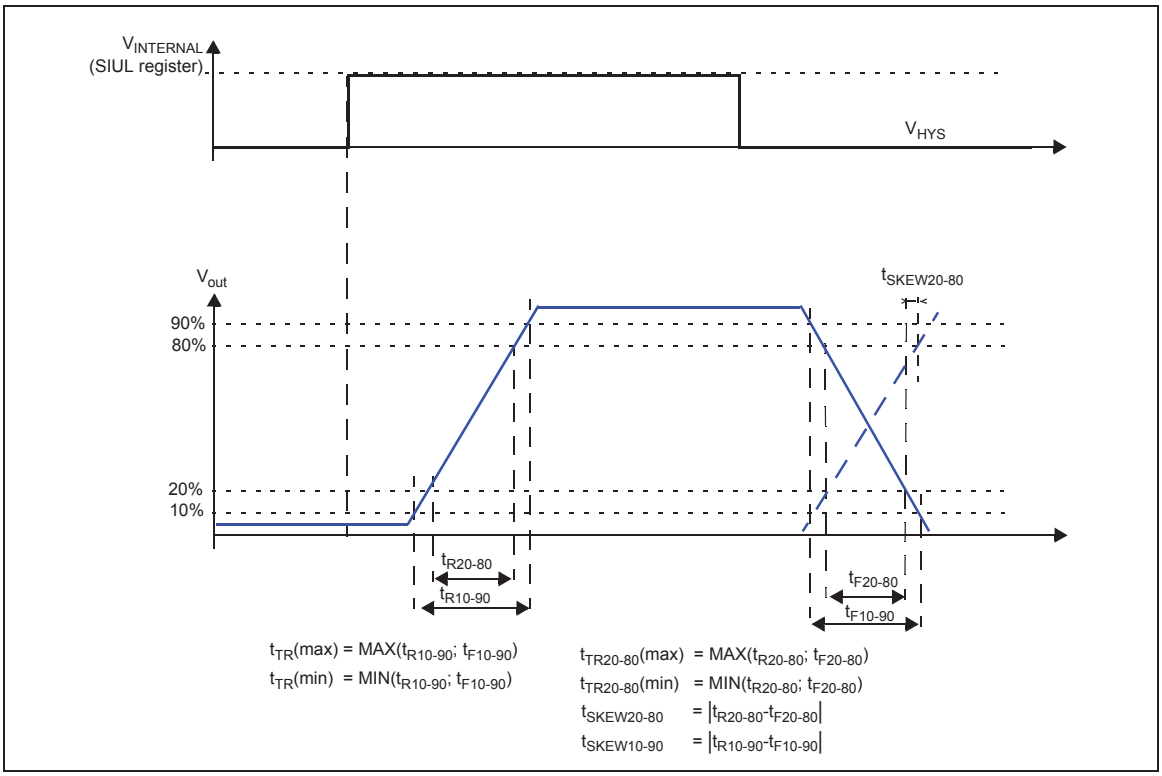
Table 6. PRAM wait states configuration

PRAMC WS	Clock Frequency (MHz)
1	≤ 180
0	≤ 120

3.3.1 Power domains and power up/down sequencing

The following table shows the constraints and relationships for the different power domains. Supply1 (on rows) can exceed Supply2 (on columns), only if the cell at the given row and column is reporting ‘ok’. This limitation is valid during power-up and power-down phases, as well as during normal device operation.

Figure 4. I/O output DC electrical characteristics definition



The following tables provide DC characteristics for bidirectional pads:

- *Table 13* provides output driver characteristics for I/O pads when in WEAK/SLOW configuration.
- *Table 14* provides output driver characteristics for I/O pads when in MEDIUM configuration.
- *Table 15* provides output driver characteristics for I/O pads when in STRONG/FAST configuration.
- *Table 16* provides output driver characteristics for I/O pads when in VERY STRONG/VERY FAST configuration.

Note: 10%/90% is the default condition for any parameter if not explicitly mentioned differently.

Table 13. WEAK/SLOW I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ol_W}	CC	D	Output low voltage for Weak type PADs	I_{ol} = 0.5 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	0.1*V_{DD}	V
V_{oh_W}	CC	D	Output high voltage for Weak type PADs	Ioh = 0.5 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	0.9*V_{DD}	—	—	V

Table 15. STRONG/FAST I/O output characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
F_{max_S}	CC	T	Maximum output frequency for Strong type PADs	CL = 25 pF V_{DD}=5.0 V ± 10%	—	—	50	MHz
				CL = 50 pF V_{DD}=5.0 V ± 10%	—	—	25	MHz
				CL = 25 pF V_{DD} = 3.3 V ± 10%	—	—	25	MHz
				CL = 50 pF V_{DD} = 3.3 V ± 10%	—	—	12.5	MHz
t_{TR_S}	CC	T	Transition time output pin STRONG configuration, 10%-90%	CL = 25 pF V_{DD} = 5.0 V ± 10%	3	—	10	ns
				CL = 50 pF V_{DD} = 5.0 V ± 10%	5	—	16	
				CL = 25 pF V_{DD} = 3.3 V ± 10%	3	—	15	
				CL = 50 pF V_{DD} = 3.3 V ± 10%	5	—	26	
I_{DCMAX_S}	CC	D	Maximum DC current	V_{DD} = 5 V ± 10%	—	—	8	mA
				V_{DD} = 3.3 V ± 10%	—	—	5.5	
$\lvert t_{SKEW\_S} \rvert$	CC	T	Difference between rise and fall time, 90%-10%	—	—	—	25	%

Table 16. VERY STRONG/VERY FAST I/O output characteristics

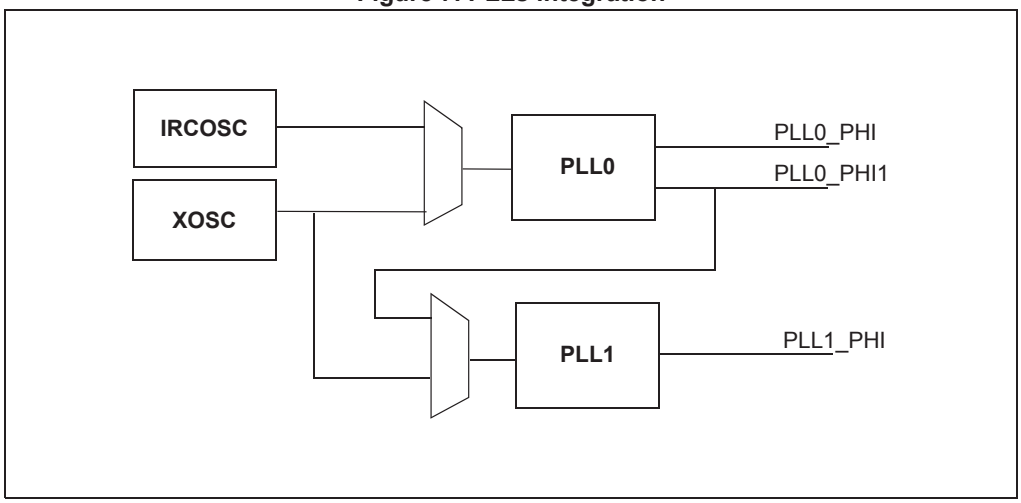
Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ol_V}	CC	D	Output low voltage for Very Strong type PADs	I_{ol} = 9.0 mA V_{DD} =5.0 V ± 10%	—	—	0.1*V_{DD}	V
				I_{ol} = 9.0 mA V_{DD} =3.3 V ± 10%	—	—	0.15*V_{DD}	V
V_{oh_V}	CC	D	Output high voltage for Very Strong type PADs	I_{oh} = 9.0 mA V_{DD} = 5.0 V ± 10%	0.9*V_{DD}	—	—	V
				I_{oh} = 9.0 mA V_{DD} = 3.3 V ± 10%	0.85*V_{DD}	—	—	V
$R_{\_V}$	CC	P	Output impedance for Very Strong type PADs	V_{DD} = 5.0 V ± 10%	20	—	60	Ω
				V_{DD} = 3.3 V ± 10%	18	—	50	

3.10 PLLs

Two phase-locked loop (PLL) modules are implemented to generate system and auxiliary clocks on the device.

Figure 7 depicts the integration of the two PLLs. Please, refer to device Reference Manual for more detailed schematic.

Figure 7. PLLs integration



3.10.1 PLL0

Table 20. PLL0 electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{PLL0IN}	SR	—	PLL0 input clock(1)	—	8	—	44	MHz
Δ_{PLL0IN}	SR	—	PLL0 input clock duty cycle(1)	—	40	—	60	%
f_{INFIN}	SR	—	PLL0 PFD (Phase Frequency Detector) input clock frequency	—	8	—	20	MHz
$f_{PLL0VCO}$	CC	P	PLL0 VCO frequency	—	600	—	1400	MHz
$f_{PLL0PHI0}$	CC	D	PLL0 output frequency	—	4.762	—	400	MHz
$f_{PLL0PHI1}$	CC	D	PLL0 output clock PHI1	—	20	—	175(2)	MHz
$t_{PLL0LOCK}$	CC	P	PLL0 lock time	—	—	—	100	µs
$\lvert\Delta_{PLL0PHI0SPJ}\rvert$ (3)	CC	T	PLL0_PHI0 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI0}$ = 400 MHz, 6-sigma	—	—	200	ps

Table 20. PLL0 electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$\lvert\Delta_{PLL0PHI1SPJ}\rvert^{(3)}$	CC	T	PLL0_PHI1 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI1}$ = 40 MHz, 6-sigma	—	—	300(4)	ps
$\Delta_{PLL0LTJ}$(3)	CC	T	PLL0 output long term jitter(4) f_{PLL0IN} = 20 MHz (resonator), VCO frequency = 800 MHz	10 periods accumulated jitter (80 MHz equivalent frequency), 6-sigma pk-pk	—	—	±250	ps
				16 periods accumulated jitter (50 MHz equivalent frequency), 6-sigma pk-pk	—	—	±300	ps
				long term jitter (< 1 MHz equivalent frequency), 6-sigma pk-pk)	—	—	±500	ps
I_{PLL0}	CC	T	PLL0 consumption	FINE LOCK state	—	—	6	mA

1. PLL0IN clock retrieved directly from either internal RCOSC or external FXOSC clock. Input characteristics are granted when using internal RCOSC or external oscillator is used in functional mode.
2. If the PLL0_PHI1 is used as an input for PLL1, then the PLL0_PHI1 frequency shall obey the maximum input frequency limit set for PLL1 (87.5 MHz, according to *Table 21*).
3. Jitter values reported in this table refer to the internal jitter, and do not include the contribution of the divider and the path to the output CLKOUT pin.
4. V_{DD_LV} noise due to application in the range V_{DD_LV} = 1.20 V±5%, with frequency below PLL bandwidth (40 kHz) will be filtered.

Table 29. SDn ADC electrical specification[1] (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Z_{CM}	CC	D	Common mode input impedance (f_{ADCD_M} = 16 MHz)	GAIN = 1	1250	1600	2000	kΩ
		D		GAIN = 2	900	1150	1450	
		D		GAIN = 4	620	850	1050	
		D		GAIN = 8	450	580	720	
		D		GAIN = 16	450	580	720	
R_{BIAS}	CC	D	Bias resistance	—	120	160	200	kΩ
V_{BIAS}	CC	D	Bias voltage	—	—	$V_{DD\_HV\_ADR\_D}/2$	—	V
ΔV_{INTCM}	CC	D	common mode input reference voltage	—	–12	$(V_{DD\_HV\_ADV} + V_{SS\_HV\_ADV})/2$	+12	%
δV_{BIAS}	CC	D	Bias voltage accuracy	—	–2.5	—	+2.5	%
V_{cmrr}	CC	T	Common mode rejection ratio	—	55	—	—	dB
R_{Caaf}	SR	D	Anti-aliasing filter	External series resistance	—	—	20	kΩ
	CC	D		Filter capacitances	180	—	—	pF
$f_{PASSBAND}$	CC	D	Pass band[13]	—	0.01		0.333 * f_{ADCD_S}	kHz
δ_{RIPPLE}	CC	D	Pass band ripple[14]	0.333 * f_{ADCD_Sin}	–1	—	1	%
$F_{rolloff}$	CC	D	Stop band attenuation	[0.5 * f_{ADCD_S}, 1.0 * f_{ADCD_S}]	40	—	—	dB
				[1.0 * f_{ADCD_S}, 1.5 * f_{ADCD_S}]	45	—	—	
				[1.5 * f_{ADCD_S}, 2.0 * f_{ADCD_S}]	50	—	—	
				[2.0 * f_{ADCD_S}, 2.5 * f_{ADCD_S}]	55	—	—	
				[2.5 * f_{ADCD_S}, f_{ADCD_M}/2]	60	—	—	

13. SNR value guaranteed only if external noise on the ADC input pin is attenuated by the required SNR value in the frequency range of $f_{ADCD\_M} - f_{ADCD\_S}$ to $f_{ADCD\_M} + f_{ADCD\_S}$, where f_{ADCD_M} is the input sampling frequency, and f_{ADCD_S} is the output sample frequency. A proper external input filter should be used to remove any interfering signals in this frequency range.
14. The ±1% passband ripple specification is equivalent to $20 * \log_{10}(0.99) = 0.087$ dB.
15. Propagation of the information from the pin to the register CDR[CDATA] and flags SFR[DFEF], SFR[DFFF] is given by the different modules that need to be crossed: delta/sigma filters, high pass filter, fifo module, clock domain synchronizers. The time elapsed between data availability at pin and internal S/D module registers is given by the below formula: REGISTER LATENCY = $t_{LATENCY} + 0.5/f_{ADCD\_S} + 2\ (\sim+1)/f_{ADCD\_M} + 2(\sim+1)f_{PBRIDGEx\_CLK}$ where f_{ADCD_S} is the frequency of the sampling clock, f_{ADCD_M} is the frequency of the modulator, and $f_{PBRIDGEx\_CLK}$ is the frequency of the peripheral bridge clock feeds to the ADC S/D module. The (~+1) symbol refers to the number of clock cycles uncertainty (from 0 to 1 clock cycle) to be added due to resynchronization of the signal during clock domain crossing. Some further latency may be added by the target module (core, DMA, interrupt) controller to process the data received from the ADC S/D module.
16. This capacitance does not include pin capacitance, that can be considered together with external capacitance, before sampling switch.
17. Consumption is given after power-up, when steady state is reached. Extra consumption up to 2 mA may be required during internal circuitry set-up.

3.13 Temperature Sensor

The following table describes the temperature sensor electrical characteristics.

Table 30. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	CC	—	Temperature monitoring range	—	–40	—	165	°C
T_{SENS}	CC	T	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	CC	P	Accuracy	T_J < 150 °C	–3	—	3	°C
		C		T_J < 165 °C	–7	—	7	

Figure 10. Power-down exit time

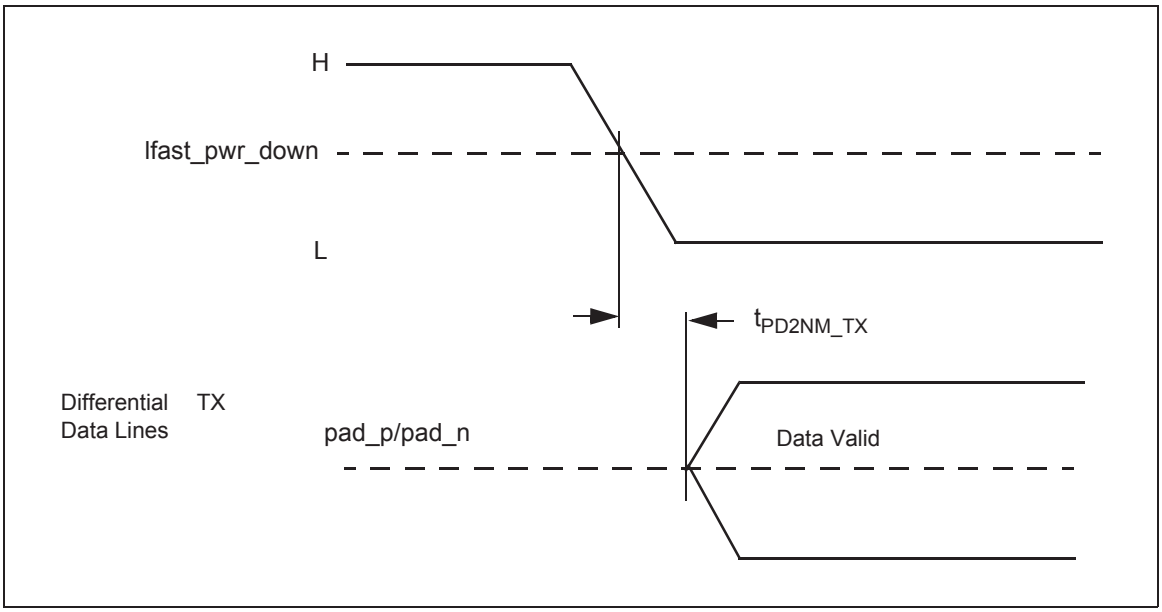
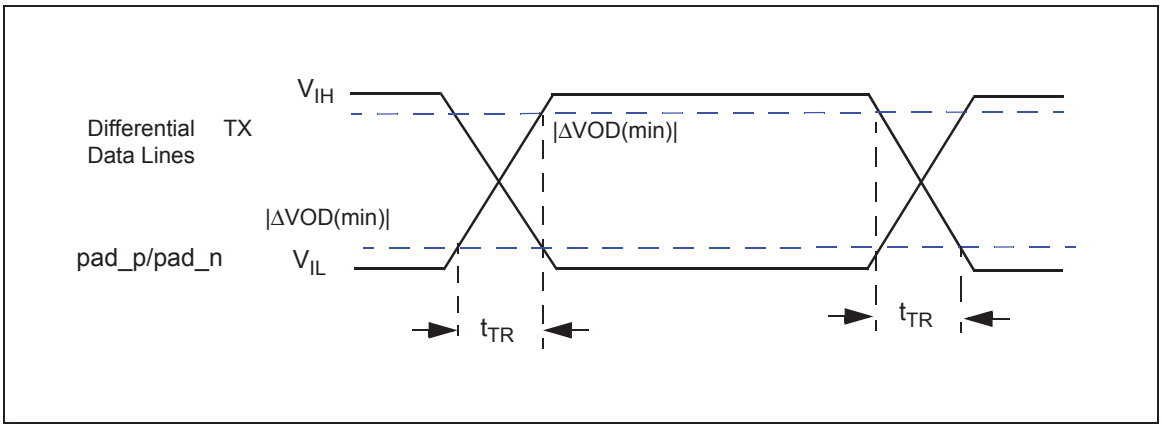


Figure 11. Rise/fall time



3.14.2 LFAST and MSC/DSPI LVDS interface electrical characteristics

The following table contains the electrical characteristics for the LFAST interface.

Table 31. LVDS pad startup and receiver electrical characteristics(1),(2)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
STARTUP(3),(4)								
t_{STRT_BIAS}	CC	T	Bias current reference startup time(5)	—	—	0.5	4	µs
t_{PD2NM_TX}	CC	T	Transmitter startup time (power down to normal mode)(6)	—	—	0.4	2.75	µs

Table 44. Voltage monitor electrical characteristics (continued)

Symbol		C	Supply/Parameter	Conditions	Value[1]			Unit
					Min	Typ	Max	
V_{LVD290_F}	CC	P	$V_{DD\_HV\_FLA}$	—	2.89	2.94	2.99	V
V_{LVD290_AD}	CC	P	$V_{DD\_HV\_ADV}$ (ADCSD pad)	—	2.89	2.94	2.99	V
V_{LVD290_AS}	CC	P	$V_{DD\_HV\_ADV}$ (ADCSAR pad)	—	2.89	2.94	2.99	V
V_{LVD290_IJ}	CC	P	$V_{DD\_HV\_IO\_JTAG}$	—	2.89	2.94	2.99	V
V_{LVD290_IF}	CC	P	$V_{DD\_HV\_IO\_FLEX}$	—	2.89	2.94	2.99	V
V_{LVD400_AD}	CC	P	$V_{DD\_HV\_ADV}$ (ADCSD pad)	—	4.15	4.23	4.31	V
V_{LVD400_AS}	CC	P	$V_{DD\_HV\_ADV}$ (ADCSAR pad)	—	4.15	4.23	4.31	V
V_{LVD400_IM}	CC	P	$V_{DD\_HV\_IO\_MAIN}$	—	4.15	4.23	4.31	V
V_{LVD400_IJ}	CC	P	$V_{DD\_HV\_IO\_JTAG}$		4.15	4.23	4.31	V
V_{LVD400_IF}	CC	P	$V_{DD\_HV\_IO\_FLEX}$	—	4.15	4.23	4.31	V
High Voltage Detectors HV								
V_{HVD400_C}	CC	P	$V_{DD\_HV\_IO\_MAIN}$		3.68	3.75	3.82	V
V_{HVD400_IJ}	CC	P	$V_{DD\_HV\_IO\_JTAG}$		3.68	3.75	3.82	V
V_{HVD400_IF}	CC	P	$V_{DD\_HV\_IO\_FLEX}$	—	3.68	3.75	3.82	V
Upper Voltage Detectors HV								
V_{UVD600_C}	CC	P	$V_{DD\_HV\_IO\_MAIN}$		5.72	5.82	5.92	V
V_{UVD600_F}	CC	P	$V_{DD\_HV\_FLA}$	—	5.72	5.82	5.92	V
V_{UVD600_IJ}	CC	P	$V_{DD\_HV\_IO\_JTAG}$	—	5.72	5.82	5.92	V
V_{UVD600_IF}	CC	P	$V_{DD\_HV\_IO\_FLEX}$	—	5.72	5.82	5.92	V
PowerOn Reset LV								
V_{POR031_C}	CC	P	V_{DD_LV}	—	0.29	0.60	0.97	V
Minimum Voltage Detectors LV								
V_{MVD082_C}	CC	P	V_{DD_LV}	—	0.85	0.88	0.91	V
V_{MVD082_B}	CC	P	$V_{DD\_LV\_BD}$	—	0.85	0.88	0.91	V
V_{MVD094_C}	CC	P	V_{DD_LV}	—	0.98	1.00	1.02	V
V_{MVD094_FA}	CC	P	V_{DD_LV} (Flash)	—	1.00	1.02	1.04	V
V_{MVD094_FB}	CC	P	V_{DD_LV} (Flash)	—	1.00	1.02	1.04	V
Low Voltage Detectors LV								
V_{LVD100_C}	CC	P	V_{DD_LV}	—	1.06	1.08	1.11	V
V_{LVD100_SB}	CC	P	V_{DD_LV} (In Standby)	—	0.99	1.01	1.03	V
V_{LVD100_F}	CC	P	V_{DD_LV} (Flash)	—	1.08	1.10	1.12	V
High Voltage Detectors LV								
V_{HVD134_C}	CC	P	V_{DD_LV}	—	1.28	1.31	1.33	V

Table 49. Nexus debug port timing(1) (continued)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
12	t_{NTDIH}	CC	D	TDI data hold time	5	—	ns
13	t_{NTMSS}	CC	D	TMS data setup time	5	—	ns
14	t_{NTMSH}	CC	D	TMS data hold time	5	—	ns
15	—	CC	D	TDO propagation delay from falling edge of TCK(8)	—	16	ns
16	—	CC	D	TDO hold time with respect to TCK falling edge (minimum TDO propagation delay)	2.25	—	ns

1. Nexus timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 3.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet.
2. t_{CYC} is system clock period.
3. Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual peripheral frequency being used. To ensure proper operation TCK frequency should be set to the peripheral frequency divided by a number greater than or equal to that specified here.
4. This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.
5. This value is TDO propagation time 36 ns + 4 ns setup time to sampling edge.
6. This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.
7. This value is TDO propagation time 16n s + 4 ns setup time to sampling edge.
8. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.

Figure 22. Nexus output timing

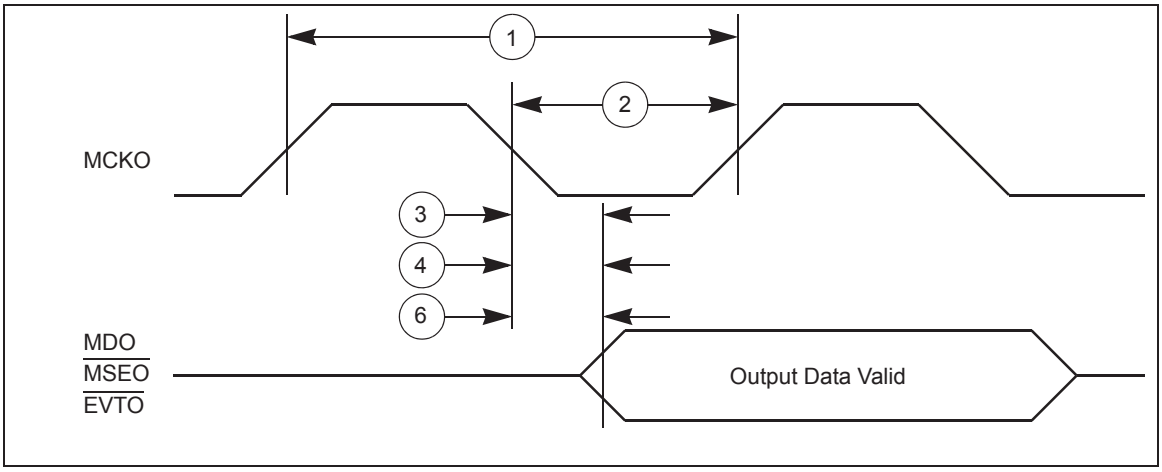


Figure 23. Nexus event trigger and test clock timings

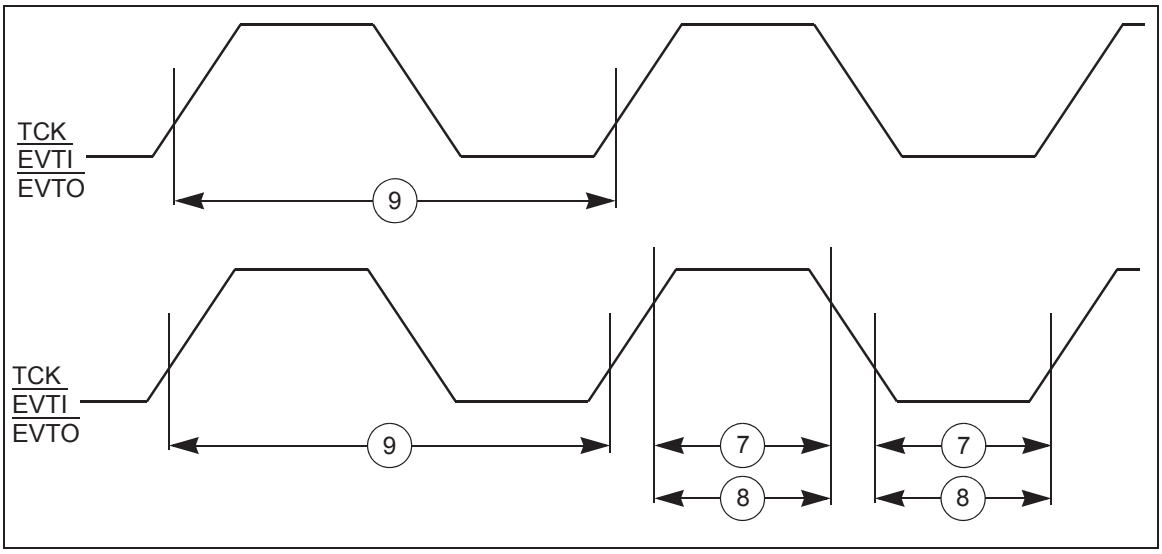


Figure 24. Nexus TDI, TMS, TDO timing

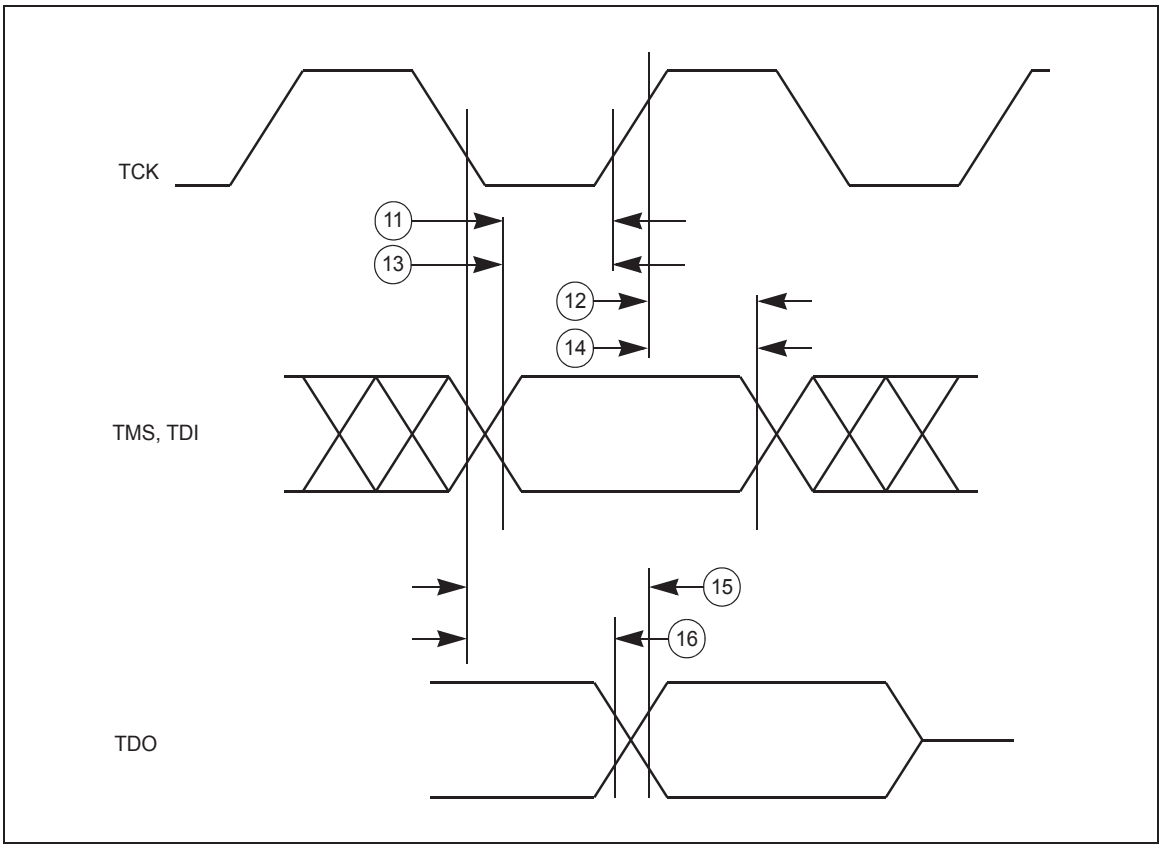
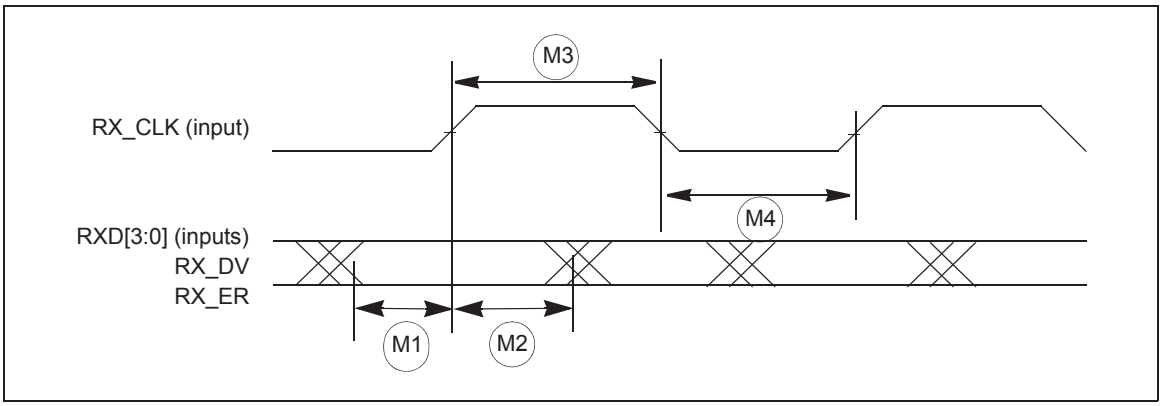


Table 55. DSPI CMOS master modified timing (full duplex and output only) — MTFE = 1, CPHA = 0 or 1[1] (continued)

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
9	t_{SUO}	CC	D	SOUT data valid time from SCK CPHA = 0[10]	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0 + t_{SYS}[5]	ns
					Strong	50 pF	—	8.0 + t_{SYS}[5]	
					Medium	50 pF	—	16.0 + t_{SYS}[5]	
				SOUT data valid time from SCK CPHA = 1[10]	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	8.0	
					Medium	50 pF	—	16.0	
SOUT data hold time (after SCK edge)									
10	t_{HO}	CC	D	SOUT data hold time after SCK CPHA = 0[11]	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7 + t_{SYS}[5]	—	ns
					Strong	50 pF	–11.0 + t_{SYS}[5]	—	
					Medium	50 pF	–15.0 + t_{SYS}[5]	—	
				SOUT data hold time after SCK CPHA = 1[11]	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	
					Medium	50 pF	–15.0	—	

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. All timing values for output signals in this table are measured to 50% of the output voltage.
3. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
4. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
5. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
6. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
7. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
8. PCSx and PCSS using same pad configuration.
9. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
10. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.

Figure 39. MII receive signal timing diagram



3.18.3.2 MII transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the *Microcontroller Reference Manual's* Ethernet chapter for details of this option and how to enable it.

Table 61. MII transmit signal timing(1)

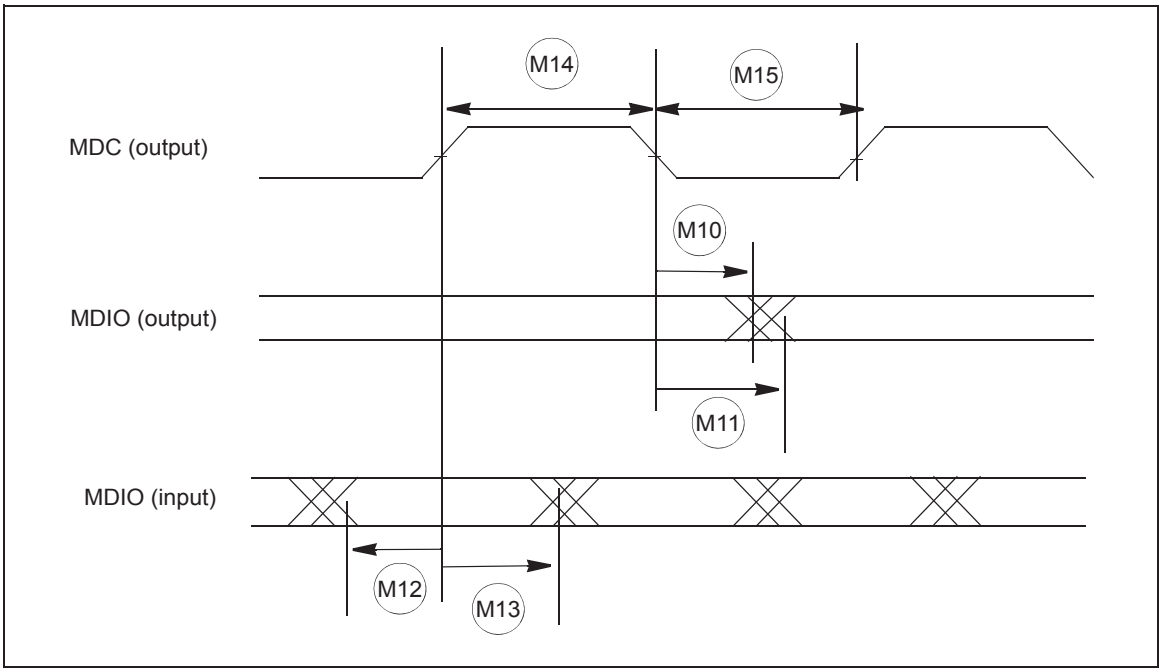
Symbol		C	Characteristic	Value(2)		Unit
				Min	Max	
M5	CC	D	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
M6	CC	D	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
M7	CC	D	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	CC	D	TX_CLK pulse width low	35%	65%	TX_CLK period

1. All timing specifications are referenced from TX_CLK = 1.4 V to the valid output levels, 0.8 V and 2.0 V.
2. Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value

3.18.3.4 MII and RMII serial management channel timing (MDIO and MDC)

The Ethernet functions correctly with a maximum MDC frequency of 2.5 MHz.

Figure 42. MII serial management channel timing diagram



3.18.3.5 MII and RMII serial management channel timing (MDIO and MDC)

The Ethernet functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 63. MII serial management channel timing(1)

Symbol		C	Characteristic	Value		Unit
				Min	Max	
M10	CC	D	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	CC	D	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	CC	D	MDIO (input) to MDC rising edge setup	10	—	ns
M13	CC	D	MDIO (input) to MDC rising edge hold	0	—	ns
M14	CC	D	MDC pulse width high	40%	60%	MDC period
M15	CC	D	MDC pulse width low	40%	60%	MDC period

1. All timing specifications are referenced from MDC = 1.4 V (TTL levels) to the valid input and output levels, 0.8 V and 2.0 V (TTL levels). For 5 V operation, timing is referenced from MDC = 50% to 2.2 V/3.5 V input and output levels.

3.18.4.2 TxD

Figure 48. TxD signal

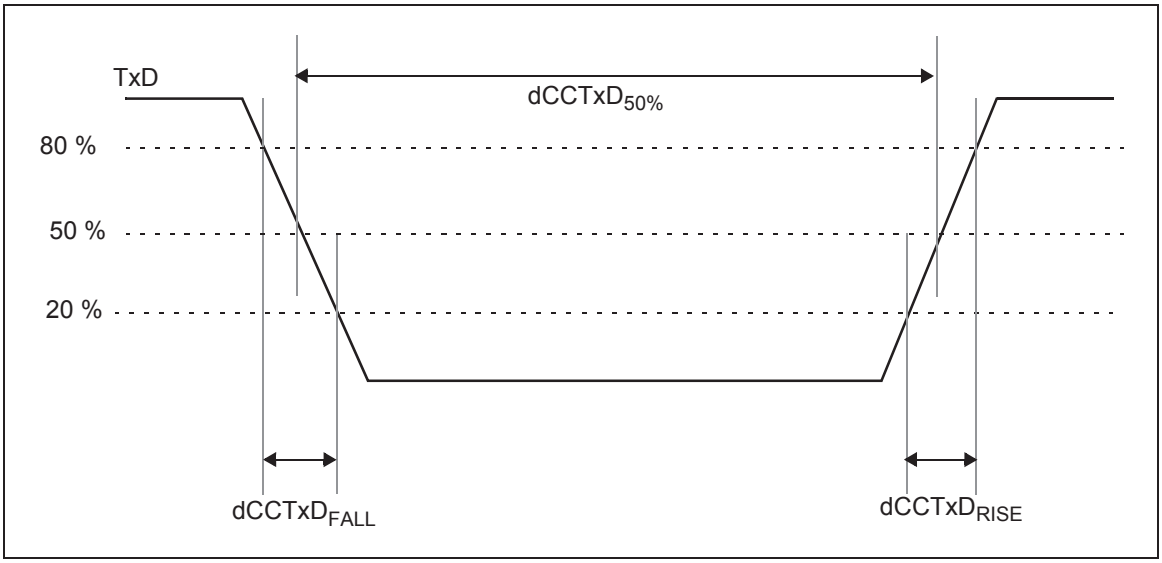


Table 68. TxD output characteristics(1),(2)

Symbol		C	Characteristic	Value		Unit
				Min	Max	
dCCTxAsym	CC	D	Asymmetry of sending CC at 25 pF load (= $dCCTxD_{50\%}$ – 100 ns)	–2.45	2.45	ns
$dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$	CC	D	Sum of Rise and Fall time of TxD signal at the output pin(3),(4)	—	9(5)	ns
		D		—	9(6)	
$dCCTxD_{01}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxD_{10}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. TxD pin load maximum 25 pF.
2. Specifications valid according to FlexRay EPL 3.0.1 standard with 20%–80% levels and a 10 pF load at the end of a 50 Ohm, 1 ns stripline. Please refer to the Very Strong I/O pad specifications.
3. Pad configured as VERY STRONG.
4. Sum of transition time simulation is performed according to Electrical Physical Layer Specification 3.0.1 and the entire temperature range of the device has been taken into account.
5. $V_{DD\_HV\_IO}$ = 5.0 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 1 ns, C_L = 10 pF.
6. $V_{DD\_HV\_IO}$ = 3.3 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 0.6 ns, C_L = 10 pF.

Table 82. Document revision history (continued)

Date	Revision	Changes
03-April-2017	2	*Section 3.17: Flash memory*: Updated the section. *Table 49: Nexus debug port timing*: Classification of parameters "t_{EVTIPW}" and "t_{EVTOPW}" changed from "P" to "D". *Table 55: DSPI CMOS master modified timing (full duplex and output only) — MTFE = 1, CPHA = 0 or 1*: Changed the Min value of t_{SCK} (very strong) from 33 to 59. *Table 56: DSPI LVDS master timing — full duplex — modified transfer format (MTFE = 1), CPHA = 0 or 1*: Added footnote "LVDS differential load considered is the capacitance on each terminal of the differential pair, as shown in *Figure 12*" to t_{SCK}. *Table 57: DSPI LVDS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock,*: Added footnote "LVDS differential load considered is the capacitance on each terminal of the differential pair, as shown in *Figure 12*" to t_{SCK}. *Table 53: DSPI channel frequency support*: Added column to show slower and faster frequencies. *Section 5: Ordering information*: Renamed figure "Ordering information scheme" to "Commercial product scheme" Added tables: *Table 80: Code Flash options*, and *Table 81: RAM options*

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