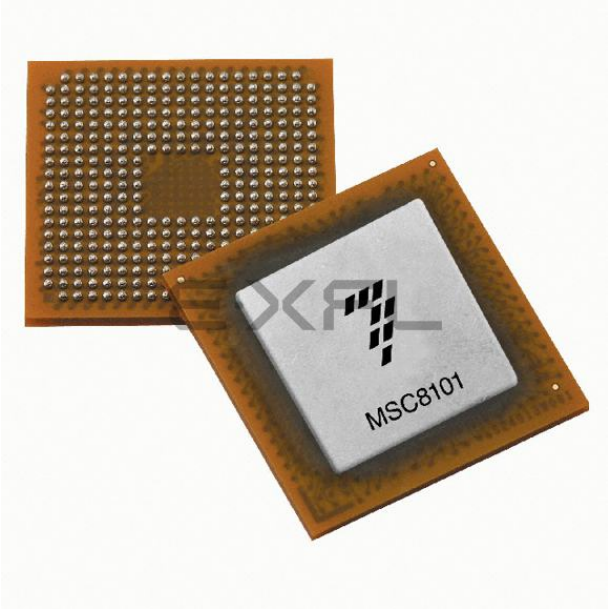


Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC140 Core
Interface	Communications Processor Module (CPM)
Clock Rate	275MHz
Non-Volatile Memory	External
On-Chip RAM	512kB
Voltage - I/O	3.30V
Voltage - Core	1.60V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	332-BFBGA, FCBGA
Supplier Device Package	332-FCBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8101vt1375f

Table of Contents

Data Sheet Conventions

pin and pin-out	Although the device package does not have pins, the term pins and pin-out are used for convenience and indicate specific signal locations within the ball-grid array.
$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
“asserted”	Means that a high true (active high) signal is high or that a low true (active low) signal is low
“deasserted”	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Although there are eight interrupt request ($\overline{\text{IRQ}}$) connections to the core processor, there are multiple external lines that can connect to these internal signal lines. After reset, the default configuration includes two $\overline{\text{IRQ1}}$ and two $\overline{\text{IRQ7}}$ input lines. The designer must select one line for each required interrupt and reconfigure the other external signal line or lines for alternate functions.

Table 1-5. System Bus, HDI16, and Interrupt Signals

Signal	Data Flow	Description
A[0–31]	Input/Output	**Address Bus** When the MSC8101 is in external master bus mode, these pins function as the address bus. The MSC8101 drives the address of its internal bus masters and responds to addresses generated by external bus masters. When the MSC8101 is in Internal Master Bus mode, these pins are used as address lines connected to memory devices and are controlled by the MSC8101 memory controller.
TT[0–4]	Input/Output	**Bus Transfer Type** The bus master drives these pins during the address tenure to specify the type of transaction.
TSIZ[0–3]	Input/Output	**Transfer Size** The bus master drives these pins with a value indicating the number of bytes transferred in the current transaction.
$\overline{\text{TBST}}$	Input/Output	**Bus Transfer Burst** The bus master asserts this pin to indicate that the current transaction is a burst transaction (transfers four quad words).
$\overline{\text{IRQ1}}$	Input	**Interrupt Request 1**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
$\overline{\text{GBL}}$	Input/Output	**Global**[1] When a master within the chip initiates a bus transaction, it drives this pin. When an external master initiates a bus transaction, it should drive this pin. Assertion of this pin indicates that the transfer is global and it should be snooped by caches in the system.
Reserved	Output	The primary configuration is reserved.
BADDR29	Output	**Burst Address 29**[1] One of five outputs of the memory controller. These pins connect directly to memory devices controlled by the MSC8101 memory controller.
$\overline{\text{IRQ2}}$	Input	**Interrupt Request 2**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
Reserved	Output	The primary configuration is reserved.
BADDR30	Output	**Burst Address 30**[1] One of five outputs of the memory controller. These pins connect directly to memory devices controlled by the MSC8101 memory controller.
$\overline{\text{IRQ3}}$	Input	**Interrupt Request 3**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
Reserved	Output	The primary configuration is reserved.
BADDR31	Output	**Burst Address 31**[1] One of five outputs of the memory controller. These pins connect directly to memory devices controlled by the MSC8101 memory controller.
$\overline{\text{IRQ5}}$	Input	**Interrupt Request 5**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.

Table 1-5. System Bus, HDI16, and Interrupt Signals (Continued)

Signal	Data Flow	Description
$\overline{BR}$	Input/Output Output	**Bus Request**[2] An output when an external arbiter is used. The MSC8101 asserts this pin to request ownership of the bus.
	Input	An input when an internal arbiter is used. An external master should assert this pin to request bus ownership from the internal arbiter.
$\overline{BG}$	Input/Output Output	**Bus Grant**[2] An output when an internal arbiter is used. The MSC8101 asserts this pin to grant bus ownership to an external bus master.
	Input	An input when an external arbiter is used. The external arbiter should assert this pin to grant bus ownership to the MSC8101.
$\overline{ABB}$	Input/Output Output	**Address Bus Busy**[1] The MSC8101 asserts this pin for the duration of the address bus tenure. Following an address acknowledge ($\overline{AACK}$) signal, which terminates the address bus tenure, the MSC8101 deasserts $\overline{ABB}$ for a fraction of a bus cycle and then stops driving this pin.
	Input	The MSC8101 does not assume bus ownership while it this pin is asserted by an external bus master.
$\overline{IRQ2}$	Input	**Interrupt Request 2**[1] One of the eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
$\overline{TS}$	Input/Output	**Bus Transfer Start** Signals the beginning of a new address bus tenure. The MSC8101 asserts this signal when one of its internal bus masters (SC140 core or DMA controller) begins an address tenure. When the MSC8101 senses this pin being asserted by an external bus master, it responds to the address bus tenure as required (snoop if enabled, access internal MSC8101 resources, memory controller support).
$\overline{AACK}$	Input/Output	**Address Acknowledge** A bus slave asserts this signal to indicate that it identified the address tenure. Assertion of this signal terminates the address tenure.
$\overline{ARTRY}$	Input	**Address Retry** Assertion of this signal indicates that the bus transaction should be retried by the bus master. The MSC8101 asserts this signal to enforce data coherency with its internal cache and to prevent deadlock situations.
$\overline{DBG}$	Input/Output Output	**Data Bus Grant**[2] An output when an internal arbiter is used. The MSC8101 asserts this pin as an output to grant data bus ownership to an external bus master.
	Input	An input when an external arbiter is used. The external arbiter should assert this pin as an input to grant data bus ownership to the MSC8101.
$\overline{DBB}$	Input/Output Output	**Data Bus Busy**[1] The MSC8101 asserts this pin as an output for the duration of the data bus tenure. Following a $\overline{TA}$, which terminates the data bus tenure, the MSC8101 deasserts $\overline{DBB}$ for a fraction of a bus cycle and then stops driving this pin.
	Input	The MSC8101 does not assume data bus ownership while $\overline{DBB}$ is asserted by an external bus master.
$\overline{IRQ3}$	Input	**Interrupt Request 3**[1] One of the eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
D[0–31]	Input/Output	**Data Bus Most Significant Word** In write transactions the bus master drives the valid data on this bus. In read transactions the slave drives the valid data on this bus. In Host Port Disabled mode, these 32 bits are part of the 64-bit data bus. In Host Port Enabled mode, these bits are used as the bus in 32-bit mode.

Table 1-7. Port A Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	Peripheral Controller: Dedicated Signal *Protocol*		
PA7	SMC2: $\overline{\text{SMSYN}}$	Input	**SMC2: Serial Management Synchronization** The SMC interface consists of SMTXD, SMRXD, SMSYN, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent, or general-circuit interface (GCI).
	SI1 TDMA1: L1TSYNC *TDM nibble* and *TDM serial*	Input	**Time-Division Multiplexing A1: Layer 1 Transmit Synchronization** The synchronizing signal for the transmit channel. See the *Serial Interface with* time-slot assigner chapter in the *MSC8101 Reference Manual*.
PA6	SI1 TDMA1: L1RSYNC *TDM nibble* and *TDM serial*	Input	**Time-Division Multiplexing A1: Layer 1 Receive Synchronization.** The synchronizing signal for the receive channel.

1.6.2 Port B Signals

Table 1-8. Port B Signals

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	Peripheral Controller: Dedicated I/O *Protocol*		
PB31	FCC2: TX_ER *MII*	Output	**FCC2: Media Independent Interface Transmit Error** Asserted by the MSC8101 to force propagation of transmit errors.
	SCC2: RXD	Input	**SCC2: Receive Data** SCC2 receives serial data from RXD.
	SI2 TDMB2: L1TXD *TDM serial*	Output	**Time-Division Multiplexing B2: Layer 1 Transmit Data** TDMB2 transmits serial data out of L1TXD.
PB30	SCC2: TXD	Output	**SCC2: Transmit Data.** SCC2 transmits serial data out of TXD.
	FCC2: RX_DV *MII*	Input	**FCC2: Media Independent Interface Receive Data Valid** Asserted by an external fast Ethernet PHY to indicate that valid data is being sent. The presence of carrier sense, but not RX_DV, indicates reception of broken packet headers, probably due to bad wiring or a bad circuit.
	SI2 TDMB2: L1RXD *TDM serial*	Input	**Time-Division Multiplexing B2: Layer 1 Receive Data** TDMB2 receives serial data from L1RXD.
PB29	FCC2: TX_EN *MII*	Output	**FCC2: Media Independent Interface Transmit Enable** Asserted by the MSC8101 when transmitting data.
	SI2 TDMB2: L1RSYNC *TDM serial*	Input	**Time-Division Multiplexing B2: Layer 1 Receive Synchronization** The synchronizing signal for the receive channel.

Table 1-8. Port B Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	Peripheral Controller: Dedicated I/O *Protocol*		
PB28	FCC2: $\overline{\text{RTS}}$ *HDLC serial*, *HDLC nibble*, and *transparent*	Output	**FCC2: Request to Send** One of the standard modem interface signals supported by FCC2 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$). $\overline{\text{RTS}}$ is asynchronous with the data. $\overline{\text{RTS}}$ is typically used in conjunction with $\overline{\text{CD}}$. The MSC8101 FCC2 transmitter requests the receiver to send data by asserting $\overline{\text{RTS}}$ low. The request is accepted when $\overline{\text{CTS}}$ is returned low.
	FCC2: RX_ER *MII*	Input	**FCC2: Media Independent Interface Receive Error** Asserted by an external fast Ethernet PHY to indicate a receive error, which often indicates bad wiring.
	SCC2: $\overline{\text{RTS}}$, TENA	Output	**SCC2: Request to Send, Transmit Enable** Typically used in conjunction with $\overline{\text{CD}}$ supported by SCC2. The MSC8101 SCC2 transmitter requests the receiver to send data by asserting $\overline{\text{RTS}}$ low. The request is accepted when $\overline{\text{CTS}}$ is returned low. TENA is the signal used in Ethernet mode.
	SI2 TDMB2: L1TSYNC *TDM serial*	Input	**Time-Division Multiplexing B2: Layer 1 Transmit Synchronization** The synchronizing signal for the transmit channel. See the serial interface with time-slot assigner chapter in the *MSC8101 Reference Manual*.
PB27	FCC2: COL *MII*	Input	**FCC2: Media Independent Interface Collision Detect** Asserted by an external fast Ethernet PHY when a collision is detected.
	SI2 TDMC2: L1TXD *TDM serial*	Output	**Time-Division Multiplexing C2: Layer 1 Transmit Data** TDMC2 transmits serial data out of L1TXD.
PB26	FCC2: CRS *MII*	Input	**FCC2: Media Independent Interface Carrier Sense Input** Asserted by an external fast Ethernet PHY to indicate activity on the cable.
	SI2 TDMC2: L1RXD *TDM serial*	Input	**Time-Division Multiplexing C2: Layer 1 Receive Data** TDMC2 receives serial data from L1RXD.
PB25	FCC2: TXD3 *MII* and *HDLC nibble*	Output	**FCC2: MII and HDLC Nibble Transmit Data Bit 3** TXD3 is bit 3 and the most significant bit of the transmit data nibble.
	SI1 TDMA1: L1TXD3 *TDM nibble*	Output	**Time-Division Multiplexing A1: Nibble Layer 1 Transmit Data Bit 3** L1TXD3 is bit 3 and the most significant bit of the transmit data nibble.
	SI2 TDMC2: L1TSYNC *TDM serial*	Input	**Time-Division Multiplexing C2: Layer 1 Transmit Synchronization** The synchronizing signal for the transmit channel. See the *Serial Interface with Time-Slot Assigner* chapter in the *MSC8101 Reference Manual*.
PB24	FCC2: TXD2 *MII* and *HDLC nibble*	Output	**FCC2: MII and HDLC Nibble: Transmit Data Bit 2** TXD2 is bit 2 of the transmit data nibble.
	SI1 TDMA1: L1RXD3 *nibble*	Input	**Time-Division Multiplexing A1: Nibble Layer 1 Receive Data Bit 3** L1RXD3 is bit 3 and the most significant bit of the receive data nibble.
	SI2 TDMC2: L1RSYNC *serial*	Input	**Time-Division Multiplexing C2: Layer 1 Receive Synchronization** The synchronizing signal for the receive channel.

Table 1-9. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC24	BRG8O	Output	**Baud-Rate Generator 8 Output** The CPM supports up to 8 BRGs used internally by the bank-of-clocks selection logic and/or to provide an output to one of the 8 BRG pins.
	CLK8	Input	**Clock 8** The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	TIN3	Input	**Timer Input 3** A timer can have one of the following sources: another timer, system clock, system clock divided by 16, or a timer input. The CPM supports up to four timer inputs. The timer inputs can be captured on the rising, falling, or both edges.
	Timer4: $\overline{\text{TOUT4}}$	Output	**Timer 4: Timer Out 4** The timers (Timer1–4]) can output a signal on a timer output ($\overline{\text{TOUT}}$[1–4]) when the reference value is reached. This signal can be an active-low pulse or a toggle of the current output. The output can also be connected internally to the input of another timer, resulting in a 32-bit timer.
	DMA: DREQ2	Input	**DMA: Data Request 2** $\overline{\text{DACK2}}$, DREQ2, $\overline{\text{DRACK2}}$, and $\overline{\text{DONE2}}$ belong to the SIU DMA controller. $\overline{\text{DONE2}}$ and $\overline{\text{DRACK2}}$ are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports.
PC23	CLK9	Input	**Clock 9** The CPM supports up to 10 clock input pins sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	DMA: $\overline{\text{DACK1}}$	Output	**DMA: Data Acknowledge 1** $\overline{\text{DACK1}}$, DREQ1, $\overline{\text{DRACK1}}$, and $\overline{\text{DONE1}}$ belong to the SIU DMA controller. $\overline{\text{DONE1}}$ and $\overline{\text{DRACK1}}$ are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports.
	EXT2	Input	**External Request 2** External request input line 2 asserts an internal request to the CPM processor. The signal can be programmed as level- or edge-sensitive, and also has programmable priority. Refer to the risc controller configuration register (RCCR) description in the Chapter 17 of the *MSC8101 Reference Manual* for programming information. There are no current microcode applications for this request line. It is reserved for future development.

2.5 Clock Configuration

The following sections provide a general description of clock configuration.

2.5.1 Valid Clock Modes

Table 2-6 shows the maximum frequency values for each rated core frequency (250, 275, or 300 MHz). The user must ensure that maximum frequency values are not exceeded.

Table 2-6. Maximum Frequencies

Characteristic	Maximum Frequency in MHz		
Core Frequency	250	275	300
CPM Frequency (CPMCLK)	166.67	183.33	200
Bus Frequency (BCLK)	83.33	91.67	100
Serial Communication Controller Clock Frequency (SCLK)	83.33	91.67	100
Baud Rate Generator Clock Frequency (BRGCLK)	83.33	91.67	100
External Clock Output Frequency (CLKOUT)	83.33	91.67	100

Six bit values map the MSC8101 clocks to one of the valid configuration mode options. Each option determines the CLKIN, SC140, system bus, SCC clock, CPM, and CLKOUT frequencies. The six bit values are derived from three dedicated input pins (MODCK[1–3]) and three bits from the hard reset configuration word (MODCK_H). To configure the SPLL pre-division factor, SPLL multiplication factor, and the frequencies for the SC140, SCC clocks, CPM parallel I/O ports, and system buses, the MODCK[1–3] pins are sampled and combined with the MODCK_H values when the internal power-on reset (internal $\overline{\text{PORESET}}$) is deasserted. Clock configuration changes only when the internal $\overline{\text{PORESET}}$ signal is deasserted. The following factors are configured:

- SPLL pre-division factor (SPLL PDF)
- SPLL multiplication factor (SPLL MF)
- Bus post-division factor (Bus DF)
- CPM division factor (CPM DF)
- Core division factor (Core DF)
- CPLL pre-division factor (CPLL PDF)
- CPLL multiplication factor (CPLL MF)

The SCC division factor (SCC DF) is fixed at 4. The BRG division factor (BRG DF) is configured through the System Clock Control Register (SCCR) and can be 4, 16 (default after reset), 64, or 256.

Note: Refer to *Clock Mode Selection for MSC8101 and MSC8103 Mask Set 2K87M* (AN2306) for details on clock configuration.

2.5.2 Clocks Programming Model

This section describes the clock registers in detail. The registers discussed are as follows:

- System Clock Control Register (SCCR)
- System Clock Mode Register (SCMR)

Table 2-16. AC Timing for SIU Inputs

No.	Characteristic	Value[2]	Units
11g	$\overline{TS}$ set-up time before the 50% level of the DLLIN rising edge	5.0	ns
11h	$\overline{BG}$ set-up time before the 50% level of the DLLIN rising edge	4.5	ns
12	Data bus set-up time before the 50% level of the DLLIN rising edge in Normal • Pipeline mode • Non-pipeline mode	 2.5 5.0	 ns ns
13	Data bus set-up time before the 50% level of the DLLIN rising edge in ECC and PARITY modes • Pipeline mode • Non-pipeline mode	 2.5 8.0	 ns ns
14	DP set-up time before the 50% level of the DLLIN rising edge • Pipeline mode • Non-pipeline mode	 4.0 9.0	 ns ns
15a	Address bus set-up time before the 50% level of the DLLIN rising edge • Extra cycle mode (SIUBCR[EXDD] = 0) • Non-extra cycle mode (SIUBCR[EXDD] = 1)	 5.0 8.0	 ns ns
15b	Address attributes: TT/$\overline{TBST}$/TSIZ/$\overline{GBL}$ set-up time before the 50% level of the DLLIN rising edge • Extra cycle mode (SIUBCR[EXDD] = 0) • Non-extra cycle mode (SIUBCR[EXDD] = 1)	 5.0 5.5	 ns ns
16[1]	PUPMWAIT/$\overline{IRQ}$ signals set-up time before the 50% level of the DLLIN rising edge	3.0	ns

Notes: **1.** The set-up time for these signals is for synchronous operation. Any set-up time can be used for asynchronous operation.
2. Input specifications are measured from the 50% level of the rising edge of DLLIN to the 50% level of the signal. Timings are measured at the pin.

Table 2-17. AC Timing for SIU Outputs

No.	Characteristic	Min.	Maximum[2]		Units
			30 pF	50 pF	
31a	$\overline{TA}$ delay from the 50% level of the DLLIN rising edge • Pipeline mode • Non-pipeline mode	 1.0 1.0	 5.0 4.0	 6.5 5.5	 ns ns
31b	$\overline{TEA}$ delay from the 50% level of the DLLIN rising edge • Pipeline mode • Non-pipeline mode	 1.0 1.0	 3.0 3.5	 4.5 5.0	 ns ns
31c	$\overline{PSDVAL}$ delay from the 50% level of the DLLIN rising edge • Pipeline mode • Non-pipeline mode	 1.0 1.0	 4.0 3.5	 5.5 5.0	 ns ns
32a	Address bus delay from the 50% level of the DLLIN rising edge • Multi master mode (SIUBCR[EBM] = 1) • Single master mode (SIUBCR[EBM] = 0)	 1.0 1.0	 6.3 5.5	 7.8 7.0	 ns ns
32b	Address attributes: TT/$\overline{TBST}$/TSIZ/$\overline{GBL}$ delay from the 50% level of the DLLIN rising edge	1.0	5.5	7.0	ns
32c	BADDR delay from the 50% level of the DLLIN rising edge	1.0	3.5	5.0	ns
33a	Data bus delay from the 50% level of the DLLIN rising edge • Pipeline mode • Non-pipeline mode	 1.0 1.0	 5.0 6.0	 6.5 7.5	 ns ns
33b	DP delay from the 50% level of the DLLIN rising edge • Pipeline mode • Non-pipeline mode	 1.0 1.0	 4.0 6.5	 5.5 8.0	 ns ns
34	Memory controller signals/ALE delay from the 50% level of the DLLIN rising edge	1.0	5.5	7.0	ns
35a	$\overline{DBG}$/$\overline{BR}$/$\overline{DBB}$ delay from the 50% level of the DLLIN rising edge	1.0	4.0	5.5	ns
35b	$\overline{AACK}$/$\overline{ABB}$/$\overline{CS}$ delay from the 50% level of the DLLIN rising edge	1.0	4.5	6.0	ns

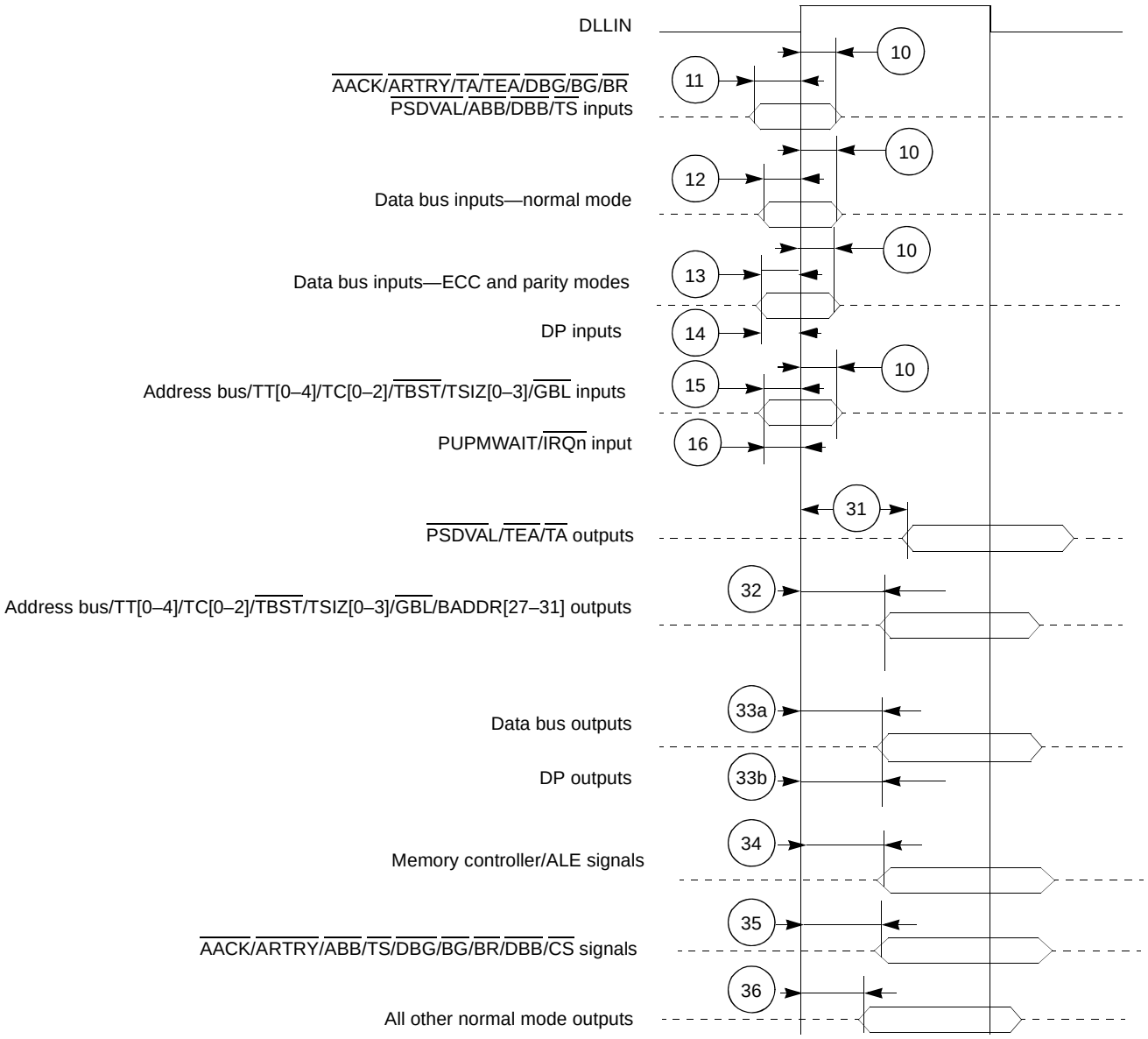


Figure 2-10. Bus Signal Timing

Figure 2-17 shows Host DMA write timing.

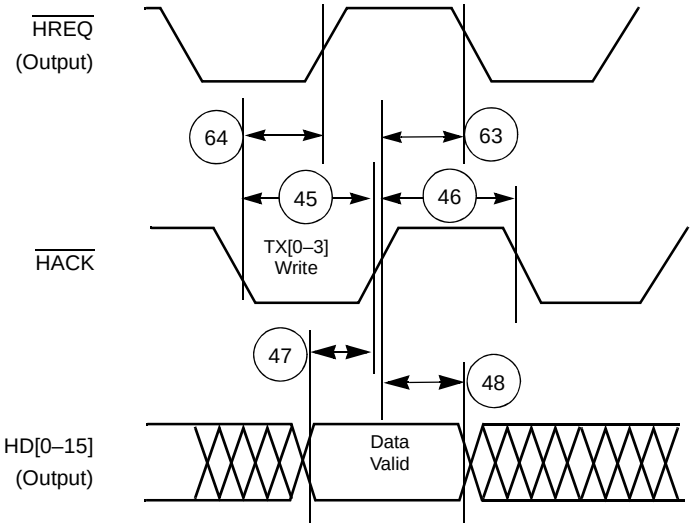


Figure 2-17. Host DMA Write Timing Diagram, HPCR[OAD] = 0

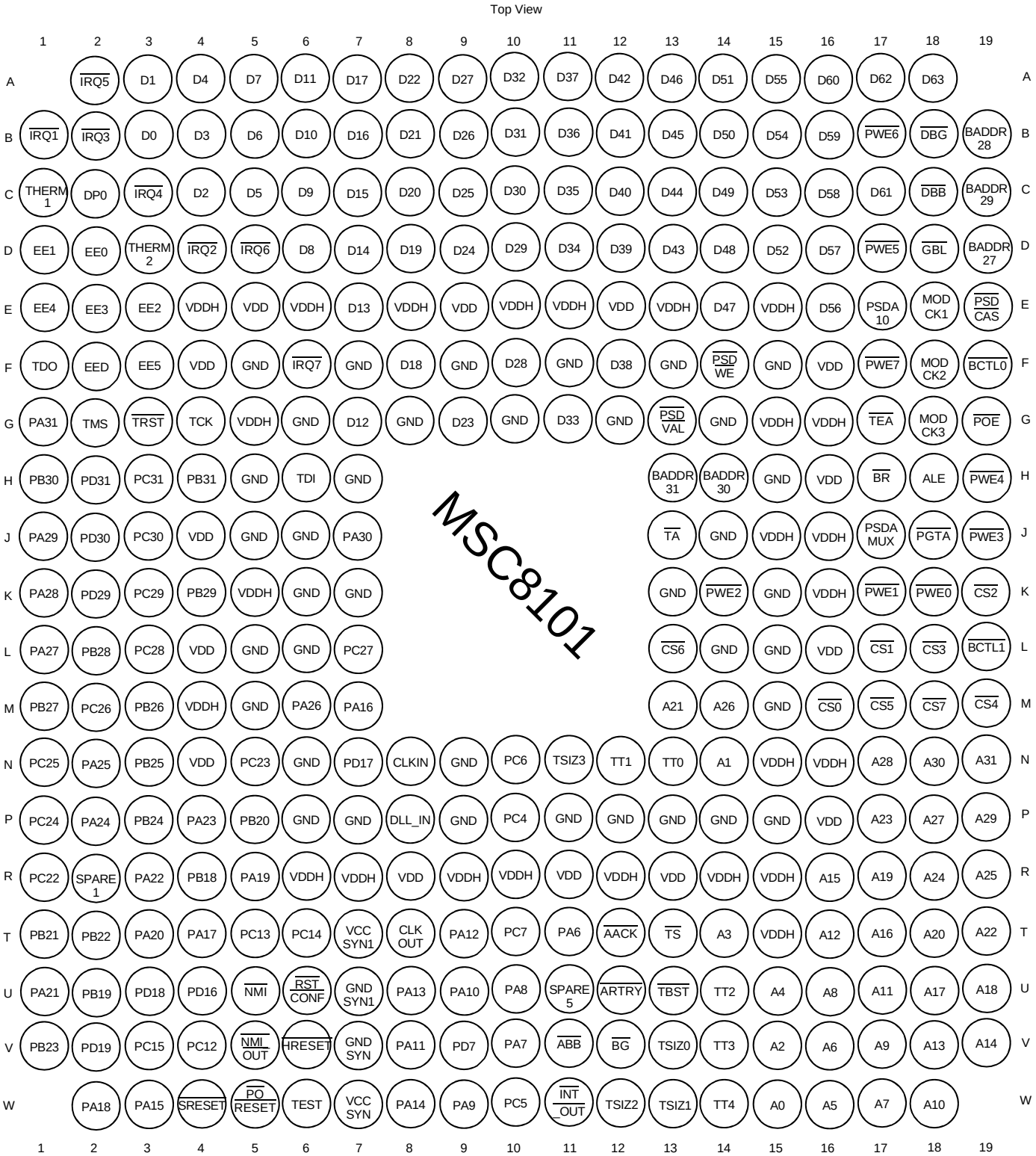
2.6.7 CPM Timings

Table 2-20. CPM Input Characteristics

No.	Characteristic	Typical	Unit
39	FCC input set-up time before low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial clock input)	 10 5	 ns ns
17	FCC input hold time after low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial clock input)	 0 3	 ns ns
18	SCC/SMC/SPI/I^2C input set-up time before low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial clock input)	 20 5	 ns ns
19	SCC/SMC/SPI/I^2C input hold time after low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial clock input)	 0 5	 ns ns
20	TDM input set-up time before low-to-high serial clock transition	5	ns
21	TDM input hold time after low-to-high serial transition	5	ns
22	PIO/TIMER/DMA input set-up time before low-to-high serial clock transition	10	ns
23	PIO/TIMER/DMA input hold time after low-to-high serial clock transition	3	ns
Note:	FCC, SCC, SMC, SPI, I^2C are Non-Multiplexed Serial Interface signals.		

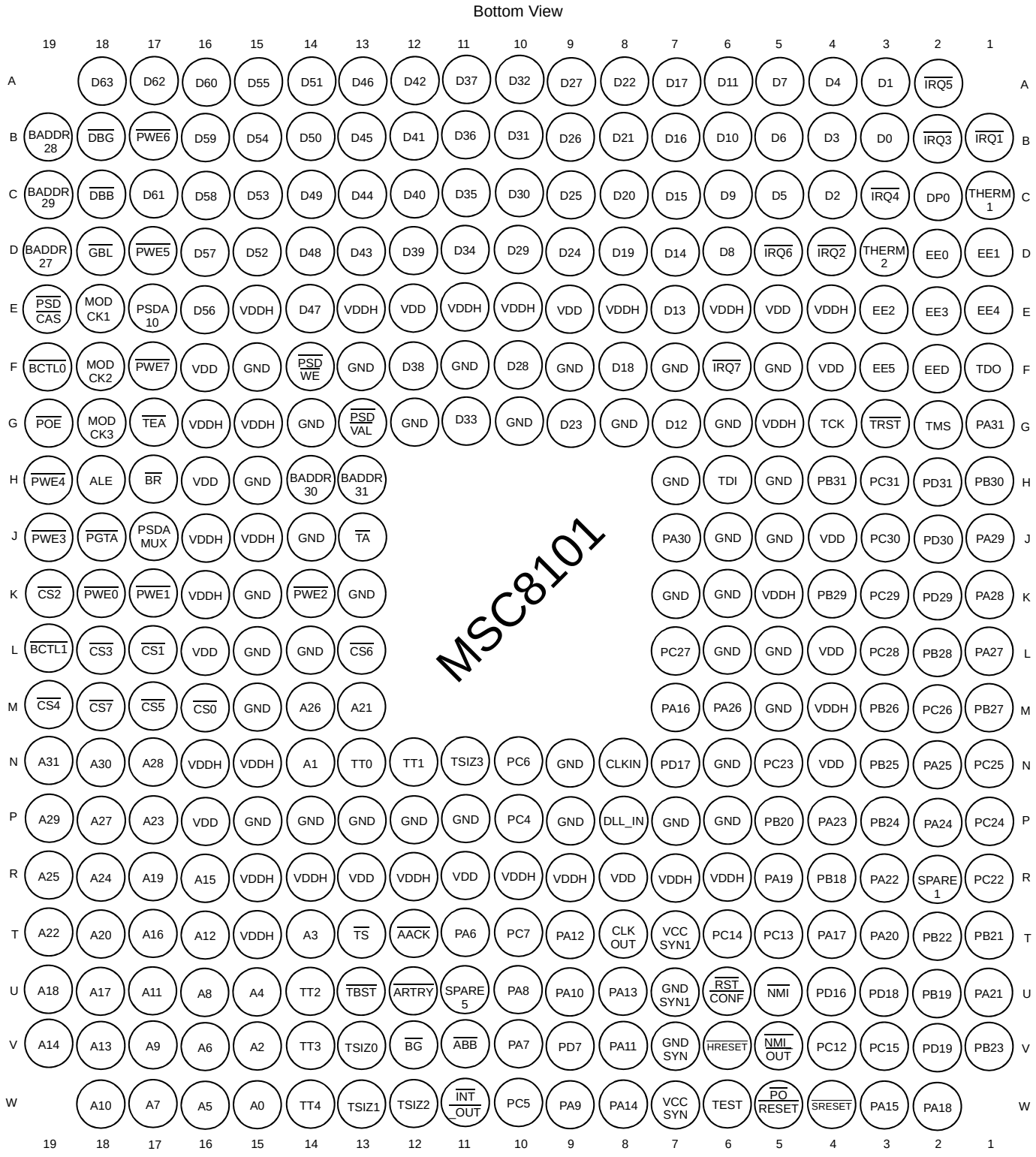
Table 2-21. CPM Output Characteristics

No.	Characteristic	Min	Max	Unit
41	FCC output delay after low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial input clock)	 0 2	 6 18	 ns ns



Note: Signal names in this figure are the default signals after reset, except for signals C2, C19, D1, D2, D18, E1, F3, H13, H14, and W11 which show the second configuration signal name.

Figure 3-1. MSC8101 Flip Chip Plastic Ball Grid Array (FC-PBGA), Top View



Note: Signal names in this figure are the default signals after reset, except for signals C2, C19, D1, D2, D18, E1, F3, H13, H14, and W11 which show the second configuration signal name.

Figure 3-2. MSC8101 Flip Chip Plastic Ball Grid Array (FC-PBGA), Bottom Vie

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
GND	G14
GND	G6
GND	G8
GND	H15
GND	H5
GND	H7
GND	J14
GND	J5
GND	J6
GND	K13
GND	K15
GND	K6
GND	K7
GND	L14
GND	L15
GND	L5
GND	L6
GND	M15
GND	M5
GND	N6
GND	N9
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	P6
GND	P7
GND	P9
GND_{SYN}	V7
GND_{SYN1}	U7
H8BIT	B16
HA0	D14
HA1	C14

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
HA2	B14
HA3	A14
$\overline{\text{HACK}}$/HACK	E16
$\overline{\text{HCS1}}$/HCS1	D15
$\overline{\text{HCS2}}$/HCS2	A16
HD0	A10
HD1	G11
HD2	D11
HD3	C11
HD4	B11
HD5	A11
HD6	F12
HD7	D12
HD8	C12
HD9	B12
HD10	A12
HD11	D13
HD12	C13
HD13	B13
HD14	A13
HD15	E14
HDDS	C16
$\overline{\text{HDS}}$/HDS	B15
HDSP	D16
HPE	D1
$\overline{\text{HRD}}$/HRD	C15
$\overline{\text{HREQ}}$/HREQ	A15
HRESET	V6
$\overline{\text{HRRQ}}$/HRRQ	E16
HRW	C15
$\overline{\text{HTRQ}}$/HTRQ	A15
$\overline{\text{HWR}}$/HWR	B15
$\overline{\text{INT\_OUT}}$	W11
$\overline{\text{IRQ1}}$	B1

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
$\overline{\text{PBS6}}$	B17
$\overline{\text{PBS7}}$	F17
PC4	P10
PC5	W10
PC6	N10
PC7	T10
PC12	V4
PC13	T5
PC14	T6
PC15	V3
PC22	R1
PC23	N5
PC24	P1
PC25	N1
PC26	M2
PC27	L7
PC28	L3
PC29	K3
PC30	J3
PC31	H3
PD7	V9
PD16	U4
PD17	N7
PD18	U3
PD19	V2
PD29	K2
PD30	J2
PD31	H2
PGPL0	E17
PGPL1	F14
PGPL2	G19
PGPL3	E19
PGPL4	J18
PGPL5	J17

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
TXCLAV0 for FCC1 UTOPIA 8	J7
TXCLAV1 for FCC1 UTOPIA 8	T10
TXCLAV2 for FCC1 UTOPIA 8	V9
TXCLAV3 for FCC1 UTOPIA 8	V2
TXD for FCC1 transparent/HDLC serial	W2
TXD for FCC2 transparent/HDLC serial	T2
TXD for SCC1	J2
TXD for SCC2	H1
TXD0 for FCC1 MII/HDLC nibble	W2
TXD0 for FCC1 UTOPIA 8	N2
TXD0 for FCC2 MII/HDLC nibble	T2
TXD1 for FCC1 MII/HDLC nibble	R5
TXD1 for FCC1 UTOPIA 8	P2
TXD1 for FCC2 MII/HDLC nibble	V1
TXD2 for FCC1 MII/HDLC nibble	T3
TXD2 for FCC1 UTOPIA 8	P4
TXD2 for FCC2 MII/HDLC nibble	P3
TXD3 for FCC1 MII/HDLC nibble	U1
TXD3 for FCC1 UTOPIA 8	R3
TXD3 for FCC2 MII/HDLC nibble	N3
TXD4 for FCC1 UTOPIA 8	U1
TXD5 for FCC1 UTOPIA 8	T3
TXD6 for FCC1 UTOPIA 8	R5
TXD7 for FCC1 UTOPIA 8	W2
$\overline{\text{TXENB}}$ for FCC1	G1
TXPRTY for FCC1 UTOPIA 8	U4
TXSOC for FCC1	J1
V_{CCSYN}	W7
V_{CCSYN1}	T7
V_{DD}	E12
V_{DD}	E5
V_{DD}	E9
V_{DD}	F16
V_{DD}	F4

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
V_{DD}	H16
V_{DD}	J4
V_{DD}	L16
V_{DD}	L4
V_{DD}	N4
V_{DD}	P16
V_{DD}	R11
V_{DD}	R13
V_{DD}	R8
V_{DDH}	E10
V_{DDH}	E11
V_{DDH}	E13
V_{DDH}	E15
V_{DDH}	E4
V_{DDH}	E6
V_{DDH}	E8
V_{DDH}	G15
V_{DDH}	G16
V_{DDH}	G5
V_{DDH}	J15
V_{DDH}	J16
V_{DDH}	K16
V_{DDH}	K5
V_{DDH}	M4
V_{DDH}	N15
V_{DDH}	N16
V_{DDH}	R10
V_{DDH}	R12
V_{DDH}	R14
V_{DDH}	R15
V_{DDH}	R6
V_{DDH}	R7
V_{DDH}	R9
V_{DDH}	T15

3.2 Lidded FC-PBGA Package Mechanical Drawing

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M–1994.
2. Dimensions in millimeters.
3. Maximum solder ball diameter measured parallel to Datum A.
4. Primary Datum A and the seating plane are defined by the spherical crowns of the solder balls.

CASE 1473-01

Figure 3-3. Case 1473-01 Mechanical Information, 332-pin Lidded FC-PBGA Package