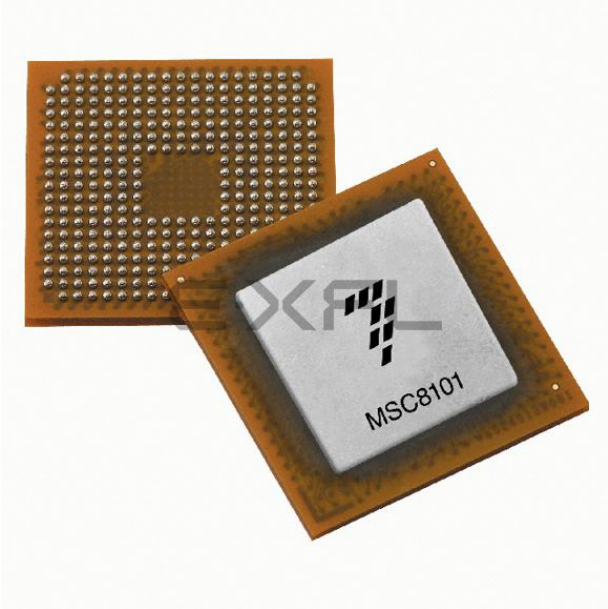

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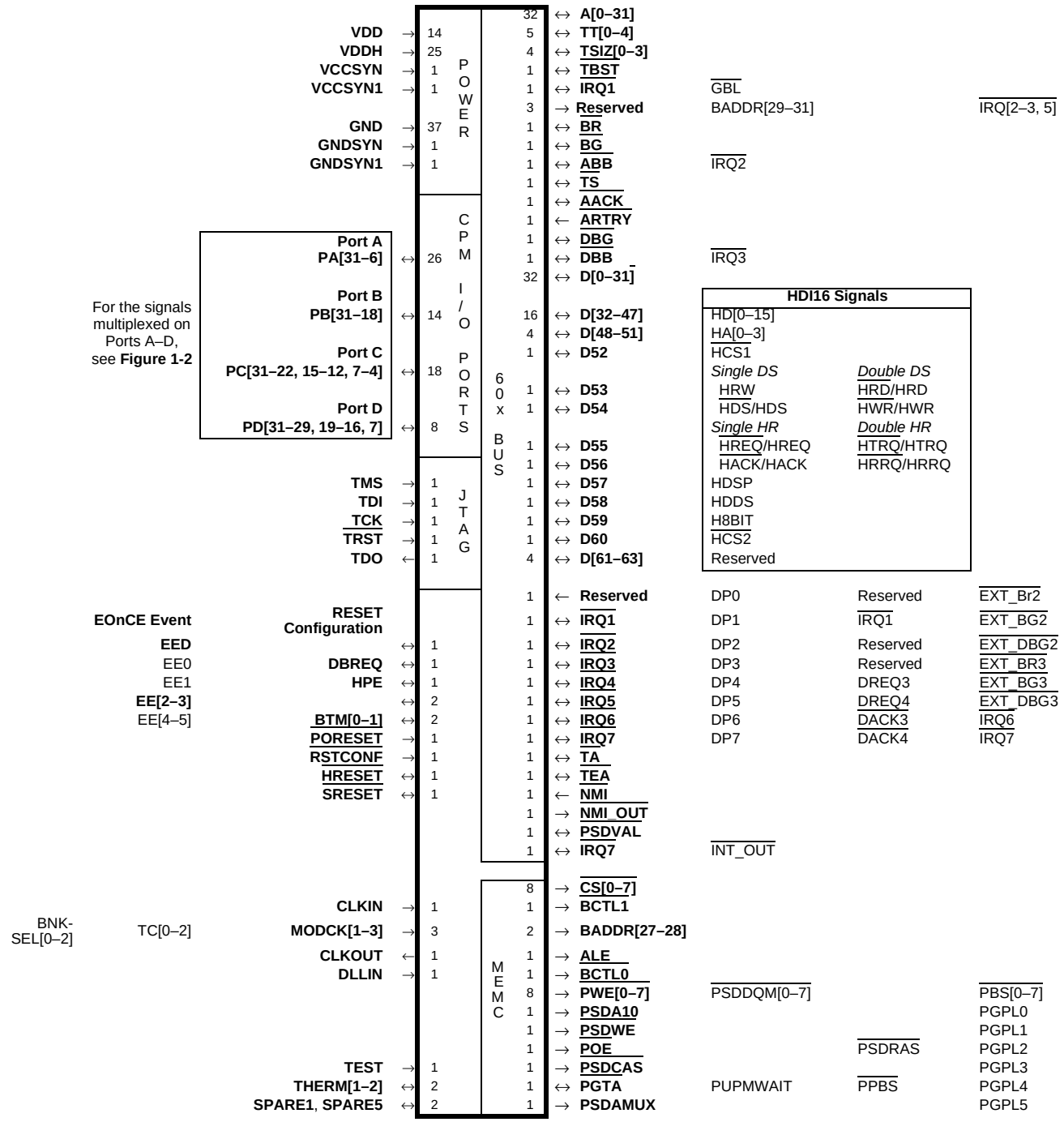
Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC140 Core
Interface	Communications Processor Module (CPM)
Clock Rate	300MHz
Non-Volatile Memory	External
On-Chip RAM	512kB
Voltage - I/O	3.30V
Voltage - Core	1.60V
Operating Temperature	-40°C ~ 75°C (TJ)
Mounting Type	Surface Mount
Package / Case	332-BFBGA, FCBGA
Supplier Device Package	332-FCBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8101vt1500f



Note: Refer to the *System Interface Unit (SIU)* chapter in the *MSC8101 Reference Manual* for details on how to configure these pins.

Figure 1-1. MSC8101 External Signals

Table 1-7. Port A Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	Peripheral Controller: Dedicated Signal *Protocol*		
PA7	SMC2: $\overline{\text{SMSYN}}$	Input	**SMC2: Serial Management Synchronization** The SMC interface consists of SMTXD, SMRXD, SMSYN, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent, or general-circuit interface (GCI).
	SI1 TDMA1: L1TSYNC *TDM nibble* and *TDM serial*	Input	**Time-Division Multiplexing A1: Layer 1 Transmit Synchronization** The synchronizing signal for the transmit channel. See the *Serial Interface with* time-slot assigner chapter in the *MSC8101 Reference Manual*.
PA6	SI1 TDMA1: L1RSYNC *TDM nibble* and *TDM serial*	Input	**Time-Division Multiplexing A1: Layer 1 Receive Synchronization.** The synchronizing signal for the receive channel.

1.6.2 Port B Signals

Table 1-8. Port B Signals

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	Peripheral Controller: Dedicated I/O *Protocol*		
PB31	FCC2: TX_ER *MII*	Output	**FCC2: Media Independent Interface Transmit Error** Asserted by the MSC8101 to force propagation of transmit errors.
	SCC2: RXD	Input	**SCC2: Receive Data** SCC2 receives serial data from RXD.
	SI2 TDMB2: L1TXD *TDM serial*	Output	**Time-Division Multiplexing B2: Layer 1 Transmit Data** TDMB2 transmits serial data out of L1TXD.
PB30	SCC2: TXD	Output	**SCC2: Transmit Data.** SCC2 transmits serial data out of TXD.
	FCC2: RX_DV *MII*	Input	**FCC2: Media Independent Interface Receive Data Valid** Asserted by an external fast Ethernet PHY to indicate that valid data is being sent. The presence of carrier sense, but not RX_DV, indicates reception of broken packet headers, probably due to bad wiring or a bad circuit.
	SI2 TDMB2: L1RXD *TDM serial*	Input	**Time-Division Multiplexing B2: Layer 1 Receive Data** TDMB2 receives serial data from L1RXD.
PB29	FCC2: TX_EN *MII*	Output	**FCC2: Media Independent Interface Transmit Enable** Asserted by the MSC8101 when transmitting data.
	SI2 TDMB2: L1RSYNC *TDM serial*	Input	**Time-Division Multiplexing B2: Layer 1 Receive Synchronization** The synchronizing signal for the receive channel.

Table 1-8. Port B Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	Peripheral Controller: Dedicated I/O *Protocol*		
PB28	FCC2: $\overline{\text{RTS}}$ *HDLC serial*, *HDLC nibble*, and *transparent*	Output	**FCC2: Request to Send** One of the standard modem interface signals supported by FCC2 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$). $\overline{\text{RTS}}$ is asynchronous with the data. $\overline{\text{RTS}}$ is typically used in conjunction with $\overline{\text{CD}}$. The MSC8101 FCC2 transmitter requests the receiver to send data by asserting $\overline{\text{RTS}}$ low. The request is accepted when $\overline{\text{CTS}}$ is returned low.
	FCC2: RX_ER *MII*	Input	**FCC2: Media Independent Interface Receive Error** Asserted by an external fast Ethernet PHY to indicate a receive error, which often indicates bad wiring.
	SCC2: $\overline{\text{RTS}}$, TENA	Output	**SCC2: Request to Send, Transmit Enable** Typically used in conjunction with $\overline{\text{CD}}$ supported by SCC2. The MSC8101 SCC2 transmitter requests the receiver to send data by asserting $\overline{\text{RTS}}$ low. The request is accepted when $\overline{\text{CTS}}$ is returned low. TENA is the signal used in Ethernet mode.
	SI2 TDMB2: L1TSYNC *TDM serial*	Input	**Time-Division Multiplexing B2: Layer 1 Transmit Synchronization** The synchronizing signal for the transmit channel. See the serial interface with time-slot assigner chapter in the *MSC8101 Reference Manual*.
PB27	FCC2: COL *MII*	Input	**FCC2: Media Independent Interface Collision Detect** Asserted by an external fast Ethernet PHY when a collision is detected.
	SI2 TDMC2: L1TXD *TDM serial*	Output	**Time-Division Multiplexing C2: Layer 1 Transmit Data** TDMC2 transmits serial data out of L1TXD.
PB26	FCC2: CRS *MII*	Input	**FCC2: Media Independent Interface Carrier Sense Input** Asserted by an external fast Ethernet PHY to indicate activity on the cable.
	SI2 TDMC2: L1RXD *TDM serial*	Input	**Time-Division Multiplexing C2: Layer 1 Receive Data** TDMC2 receives serial data from L1RXD.
PB25	FCC2: TXD3 *MII* and *HDLC nibble*	Output	**FCC2: MII and HDLC Nibble Transmit Data Bit 3** TXD3 is bit 3 and the most significant bit of the transmit data nibble.
	SI1 TDMA1: L1TXD3 *TDM nibble*	Output	**Time-Division Multiplexing A1: Nibble Layer 1 Transmit Data Bit 3** L1TXD3 is bit 3 and the most significant bit of the transmit data nibble.
	SI2 TDMC2: L1TSYNC *TDM serial*	Input	**Time-Division Multiplexing C2: Layer 1 Transmit Synchronization** The synchronizing signal for the transmit channel. See the *Serial Interface with Time-Slot Assigner* chapter in the *MSC8101 Reference Manual*.
PB24	FCC2: TXD2 *MII* and *HDLC nibble*	Output	**FCC2: MII and HDLC Nibble: Transmit Data Bit 2** TXD2 is bit 2 of the transmit data nibble.
	SI1 TDMA1: L1RXD3 *nibble*	Input	**Time-Division Multiplexing A1: Nibble Layer 1 Receive Data Bit 3** L1RXD3 is bit 3 and the most significant bit of the receive data nibble.
	SI2 TDMC2: L1RSYNC *serial*	Input	**Time-Division Multiplexing C2: Layer 1 Receive Synchronization** The synchronizing signal for the receive channel.

Table 1-8. Port B Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PB23	FCC2: TXD1 *MII* and *HDLC nibble*	Output	**FCC2: MII and HDLC Nibble: Transmit Data Bit 1** TXD1 is bit 1 of the transmit data nibble.
	SI1 TDMA1: L1RXD2 *TDM nibble*	Input	**Time-Division Multiplexing A1: Nibble Layer 1 Receive Data Bit 2** L1RXD2 is bit 2 of the receive data nibble.
	SI2 TDMD2: L1TXD *TDM serial*	Output	**Time-Division Multiplexing D2: Layer 1 Transmit Data** TDMA1 transmits serial data out of L1TXD.
PB22	FCC2: TXD0 *MII* and *HDLC nibble*	Output	**FCC2: MII and HDLC Nibble Transmit Data Bit 0** TXD0 is bit 0 and the least significant bit of the transmit data nibble.
	FCC2: TXD *HDLC serial* and *transparent*	Output	**FCC2: HDLC Serial and Transparent Transmit Data** Serial data is transmitted via TXD.
	SI1 TDMA1: L1RXD1 *TDM nibble*	Input	**Time-Division Multiplexing A1: Nibble Layer 1 Receive Data Bit 1** L1RXD1 is bit 1 of the receive data nibble.
	SI2 TDMD2: L1RXD *TDM serial*	Input	**Time-Division Multiplexing D2: Layer 1 Receive Data** Serial data is received via L1RXD.
PB21	FCC2: RXD0 *MII* and *HDLC nibble*	Input	**FCC2: MII and HDLC Nibble Receive Data Bit 0** RXD0 is bit 0 and the least significant bit of the receive data nibble.
	FCC2: RXD *HDLC serial* and *transparent*	Input	**FCC2: HDLC Serial and Transparent Receive Data** Serial data is received via RXD.
	SI1 TDMA1: L1TXD2 *TDM nibble*	Output	**Time-Division Multiplexing A1: Nibble Layer 1 Transmit Data Bit 2** L1TXD2 is bit 2 of the transmit data nibble.
	SI2 TDMD2: L1TSYNC *TDM serial*	Input	**Time-Division Multiplexing D2: Layer 1 Transmit Synchronize Data** The synchronizing signal for the transmit channel. See the *Serial Interface with Time-Slot Assigner* chapter in the *MSC8101 Reference Manual*.
PB20	FCC2: RXD1 *MII* and *HDLC nibble*	Input	**FCC2: MII and HDLC Nibble: Receive Data Bit 1** RXD1 is bit 1 of the receive data nibble.
	SI1 TDMA1: L1TXD1 *TDM nibble*	Output	**Time-Division Multiplexing A1: Nibble Layer 1 Transmit Data Bit 1** L1TXD1 is bit 1 of the transmit data nibble.
	SI2 TDMD2: L1RSYNC *TDM serial*	Input	**Time-Division Multiplexing D2: Layer 1 Receive Synchronize Data** The synchronizing signal for the receive channel.
PB19	FCC2: RXD2 *MII* and *HDLC nibble*	Input	**FCC2: MII and HDLC Nibble Receive Data Bit 2** RXD2 is bit 2 of the receive data nibble.
	I^2C: SDA	Input/ Output	**I^2C: Inter-Integrated Circuit Serial Data** The I^2C interface comprises two signals: serial data (SDA) and serial clock (SDA). The I^2C controller uses a synchronous, multimaster bus that can connect several integrated circuits on a board. Clock rates run up to 520 kHz@25 MHz system clock.

Table 1-9. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC30	BRG2O	Output	**Baud-Rate Generator 2 Output** The CPM supports up to 8 BRGs used internally by the bank-of-clocks selection logic and/or to provide an output to one of the 8 BRG pins.
	CLK2	Input	**Clock 2** The CPM supports up to 10 clock input pins sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	Timer1: $\overline{\text{TOUT1}}$	Output	**Timer 1: Timer Out 1** The timers (Timer[1–4]) can output a signal on a timer output ($\overline{\text{TOUT[1–4]}}$) when the reference value is reached. This signal can be an active-low pulse or a toggle of the current output. The output can also connect internally to the input of another timer, resulting in a 32-bit timer.
	EXT1	Input	**External Request 1** Asserts an internal request to the CPM processor. The signal can be programmed as level- or edge-sensitive, and also has programmable priority. Refer to the RISC Controller Configuration Register (RCCR) description in the Chapter 17 of the *MSC8101 Reference Manual* for programming information. There are no current microcode applications for this request line. It is reserved for future development.
PC29	BRG3O	Output	**Baud-Rate Generator 3 Output** The CPM supports up to 8 BRGs used internally by the bank-of-clocks selection logic and/or to provide an output to one of the 8 BRG pins.
	CLK3	Input	**Clock 3** The CPM supports up to 10 clock input pins sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	TIN2	Input	**Timer Input 2** A timer can have one of the following sources: another timer, system clock, system clock divided by 16 or a timer input. The CPM supports up to 4 timer inputs. The timer inputs can be captured on the rising, falling or both edges.
	SCC1: $\overline{\text{CTS}}$, CLSN	Input	**SCC1: Clear to Send, Collision** Typically used in conjunction with $\overline{\text{RTS}}$. The MSC8101 SCC1 transmitter sends out a request to send data signal ($\overline{\text{RTS}}$). The request is accepted when $\overline{\text{CTS}}$ is returned low. CLSN is the signal used in Ethernet mode. See also PC15.

2.4 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8101. The measurements in **Table 2-4** assume the following system conditions:

- T_J = 0 – 100 °C
- V_{DD} = 1.6 V ± 5% V_{DC}
- V_{DDH} = 3.3 V ± 5% V_{DC}
- GND = 0 V_{DC}

Note: The leakage current is measured for nominal V_{DDH} and V_{DD} or both V_{DDH} and V_{DD} must vary in the same direction (for example, both V_{DDH} and V_{DD} vary by ± 5 percent).

Table 2-4. DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Input high voltage[1], all inputs except CLKIN	V_{IH}	2.0	3.465	V
Input low voltage[1]	V_{IL}	GND	0.8	V
CLKIN input high voltage	V_{IHC}	2.5	3.465	V
CLKIN input low voltage[2]	V_{ILC}	GND	0.8	V
Input leakage current, V_{IN} = V_{DDH}	I_{IN}	—	10	µA
Tri-state (high impedance off state) leakage current, V_{IN} = V_{DDH}	I_{OZ}	—	10	µA
Signal low input current[3], V_{IL} = 0.8 V	I_L	—	–4.0	mA
Signal high input current[3], V_{IH} = 2.0 V	I_H	—	4.0	mA
Output high voltage, I_{OH} = –2 mA, except open drain pins	V_{OH}	2.4	—	V
Output low voltage, I_{OL}= 3.2 mA	V_{OL}	—	0.4	V

Notes:
1. See **Figure 2-1** for undershoot and overshoot voltages.
2. The optimum CLKIN duty cycle is obtained when: V_{ILC} = V_{DDH} – V_{IHC}.
3. Not tested. Guaranteed by design.

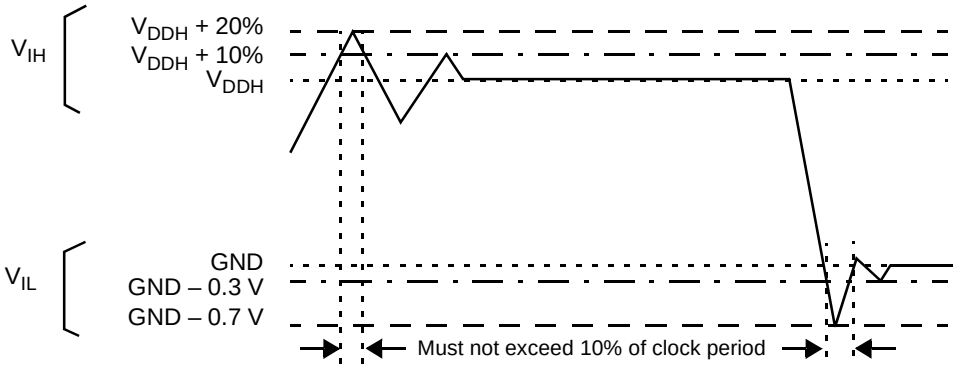


Figure 2-1. Overshoot/Undershoot Voltage for V_{IH} and V_{IL}

Table 2-5. Typical Power Dissipation

Characteristic	Symbol	Typical	Unit
Core power dissipation at 300 MHz	P_{CORE}	450	mW
CPM power dissipation at 200 MHz	P_{CPM}	320	mW
SIU power dissipation at 100 MHz	P_{SIU}	80	mW
Core leakage power	P_{LCO}	3	mW
CPM leakage power	P_{LCP}	6	mW
SIU leakage power	P_{LSI}	2	mW

2.5.2.1 System Clock Control Register

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	—															
Type	Reserved															
Reset	—															
Bit	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
	—											CLKODIS	—		DFBRG	
Type	Reserved											R/W	Reserved		R/W	
Reset	—											0	—		0	1

Figure 2-2. System Clock Control Register (SCCR)—**0x10C80**

SCCR is memory-mapped into the SIU register map of the MSC8101.

Table 2-7. SCCR Bit Descriptions

Name Bit No.	Defaults		Description	Settings
	POWERSET	Hard Reset		
— 0–26	—	—	Reserved. Write to 0 fro future compatibility.	
CLKODIS 27	0	Unaffected	**CLKOUT Disable** Disables the CLKOUT signal. The value of CLKOUT when disabled is indeterminate (can be 1 or 0).	0 CLKOUT enabled (default) 1 CLKOUT disabled
— 28–29	—	—	Reserved. Write to 0 fro future compatibility.	
DFBRG 30–31	01	Unaffected	**Division Factor for the BRG Clock** Defines the BRGCLK frequency. Changing this value does not result in a loss of lock condition.	00 Divide by 4 01 Divide by 16 (default value) 10 Divide by 64 11 Divide by 256

2.5.2.2 System Clock Mode Register

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	COREPDF				COREMF				BUSDF				CPMDF			
Type	R															
Reset	—															
Bit	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
	SPLLPDF				SPLLMF				—	DLLDIS	—		COREDF			
Type	R															
Reset	—															

Figure 2-3. System Clock Mode Register (SCMR)—**0x10C88**

SCMR is a read-only register that is updated during power-on reset (PORESET) and provides the mode control signals to the PLLs, DLL, and clock logic. This register reflects the currently defined configuration settings. For details of the available setting options, see *AN2306/D*.

2.6.5 System Bus Access Timing

2.6.5.1 Core Data Transfers

Generally, all MSC8101 bus and system output signals are driven from the rising edge of the reference clock (REFCLK), which is DLLIN. Memory controller signals, however, trigger on four points within a DLLIN cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge of DLLIN (and T3 at the falling edge), but the spacing of T2 and T4 depends on the PLL clock ratio selected, as **Table 2-15** shows.

Table 2-15. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of DLLIN)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 DLLIN	1/2 DLLIN	3/4 DLLIN
1:2.5	3/10 DLLIN	1/2 DLLIN	8/10 DLLIN
1:3.5	4/14 DLLIN	1/2 DLLIN	11/14 DLLIN

Figure 2-9 is a graphical representation of **Table 2-15**.

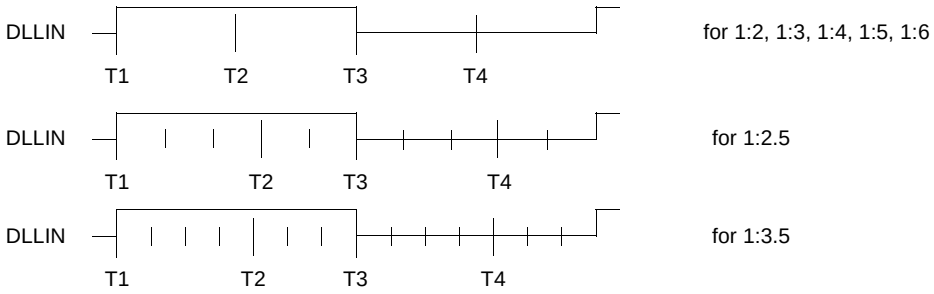


Figure 2-9. Internal Tick Spacing for Memory Controller Signals

Note: The UPM machine and GPCM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. SDRAM machine outputs change only on the DLLIN rising edge.

Table 2-16. AC Timing for SIU Inputs

No.	Characteristic	Value[2]	Units
10	Hold time for all signals after the 50% level of the DLLIN rising edge	0.5	ns
11a	$\overline{\text{ABB}}/\overline{\text{AACK}}$ set-up time before the 50% level of the DLLIN rising edge	3.5	ns
11b	$\overline{\text{DBG}}/\overline{\text{DBB}}/\overline{\text{BR}}/\overline{\text{TC}}$ set-up time before the 50% level of the DLLIN rising edge	5.0	ns
11c	$\overline{\text{ARTRY}}$ set-up time before the 50% level of the DLLIN rising edge	4.0	ns
11d	$\overline{\text{TA}}$ set-up time before the 50% level of the DLLIN rising edge • Pipeline mode • Non-pipeline mode	 3.5 4.0	 ns ns
11e	$\overline{\text{TEA}}$ set-up time before the 50% level of the DLLIN rising edge • Pipeline mode • Non-pipeline mode	 4.0 3.0	 ns ns
11f	$\overline{\text{PSDVAL}}$ set-up time before the 50% level of the DLLIN rising edge • Pipeline mode • Non-pipeline mode	 3.5 3.5	 ns ns

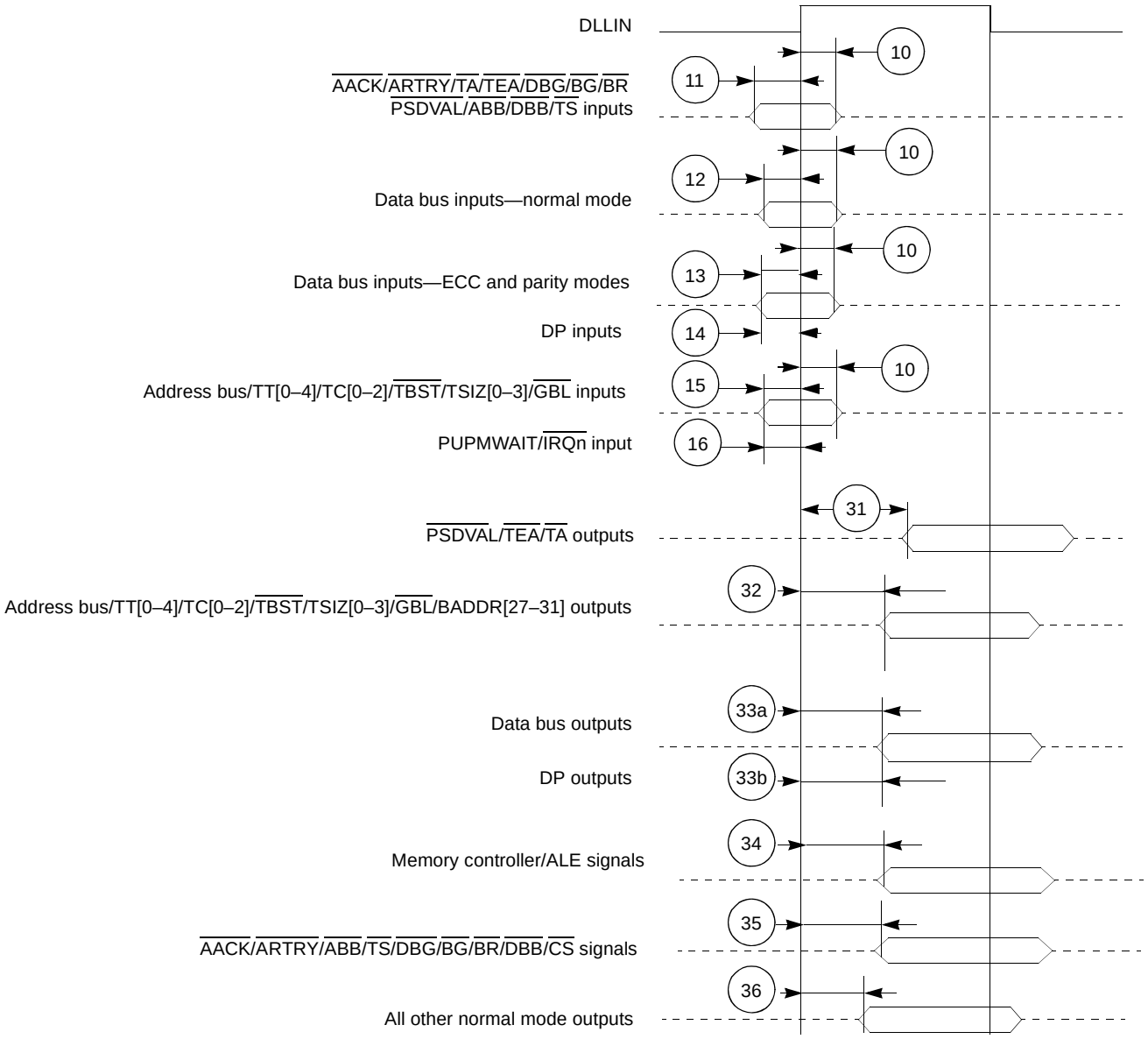


Figure 2-10. Bus Signal Timing

2.6.5.2 DMA Data Transfers

Table 2-18 describes the DMA signal timing.

Table 2-18. DMA Signals

Number	Characteristic	Minimum	Maximum	Units
72	DREQ set-up time before DLLIN falling edge	6	—	ns
73	DREQ hold time after DLLIN falling edge	0.5	—	ns
74	$\overline{\text{DONE}}$ set-up time before DLLIN rising edge	9	—	ns
75	$\overline{\text{DONE}}$ hold time after DLLIN rising edge	0.5	—	ns
76	$\overline{\text{DACK}}$/$\overline{\text{DRACK}}$/$\overline{\text{DONE}}$ delay after DLLIN rising edge	0.5	9	ns

The DREQ signal is synchronized with the falling edge of DLLIN. $\overline{\text{DONE}}$ timing is relative to the rising edge of DLLIN. To achieve fast response, a synchronized peripheral should assert DREQ according to the timings in **Table 2-18**. **Figure 2-11** shows synchronous peripheral interaction.

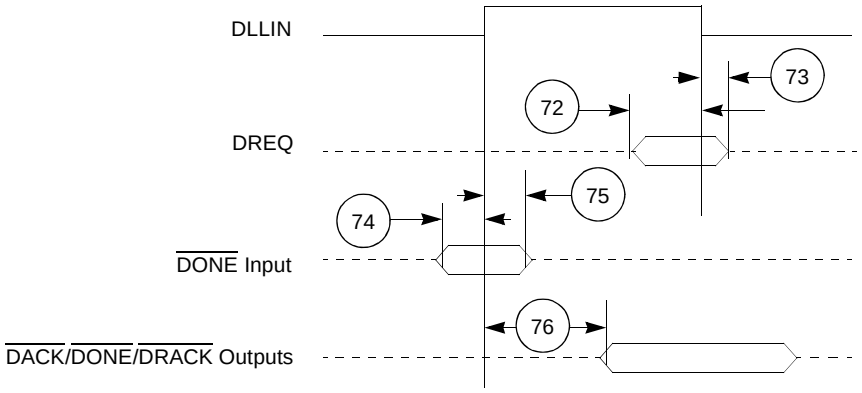


Figure 2-11. DMA Signals

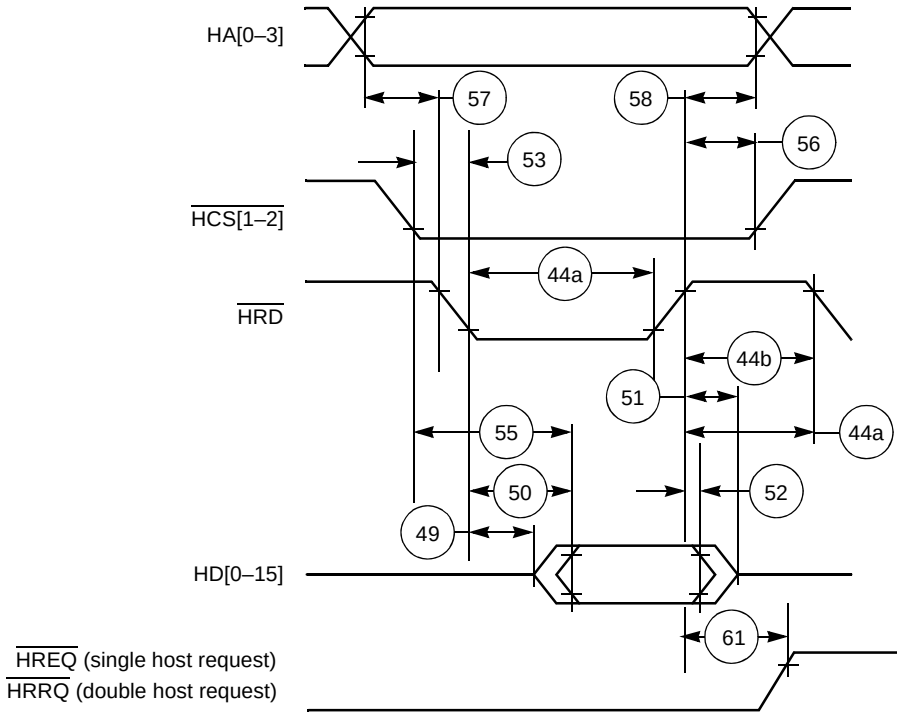


Figure 2-13. Read Timing Diagram, Double Data Strobe

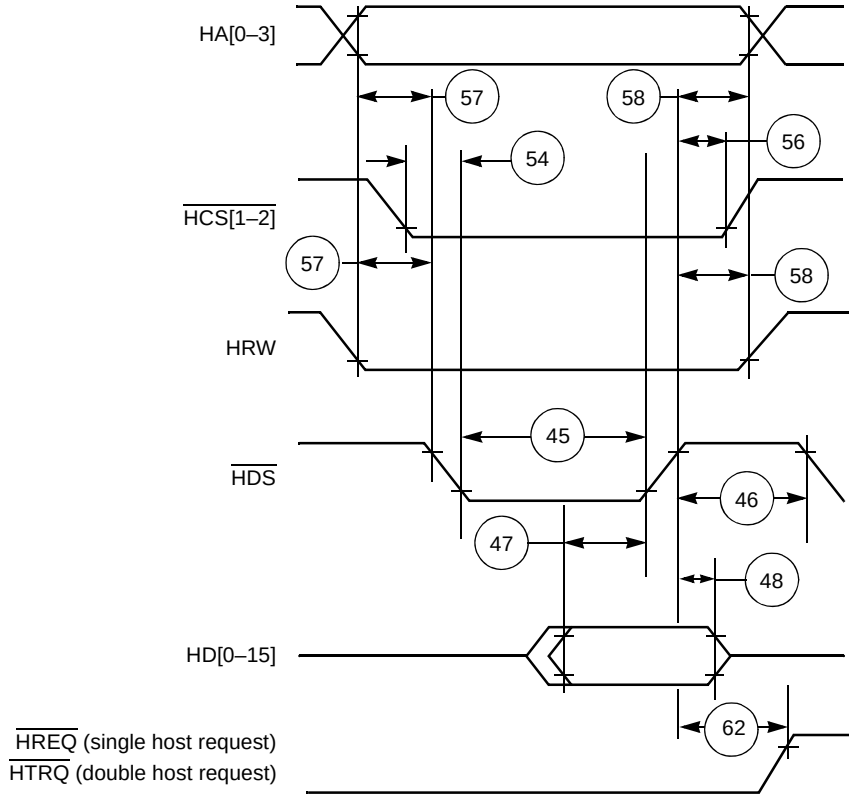


Figure 2-14. Write Timing Diagram, Single Data Strobe

Packaging 3

This chapter provides information about the MSC8101 package, including diagrams of the package pinouts and tables showing how the signals discussed in **Chapter 1** are allocated. The MSC8101 is available in a 332-pin lidded flip chip-plastic ball grid array (FC-PBGA).

3.1 FC-PBGA Package Description

Figure 3-1 and **Figure 3-2** show top and bottom views of the FC-PBGA package, including pinouts. **Table 3-1** lists the MSC8101 signals alphabetically by signal name. Connections with multiple names are listed individually by each name. Signals with programmable polarity are shown both as signals which are asserted low (default) and high (that is, $\overline{\text{NAME}}$/NAME). **Table 3-2** lists the signals numerically by pin number. Each pin number is listed once with the various signals that are multiplexed to it. For simplicity, signals with programmable polarity are shown in this table only with their default name (asserted low).

Note: The package description in this chapter applies to packages with lead-bearing and lead-free spheres.

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
GND	G14
GND	G6
GND	G8
GND	H15
GND	H5
GND	H7
GND	J14
GND	J5
GND	J6
GND	K13
GND	K15
GND	K6
GND	K7
GND	L14
GND	L15
GND	L5
GND	L6
GND	M15
GND	M5
GND	N6
GND	N9
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	P6
GND	P7
GND	P9
GND_{SYN}	V7
GND_{SYN1}	U7
H8BIT	B16
HA0	D14
HA1	C14

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
$\overline{\text{IRQ1}}$	D18
$\overline{\text{IRQ2}}$	C19
$\overline{\text{IRQ2}}$	D4
$\overline{\text{IRQ2}}$	V11
$\overline{\text{IRQ3}}$	B2
$\overline{\text{IRQ3}}$	C18
$\overline{\text{IRQ3}}$	H14
$\overline{\text{IRQ4}}$	C3
$\overline{\text{IRQ5}}$	A2
$\overline{\text{IRQ5}}$	H13
$\overline{\text{IRQ6}}$	D5
$\overline{\text{IRQ7}}$	F6
$\overline{\text{IRQ7}}$	W11
L1RSYNC for SI1 TDMA1	T11
L1RSYNC for SI2 TDMB2	K4
L1RSYNC for SI2 TDMC2	P3
L1RSYNC for SI2 TDMD2	P5
L1RXD for SI1 TDMA1 Serial	U10
L1RXD for SI2 TDMB2	H1
L1RXD for SI2 TDMC2	M3
L1RXD for SI2 TDMD2	T2
L1RXD0 for SI1 TDMA1 Nibble	U10
L1RXD1 for SI1 TDMA1 Nibble	T2
L1RXD2 for SI1 TDMA1 Nibble	V1
L1RXD3 for SI1 TDMA1 Nibble	P3
L1TSYNC for SI1 TDMA1	V10
L1TSYNC for SI2 TDMB2	L2
L1TSYNC for SI2 TDMC2	N3
L1TSYNC for SI2 TDMD2	T1
L1TXD for SI1 TDMA1 Serial	W9
L1TXD for SI2 TDMB2	H4
L1TXD for SI2 TDMC2	M1
L1TXD for SI2 TDMD2	V1
L1TXD0 for SI1 TDMA1 Nibble	W9

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
PA18	W2
PA19	R5
PA20	T3
PA21	U1
PA22	R3
PA23	P4
PA24	P2
PA25	N2
PA26	M6
PA27	L1
PA28	K1
PA29	J1
PA30	J7
PA31	G1
PB18	R4
PB19	U2
PB20	P5
PB21	T1
PB22	T2
PB23	V1
PB24	P3
PB25	N3
PB26	M3
PB27	M1
PB28	L2
PB29	K4
PB30	H1
PB31	H4
$\overline{\text{PBS0}}$	K18
$\overline{\text{PBS1}}$	K17
$\overline{\text{PBS2}}$	K14
$\overline{\text{PBS3}}$	J19
$\overline{\text{PBS4}}$	H19
$\overline{\text{PBS5}}$	D17

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
E5	V_{DD}
E6	V_{DDH}
E7	D13
E8	V_{DDH}
E9	V_{DD}
E10	V_{DDH}
E11	V_{DDH}
E12	V_{DD}
E13	V_{DDH}
E14	D47 / HD15
E15	V_{DDH}
E16	D56 / $\overline{\text{HACK}}$ / $\overline{\text{HRRQ}}$
E17	PSDA10 / PGPL0
E18	MODCK1 / TC0 / BNKSEL0
E19	$\overline{\text{PSDCAS}}$ / PGPL3
F1	TDO
F2	EED
F3	BTM1 / EE5
F4	V_{DD}
F5	GND
F6	$\overline{\text{IRQ7}}$ / DP7 / $\overline{\text{DACK4}}$
F7	GND
F8	D18
F9	GND
F10	D28
F11	GND
F12	D38 / HD6
F13	GND
F14	$\overline{\text{PSDWE}}$ / PGPL1
F15	GND
F16	V_{DD}
F17	$\overline{\text{PWE7}}$ / $\overline{\text{PSDDQM7}}$ / $\overline{\text{PBS7}}$
F18	MODCK2 / TC1 / BNKSEL1
F19	$\overline{\text{BCTL0}}$
G1	PA31 / FCC1:UTOPIA8:$\overline{\text{TXENB}}$ / FCC1:MII:COL
G2	TMS
G3	$\overline{\text{TRST}}$
G4	TCK
G5	V_{DDH}

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
G6	GND
G7	D12
G8	GND
G9	D23
G10	GND
G11	D33 / HD1
G12	GND
G13	$\overline{\text{PSDVAL}}$
G14	GND
G15	V_{DDH}
G16	V_{DDH}
G17	$\overline{\text{TEA}}$
G18	MODCK3 / TC2 / BNKSEL2
G19	$\overline{\text{POE}}$ / $\overline{\text{PSDRAS}}$ / PGPL2
H1	PB30 / FCC2:MII:RX_DV / SCC2:TXD / TDBM2:L1RXD
H2	PD31 / SCC1:RXD / $\overline{\text{DRACK1}}$ / $\overline{\text{DONE1}}$
H3	PC31 / BRG1O / CLK1 / $\overline{\text{TGATE1}}$
H4	PB31 / FCC2:MII:TX_ER / SCC2:RXD / TDMB2:L1TXD
H5	GND
H6	TDI
H7	GND
H13	Reserved / BADDR31 / $\overline{\text{IRQ5}}$
H14	Reserved / BADDR30 / $\overline{\text{IRQ3}}$
H15	GND
H16	V_{DD}
H17	$\overline{\text{BR}}$
H18	ALE
H19	$\overline{\text{PWE4}}$ / $\overline{\text{PSDDQM4}}$ / $\overline{\text{PBS4}}$
J1	PA29 / FCC1:UTOPIA8:TXSOC / FCC1:MII:TX_ER
J2	PD30 / SCC1:TXD / DMA:$\overline{\text{DRACK2}}$/$\overline{\text{DONE2}}$
J3	PC30 / EXT1 / BRG2O / CLK2 / $\overline{\text{TOUT1}}$
J4	V_{DD}
J5	GND
J6	GND
J7	PA30 / FCC1:UTOPIA8:TXCLAV / FCC1:UTOPIA8:$\overline{\text{TXCLAV0}}$ / FCC1:MII:CRS / FCC1:HDLC and transparent:RTS
J13	$\overline{\text{TA}}$
J14	GND
J15	V_{DDH}

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
V7	GND_{SYN}
V8	PA11 / FCC1:UTOPIA8:RXD1 / SDMA:MSNUM4
V9	PD7 / FCC1:UTOPIA8:TXADDR3 / FCC1:UTOPIA8:TXCLAV2 / SMC1:$\overline{\text{SMSYN}}$
V10	PA7 / SMC2:$\overline{\text{SMSYN}}$ / TDMA1:L1TSYNC
V11	$\overline{\text{ABB}}$ / $\overline{\text{IRQ2}}$
V12	$\overline{\text{BG}}$
V13	TSIZ0
V14	TT3
V15	A2
V16	A6
V17	A9
V18	A13
V19	A14
W2	PA18 / FCC1:UTOPIA8:TXD7 / FCC1:MII and HDLC nibble:TXD0 / FCC1:transparent and HDLC serial:TXD
W3	PA15 / FCC1:UTOPIA8:RXD5 / FCC1:MII and HDLC nibble:RXD2
W4	$\overline{\text{SRESET}}$
W5	$\overline{\text{PORESET}}$
W6	TEST
W7	V_{CCSYN}
W8	PA14 / FCC1:UTOPIA8 RXD4 / FCC1:MII and HDLC nibble:RXD3
W9	PA9 / SMC2:SMTXD / TDMA1:serial:L1TXD /TDMA1:nibble:L1TXD0
W10	PC5 / FCC2:$\overline{\text{CTS}}$ / SMC1:SMTXD / SI2:LIST3
W11	$\overline{\text{IRQ7}}$ / $\overline{\text{INT\_OUT}}$
W12	TSIZ2
W13	TSIZ1
W14	TT4
W15	A0
W16	A5
W17	A7
W18	A10