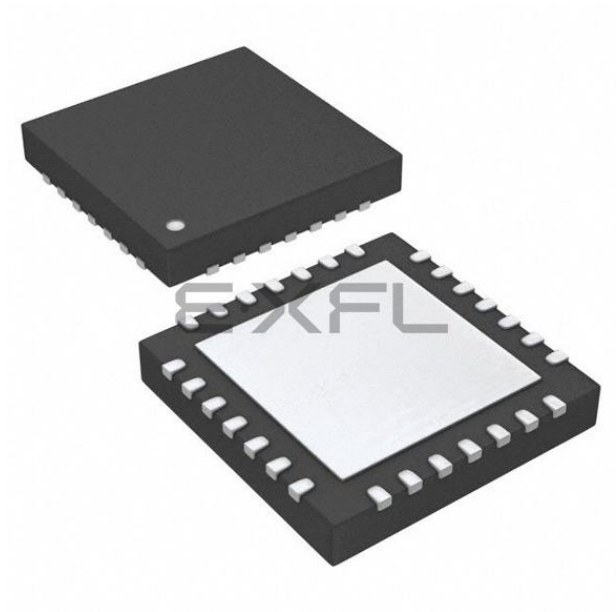

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18854-e-mv

TABLE 3-8: PIC16(L)F18854 MEMORY MAP, BANK 29

	Bank 29
E8Ch	—
E8Dh	—
E8Eh	—
E8Fh	PPSLOCK
E90h	INTPPS
E91h	T0CKIPPS
E92h	T1CKIPPS
E93h	T1GPPS
E94h	T3CKIPPS
E95h	T3GPPS
E96h	T5CKIPPS
E97h	T5GPPS
E98h	—
E99h	—
E9Ah	—
E9Bh	—
E9Ch	T2AINPPS
E9Dh	T4AINPPS
E9Eh	T6AINPPS
E9Fh	—
EA0h	—
EA1h	CCP1PPS
EA2h	CCP2PPS
EA3h	CCP3PPS
EA4h	CCP4PPS
EA5h	CCP5PPS
EA6h	—
EA7h	—
EA8h	—
EA9h	SMT1WINPPS
EAAh	SMT1SIGPPS
EABh	SMT2WINPPS
EACh	SMT2SIGPPS
EADh	—
EAEh	—
EAFh	—
EB0h	—

	Bank 29
EB1h	CWG1PPS
EB2h	CWG2PPS
EB3h	CWG3PPS
EB4h	—
EB5h	—
EB6h	—
EB7h	—
EB8h	MDCARLPPS
EB9h	MDCARHPPS
EBAh	MDSRCPPS
EBBh	CLCIN0PPS
EBCh	CLCIN1PPS
EBDh	CLCIN2PPS
EBEh	CLCIN3PPS
EBFh	—
EC0h	—
EC1h	—
EC2h	—
EC3h	ADCACTPPS
EC4h	—
EC5h	SSP1CLKPPS
EC6h	SSP1DATPPS
EC7h	SSP1SSPPS
EC8h	SSP2CLKPPS
EC9h	SSP2DATPPS
ECAh	SSP2SSPPS
ECBh	RXPPS
ECCh	TXPPS
ECDh – EEFh	—

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 3-11: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 4											
CPU CORE REGISTERS; see Table 3-2 for specifics											
20Ch	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								0000 0000	uuuu uuuu
20Dh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								0000 0000	uuuu uuuu
20Eh	T1CON	—	—	CKPS<1:0>		—	$\overline{\text{SYNC}}$	RD16	ON	--00 -000	--uu -uuu
20Fh	T1GCON	GE	GPOL	GTM	GSPM	GGO/$\overline{\text{DONE}}$	GVAL	—	—	0000 0x--	uuuu ux--
210h	T1GATE	—	—	—	GSS<4:0>					---0 0000	---u uuuu
211h	T1CLK	—	—	—	—	CS<3:0>				---- 0000	---- uuuu
212h	TMR3L	Holding Register for the Least Significant Byte of the 16-bit TMR3 Register								0000 0000	uuuu uuuu
213h	TMR3H	Holding Register for the Most Significant Byte of the 16-bit TMR3 Register								0000 0000	uuuu uuuu
214h	T3CON	—	—	CKPS<1:0>		—	$\overline{\text{SYNC}}$	RD16	ON	--00 -000	--uu -uuu
215h	T3GCON	GE	GPOL	GTM	GSPM	GGO/$\overline{\text{DONE}}$	GVAL	—	—	0000 0x--	uuuu ux--
216h	T3GATE	—	—	—	GSS<4:0>					---0 0000	---u uuuu
217h	T3CLK	—	—	—	—	CS<3:0>				---- 0000	---- uuuu
218h	TMR5L	Holding Register for the Least Significant Byte of the 16-bit TMR5 Register								0000 0000	uuuu uuuu
219h	TMR5H	Holding Register for the Most Significant Byte of the 16-bit TMR5 Register								0000 0000	uuuu uuuu
21Ah	T5CON	—	—	CKPS<1:0>		—	$\overline{\text{SYNC}}$	RD16	ON	--00 -000	--uu -uuu
21Bh	T5GCON	GE	GPOL	GTM	GSPM	GGO/$\overline{\text{DONE}}$	GVAL	—	—	0000 0x--	uuuu ux--
21Ch	T5GATE	—	—	—	GSS<4:0>					---0 0000	---u uuuu
21Dh	T5CLK	—	—	—	—	CS<3:0>				---- 0000	---- uuuu
21Eh	CCPTMRS0	C4TSEL<1:0>		C3TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>		0101 0101	0101 0101
21Fh	CCPTMRS1	—	—	P7TSEL<1:0>		P6TSEL<1:0>		C5TSEL<1:0>		--01 0101	--01 0101

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Register present on PIC16F18854 devices only.

2: Unimplemented, read as '1'.

TABLE 3-11: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 9											
CPU CORE REGISTERS; see Table 3-2 for specifics											
48Ch	SMT1TMRL	TMR<7:0>								0000 0000	0000 0000
48Dh	SMT1TMRH	TMR<15:8>								0000 0000	0000 0000
48Eh	SMT1TMRU	TMR<23:16>								0000 0000	0000 0000
48Fh	SMT1CPRL	CPR<7:0>								xxxx xxxx	uuuu uuuu
490h	SMT1CPRH	CPR<15:8>								xxxx xxxx	uuuu uuuu
491h	SMT1CPRU	CPR<23:16>								xxxx xxxx	uuuu uuuu
492h	SMT1CPWL	CPW<7:0>								xxxx xxxx	uuuu uuuu
493h	SMT1CPWH	CPW<15:8>								xxxx xxxx	uuuu uuuu
494h	SMT1CPWU	CPW<23:16>								xxxx xxxx	uuuu uuuu
495h	SMT1PRL	PR<7:0>								1111 1111	1111 1111
496h	SMT1PRH	PR<15:8>								1111 1111	1111 1111
497h	SMT1PRU	PR<23:16>								1111 1111	1111 1111
498h	SMT1CON0	EN	—	STP	WPOL	SPOL	CPOL	SMT1PS<1:0>		0-00 0000	0-00 0000
499h	SMT1CON1	SMT1GO	REPEAT	—	—	MODE<3:0>				00-- 0000	00-- 0000
49Ah	SMT1STAT	CPRUP	CPWUP	RST	—	—	TS	WS	AS	000- -000	000- -000
49Bh	SMT1CLK	—	—	—	—	—	CSEL<2:0>			---- -000	---- -000
49Ch	SMT1SIG	—	—	—	SSEL<4:0>					---0 0000	---0 0000
49Dh	SMT1WIN	—	—	—	WSEL<4:0>					---0 0000	---0 0000
49Eh	—	Unimplemented								—	—
49Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Register present on PIC16F18854 devices only.

2: Unimplemented, read as '1'.

9.0 WINDOWED WATCHDOG TIMER (WWDT)

The Watchdog Timer (WDT) is a system timer that generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events. The Windowed Watchdog Timer (WDT) differs in that CLRWDT instructions are only accepted when they are performed within a specific window during the time-out period.

The WDT has the following features:

- Selectable clock source
- Multiple operating modes
  - WDT is always on
  - WDT is off when in Sleep
  - WDT is controlled by software
  - WDT is always off
- Configurable time-out period is from 1 ms to 256 seconds (nominal)
- Configurable window size from 12.5 to 100 percent of the time-out period
- Multiple Reset conditions
- Operation during Sleep

REGISTER 10-6: NVMCON2: NONVOLATILE MEMORY CONTROL 2 REGISTER

W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0
NVMCON2<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
S = Bit can only be set	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **NVMCON2<7:0>:** Flash Memory Unlock Pattern bits

To unlock writes, a 55h must be written first, followed by an AAh, before setting the WR bit of the NVMCON1 register. The value written to this register is used to unlock the writes.

TABLE 10-5: SUMMARY OF REGISTERS ASSOCIATED WITH NONVOLATILE MEMORY (NVM)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	114
PIE7	SCANIE	CRCIE	NVMIE	NCO1IE	—	CWG3IE	CWG2IE	CWG1IE	117
PIR7	SCANIF	CRCIF	NVMIF	NCO1IF	—	CWG3IF	CWG2IF	CWG1IF	126
NVMCON1	—	NVMREGS	LWLO	FREE	WRERR	WREN	WR	RD	166
NVMCON2	NVMCON2<7:0>								167
NVMADRL	NVMADR<7:0>								165
NVMADRH	—(1)	NVMADR<14:8>							165
NVMDATL	NVMDAT<7:0>								165
NVMDATH	—	—	NVMDAT<13:8>						165

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by NVM.

Note 1: Unimplemented, read as '1'.

REGISTER 12-18: SLRCONB: PORTB SLEW RATE CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
SLRB7	SLRB6	SLRB5	SLRB4	SLRB3	SLRB2	SLRB1	SLRB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **SLRB<7:0>:** PORTB Slew Rate Enable bits
For RB<7:0> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

REGISTER 12-19: INLVLB: PORTB INPUT LEVEL CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
INLVLB7	INLVLB6	INLVLB5	INLVLB4	INLVLB3	INLVLB2	INLVLB1	INLVLB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **INLVLB<7:0>:** PORTB Input Level Select bits
For RB<7:0> pins, respectively
1 = ST input used for PORT reads and interrupt-on-change
0 = TTL input used for PORT reads and interrupt-on-change

REGISTER 12-30: CCDPC: CURRENT CONTROLLED DRIVE POSITIVE PORTC REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
CCDPC7	CCDPC6	CCDPC5	CCDPC4	CCDPC3	CCDPC2	CCDPC1	CCDPC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **CCDPC<7:0>:** RC<7:0> Current Controlled Drive Positive Control bits(1)
- 1 = Current-controlled source enabled
- 0 = Current-controlled source disabled

Note 1: If CCDPCy is set, when CCDEN = 0 (Register 12-1), operation of the pin is undefined.

REGISTER 12-31: CCDNC: CURRENT CONTROLLED DRIVE NEGATIVE PORTC REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
CCDNC7	CCDNC6	CCDNC5	CCDNC4	CCDNC3	CCDNC2	CCDNC1	CCDNC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **CCDNC<7:0>:** RC<7:0> Current Controlled Drive Negative Control bits(1)
- 1 = Current-controlled source enabled
- 0 = Current-controlled source disabled

Note 1: If CCDNCy is set, when CCDEN = 0 (Register 12-1), operation of the pin is undefined.

13.0 PERIPHERAL PIN SELECT (PPS) MODULE

The Peripheral Pin Select (PPS) module connects peripheral inputs and outputs to the device I/O pins. Only digital signals are included in the selections. All analog inputs and outputs remain fixed to their assigned pins. Input and output selections are independent as shown in the simplified block diagram Figure 13-1.

TABLE 13-1: PPS INPUT SIGNAL ROUTING OPTIONS

Input Signal Name	Input Register Name	Default Location at POR	Remappable to Pins of PORTx		
			PIC16F18854		
			PORTA	PORTB	PORTC
INT	INTPPS	RB0	●	●	
T0CKI	T0CKIPPS	RA4	●	●	
T1CKI	T1CKIPPS	RC0	●		●
T1G	T1GPPS	RB5		●	●
T3CKI	T3CKIPPS	RC0		●	●
T3G	T3GPPS	RC0	●		●
T5CKI	T5CKIPPS	RC2	●		●
T5G	T5GPPS	RB4		●	●
T2IN	T2INPPS	RC3	●		●
T4IN	T4INPPS	RC5		●	●
T6IN	T6INPPS	RB7		●	●
CCP1	CCP1PPS	RC2		●	●
CCP2	CCP2PPS	RC1		●	●
CCP3	CCP3PPS	RB5		●	●
CCP4	CCP4PPS	RB0		●	●
CCP5	CCP5PPS	RA4	●		●
SMTWIN1	SMTWIN1PPS	RC0		●	●
SMTSIG1	SMTSIG1PPS	RC1		●	●
SMTWIN2	SMTWIN2PPS	RB4		●	●
SMTSIG2	SMTSIG2PPS	RB5		●	●
CWG1IN	CWG1PPS	RB0		●	●
CWG2IN	CWG2PPS	RB1		●	●
CWG3IN	CWG3PPS	RB2		●	●
MDCARL	MDCARLPPS	RA3	●		●
MDCARH	MDCARHPPS	RA4	●		●
MDSRC	MDSRCPPS	RA5	●		●
CLCIN0	CLCIN0PPS	RA0	●		●
CLCIN1	CLCIN1PPS	RA1	●		●
CLCIN2	CLCIN2PPS	RB6		●	●

14.0 PERIPHERAL MODULE DISABLE

The PIC16F18855/75 provides the ability to disable selected modules, placing them into the lowest possible Power mode.

For legacy reasons, all modules are ON by default following any Reset.

14.1 Disabling a Module

Disabling a module has the following effects:

- All clock and control inputs to the module are suspended; there are no logic transitions, and the module will not function.
- The module is held in Reset.
- Any SFRs become “unimplemented”
  - Writing is disabled
  - Reading returns 00h
- Module outputs are disabled; I/O goes to the next module according to pin priority

14.2 Enabling a module

When the register bit is cleared, the module is re-enabled and will be in its Reset state; SFR data will reflect the POR Reset values.

Depending on the module, it may take up to one full instruction cycle for the module to become active. There should be no interaction with the module (e.g., writing to registers) for at least one instruction after it has been re-enabled.

14.3 Disabling a Module

When a module is disabled, any and all associated input selection registers (ISMs) are also disabled.

14.4 System Clock Disable

Setting SYSCMD (PMD0, Register 14-1) disables the system clock (FOSC) distribution network to the peripherals. Not all peripherals make use of SYSCLK, so not all peripherals are affected. Refer to the specific peripheral description to see if it will be affected by this bit.

FIGURE 20-1: SIMPLIFIED CWG BLOCK DIAGRAM (HALF-BRIDGE MODE)

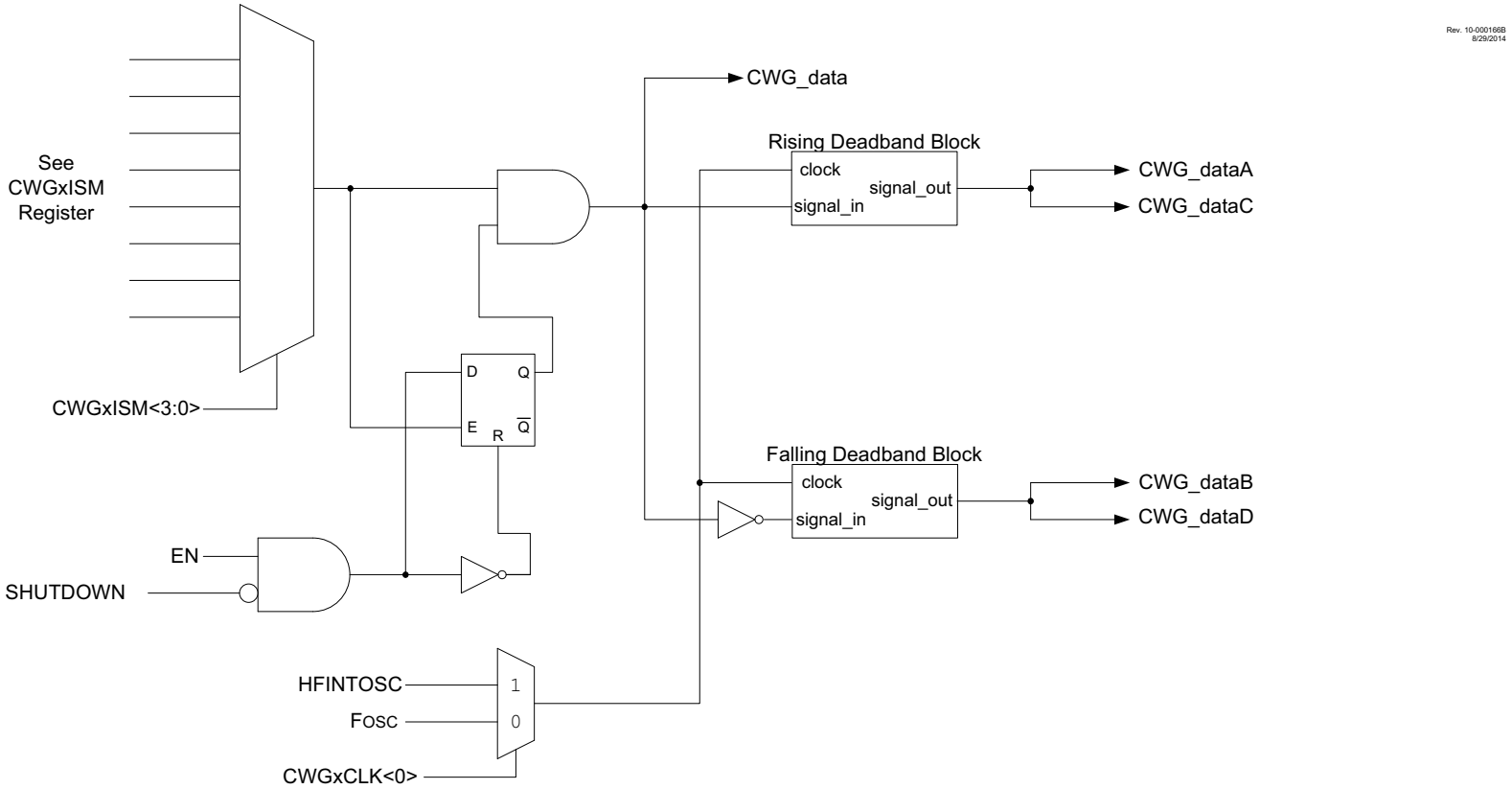
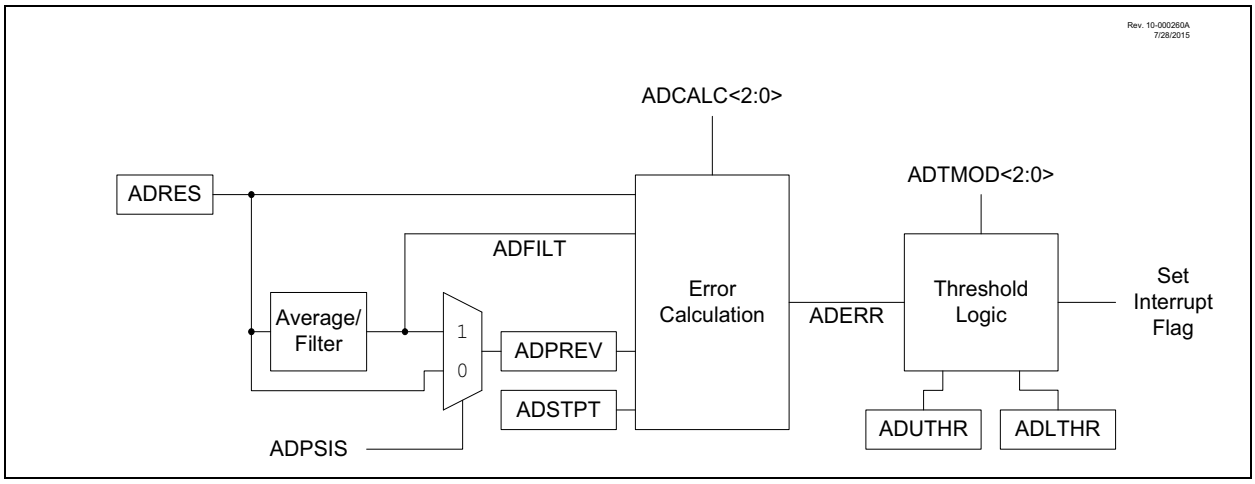


FIGURE 23-11: COMPUTATIONAL FEATURES SIMPLIFIED BLOCK DIAGRAM



The operation of the ADC computational features is controlled by the ADMD <2:0> bits in the ADCON2 register.

The module can be operated in one of five modes:

• **Basic**: This is a legacy mode. In this mode, ADC conversion occurs on single (ADDSEN=0) or double (ADDSEN=1) samples. ADIF is set after each conversion completes.

• **Accumulate**: With each trigger, the ADC conversion result is added to accumulator and ADCNT increments. ADIF is set after each conversion. ADTIF is set according to the Calculation mode.

• **Average**: With each trigger, the ADC conversion result is added to the accumulator. When the ADRPT number of samples have been accumulated, a threshold test is performed. Upon the next trigger, the counter is reset to '1' and the accumulator is replaced with the first ADC conversion cleared. For the subsequent threshold tests, additional ADRPT samples are required to be accumulated.

• **Burst Average**: At the trigger, the accumulator and counter are cleared. The ADC conversion results are then collected repetitively until ADRPT samples are accumulated and finally the threshold is tested.

• **Low-Pass Filter (LPF)**: With each trigger, the ADC conversion result is sent through a filter. When ADRPT samples have occurred, a threshold test is performed. Every trigger after that the ADC conversion result is sent through the filter and another threshold test is performed.

The five modes are summarized in Table 23-3 below.

REGISTER 23-32: ADACT: ADC AUTO CONVERSION TRIGGER CONTROL REGISTER

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	ADACT<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-5 **Unimplemented**: Read as ‘0’

bit 4-0 **ADACT<4:0>**: Auto-Conversion Trigger Select Bits
See Table 23-2.

TABLE 23-6: SUMMARY OF REGISTERS ASSOCIATED WITH ADC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON0	ADON	ADCONT	—	ADCS	—	ADFRM0	—	ADGO	322
ADCON1	ADPPOL	ADIPEN	ADGPOL	—	—	—	—	ADDSEN	323
ADCON2	ADPSIS	ADCRS<2:0>			ADACLR	ADMD<2:0>			324
ADCON3	—	ADCALC<2:0>			ADSOI	ADTMD<2:0>			325
ADACT	—	—	—	ADACT<4:0>					324
ADACCH	ADACCH								334
ADACCL	ADACCL								334
ADPREVH	ADPREVH								333
ADPREVL	ADPREVL								334
ADRESH	ADRESH								332
ADRESL	ADRESL								332
ADSTAT	ADAOV	ADUTHR	ADLTHR	ADMATH	—	ADSTAT<2:0>			326
ADCLK	—	—	ADCCS<5:0>						327
ADREF	—	—	—	ADNREF	—	—	ADPREF<1:0>		327
ADCAP	—	—	—	ADCAP<4:0>					330
ADPRE	ADPRE<7:0>								329
ADACQ	ADACQ<7:0>								329
ADPCH	—	—	ADPCH<5:0>						328
ADCNT	ADCNT<7:0>								331
ADRPT	ADRPT<7:0>								330
ADLTHL	ADLTH<7:0>								336
ADLTHH	ADLTH<15:8>								336
ADUTHL	ADUTH<7:0>								337
ADUTHH	ADUTH<15:8>								337
ADSTPTL	ADSTPT<7:0>								335
ADSTPTH	ADSTPT<15:8>								335
ADFLTRL	ADFLTR<7:0>								331
ADFLTRH	ADFLTR<15:8>								331
ADERRL	ADERR<7:0>								336
ADERRH	ADERR<15:8>								335
ANSELA	ANSA7	ANSA6	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	185
ANSELB	ANSB7	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	193
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	ANSC1	ANSC0	201
DAC1CON1	—	—	—	DAC1R<4:0>					354
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		234
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	114
PIE1	OSFIE	CSWIE	—	—	—	—	ADTIE	ADIE	116
PIR1	OSFIF	CSWIF	—	—	—	—	ADTIF	ADIF	125
OSCSTAT	EXTOR	HFOR	MFOR	LFOR	SOR	ADOR	—	PLLR	104

Legend: – = unimplemented read as '0'. Shaded cells are not used for the ADC module.

Note 1: only.

28.11 Register Definitions: Timer1 Control start here with Memory chapter compare

Long bit name prefixes for the Timer1/3/5 are shown in Table 28-3. Refer to **Section 1.1 "Register and Bit naming conventions"** for more information

TABLE 28-3:

Peripheral	Bit Name Prefix
Timer1	T1
Timer3	T3
Timer5	T5

REGISTER 28-1: TxCON: TIMER1/3/5 CONTROL REGISTER

U-0	U-0	R/W-0/u	R/W-0/u	U-0	R/W-0/u	R/W-0/u	R/W-0/u
—	—	CKPS<1:0>		—	$\overline{\text{SYNC}}$	RD16	ON
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
- 11 = 1:8 Prescale value
- 10 = 1:4 Prescale value
- 01 = 1:2 Prescale value
- 00 = 1:1 Prescale value

bit 3 **Unimplemented:** Read as '0'

bit 2 **SYNC:** Timer1 Synchronization Control bit

When TMR1CLK = FOSC or FOSC/4
This bit is ignored. The timer uses the internal clock and no additional synchronization is performed.
When TMR1CS<1:0> = (any setting other than FOSC or FOSC/4)
- 1 = Do not synchronize external clock input
- 0 = Synchronized external clock input with system clock

bit 1 **RD16:** Timer1 On bit
- 1 = Enables Timer1
- 0 = Stops Timer1 and clears Timer1 gate flip-flop

bit 0 **ON:** Timer1 On bit
- 1 = Enables Timer1
- 0 = Stops Timer1 and clears Timer1 gate flip-flop

TABLE 28-4: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	114
PIR1	OSFIF	CSWIF	—	—	—	—	ADTIF	ADIF	114
PIE1	OSFIE	CSWIE	—	—	—	—	ADTIE	ADIE	116
T1CON	—	—	CKPS<5:4>		—	$\overline{\text{SYNC}}$	RD16	ON	383
T1GCON	GE	GPOL	GTM	GSPM	GGO/$\overline{\text{DONE}}$	GVAL	—	—	384
T1GATE	—	—	—	GSS<4:0>					386
T1CLK	—	—	—	—	CS<3:0>				385
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								375*
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								375*
T1CKIPPS	—	—	—	T1CKIPPS<4:0>					214
T1GPPS	—	—	—	T1GPPS<4:0>					214
T3CON	—	—	CKPS<5:4>		—	$\overline{\text{SYNC}}$	RD16	ON	383
T3GCON	GE	GPOL	GTM	GSPM	GGO/$\overline{\text{DONE}}$	GVAL	—	—	384
T3GATE	—	—	—	GSS<4:0>					386
T3CLK	—	—	—	—	CS<3:0>				385
TMR3L	Holding Register for the Least Significant Byte of the 16-bit TMR3 Register								375*
TMR3H	Holding Register for the Most Significant Byte of the 16-bit TMR3 Register								375*
T3CKIPPS	—	—	—	T3CKIPPS<4:0>					214
T3GPPS	—	—	—	T3GPPS<4:0>					214
T5CON	—	—	CKPS<5:4>		—	$\overline{\text{SYNC}}$	RD16	ON	383
T5GCON	GE	GPOL	GTM	GSPM	GGO/$\overline{\text{DONE}}$	GVAL	—	—	384
T5GATE	—	—	—	GSS<4:0>					386
T5CLK	—	—	—	—	CS<3:0>				385
TMR5L	Holding Register for the Least Significant Byte of the 16-bit TMR5 Register								375*
TMR5H	Holding Register for the Most Significant Byte of the 16-bit TMR5 Register								375*
T5CKIPPS	—	—	—	T5CKIPPS<4:0>					214
T5GPPS	—	—	—	T5GPPS<4:0>					214
T0CON0	T0EN	—	T0OUT	T016BIT	T0OUTPS<3:0>				372
CMxCON0	CxON	CxOUT	—	CxPOL	—	CxSP	CxHYS	CxSYNC	245
CCPTMRS0	C4TSEL<1:0>		C3TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>		421
CCPTMRS1	—	—	P7TSEL<1:0>		P6TSEL<1:0>		C5TSEL<1:0>		421
CCPxCON	CCPxEN	—	CCPxOUT	CCPxFMT	CCPxMODE<3:0>				418
CLCxSELy	—	—	—	LCxDyS<4:0>					294
ADACT	—	—	—	ADACT<4:0>					324

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used with the Timer1 modules.

* Page with register information.

REGISTER 30-1: CCPxCON: CCPx CONTROL REGISTER (CONTINUED)

bit 3-0 **MODE<3:0>:** CCPx Mode Select bits(1)

1111 = PWM mode
1110 = Reserved
1101 = Reserved
1100 = Reserved

1011 = Compare mode: output will pulse 0-1-0; Clears TMR1
1010 = Compare mode: output will pulse 0-1-0
1001 = Compare mode: clear output on compare match
1000 = Compare mode: set output on compare match

0111 = Capture mode: every 16th rising edge of CCPx input
0110 = Capture mode: every 4th rising edge of CCPx input
0101 = Capture mode: every rising edge of CCPx input
0100 = Capture mode: every falling edge of CCPx input

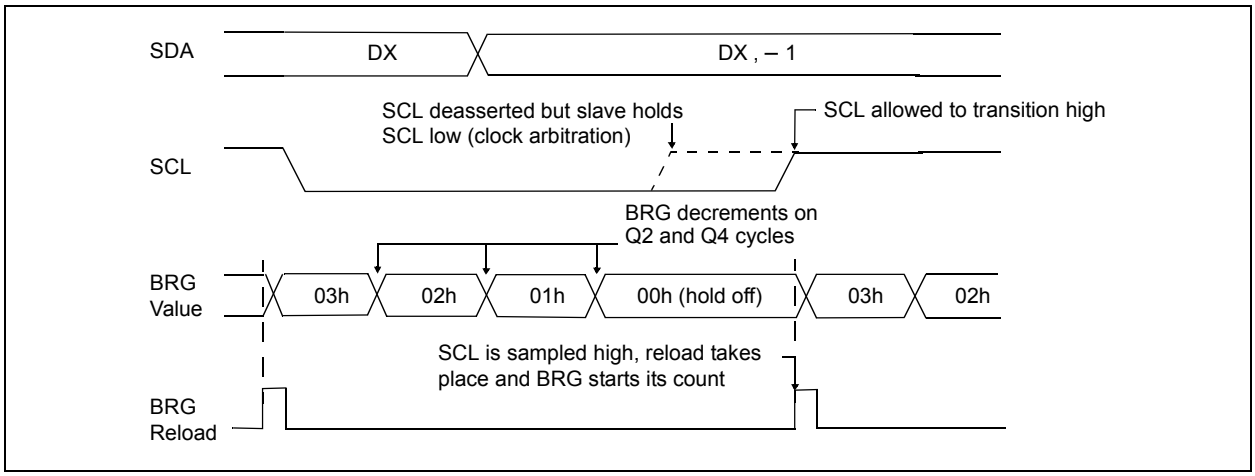
0011 = Capture mode: every edge of CCPx input
0010 = Compare mode: toggle output on match
0001 = Compare mode: toggle output on match; clear TMR1
0000 = Capture/Compare/PWM off (resets CCPx module)

Note 1: All modes will set the CCPxIF bit, and will trigger an ADC conversion if CCPx is selected as the ADC trigger source.

31.6.2 CLOCK ARBITRATION

Clock arbitration occurs when the master, during any receive, transmit or Repeated Start/Stop condition, releases the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the Baud Rate Generator (BRG) is suspended from counting until the SCL pin is actually sampled high. When the SCL pin is sampled high, the Baud Rate Generator is reloaded with the contents of SSPxADD<7:0> and begins counting. This ensures that the SCL high time will always be at least one BRG rollover count in the event that the clock is held low by an external device (Figure 31-25).

FIGURE 31-25: BAUD RATE GENERATOR TIMING WITH CLOCK ARBITRATION

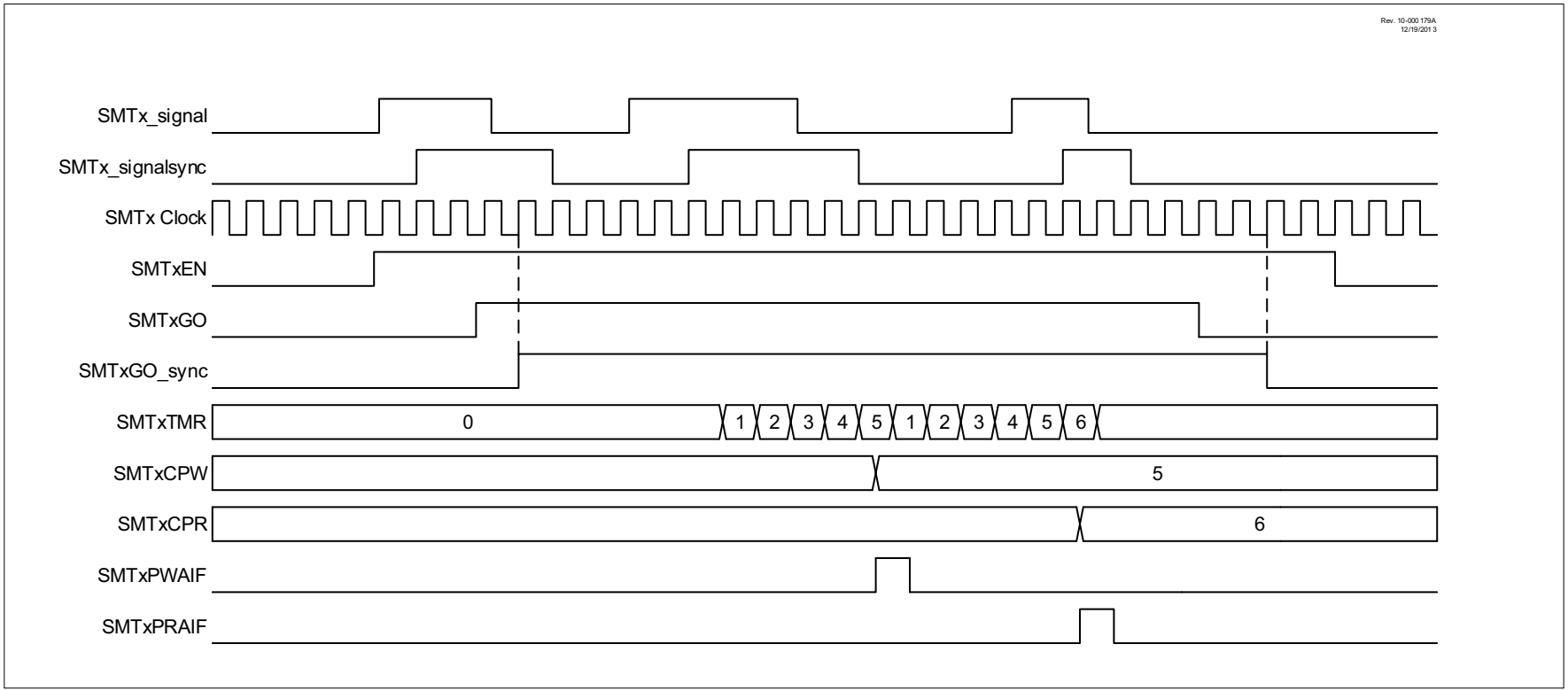


31.6.3 WCOL STATUS FLAG

If the user writes the SSPxBUF when a Start, Restart, Stop, Receive or Transmit sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write does not occur). Any time the WCOL bit is set it indicates that an action on SSPxBUF was attempted while the module was not idle.

Note:	Because queuing of events is not allowed, writing to the lower five bits of SSPxCON2 is disabled until the Start condition is complete.

FIGURE 32-9: HIGH AND LOW MEASURE MODE SINGLE ACQUISITION TIMING DIAGRAM



36.0 INSTRUCTION SET SUMMARY

Each instruction is a 14-bit word containing the operation code (opcode) and all required operands. The opcodes are broken into three broad categories.

- Byte Oriented
- Bit Oriented
- Literal and Control

The literal and control category contains the most varied instruction word format.

Table 36-4 lists the instructions recognized by the MPASM™ assembler.

All instructions are executed within a single instruction cycle, with the following exceptions, which may take two or three cycles:

- Subroutine takes two cycles (CALL, CALLW)
- Returns from interrupts or subroutines take two cycles (RETURN, RETLW, RETFIE)
- Program branching takes two cycles (GOTO, BRA, BRW, BTFSS, BTFSC, DECFSZ, INCSFZ)
- One additional instruction cycle will be used when any instruction references an indirect file register and the file select register is pointing to program memory.

One instruction cycle consists of 4 oscillator cycles; for an oscillator frequency of 4 MHz, this gives a nominal instruction execution rate of 1 MHz.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

36.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

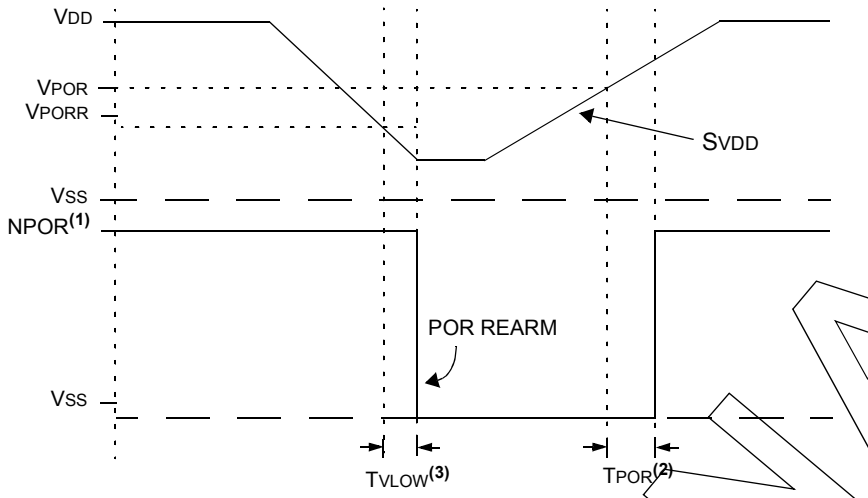
TABLE 36-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
n	FSR or INDF number. (0-1)
mm	Prepost increment-decrement mode selection

TABLE 36-2: ABBREVIATION DESCRIPTIONS

Field	Description
PC	Program Counter
$\overline{TO}$	Time-Out bit
C	Carry bit
DC	Digit Carry bit
Z	Zero bit
$\overline{PD}$	Power-Down bit

FIGURE 37-3: POR AND POR REARM WITH SLOW RISING VDD



Note 1: When NPOR is low, the device is held in Reset.
2: TPOR 1 μs typical.
3: TVLOW 2.7 μs typical.

