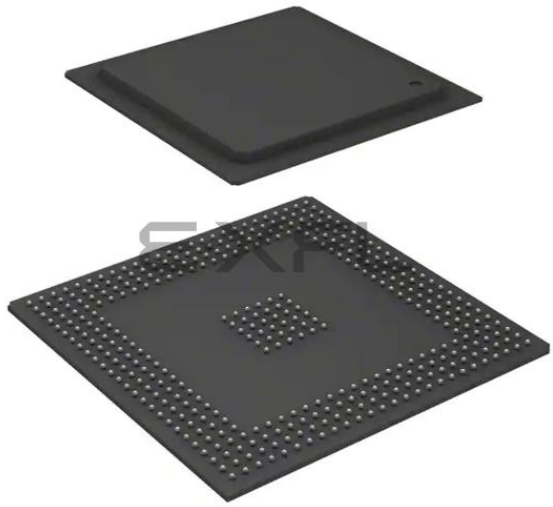

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Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
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Chapter 2
Signal Descriptions

This chapter describes the MPC561/MPC563 microcontroller's external signals. It contains a description of individual signals, shows their behavior, shows whether the signal is an input or an output, and indicates signal multiplexing.

NOTE

A bar over a signal name indicates that the signal is active-low—for example, $\overline{\text{TA}}$ (transfer acknowledge). Active-low signals are referred to as asserted (active) when they are low and negated when they are high. Signals that are not active-low, such as ADDR[8:31] (address bus signals) and DATA[0:31] (data bus signals) are referred to as asserted when they are high and negated when they are low.

Refer to Appendix F, "Electrical Characteristics," and Appendix G, "66-MHz Electrical Characteristics," for detailed electrical information for each signal.

2.1 Signal Groupings

Figure 2-1 illustrates the external signals of the MPC561/MPC563 grouped by functional module.

Table 2-1. MPC561/MPC563 Signal Descriptions (continued)

Signal Name	No. of Signals	Type	Function after Reset[1]	Description
A_AN2 / A_ANy/ A_PQB2	1	I	A_AN2	Analog Channel 2. Internally multiplexed input-only analog channel. The input is passed on as a separate signal to the QADC64E.
		I		Multiplexed Analog Input (A_ANy). Externally multiplexed analog input.
		I/O[5]		Port A_PQB2. This is a bidirectional general-purpose I/O if the QADC64E is configured in enhanced mode, otherwise it is an input only.
A_AN3 / A_ANz / A_PQB3	1	I	A_AN3	Analog Input 3. Internally multiplexed input-only analog channel. The input is passed on as a separate signal to the QADC64E.
		I		Multiplexed Analog Input (A_ANz). Externally multiplexed analog input.
		I/O[5]		Port A_PQB 3. This is a bidirectional general-purpose I/O if the QADC64E is configured in enhanced mode, otherwise it is an input only.
A_AN[48:51] / A_PQB[4:7]	4	I	AN[48:51]	Analog Input [48:51]. Analog input channel. The input is passed on as a separate signal to the QADC64E.
		I/O[5]		Port A_PQB[4:7]. This is a bidirectional general-purpose I/O if the QADC64E is configured in enhanced mode, otherwise it is an input only.
A_AN[52:54] / A_MA[0:2] / A_PQA[0:2]	3	I	A_AN[52:54]	Analog Input [52:54]. Input-only. These inputs are passed on as separate signals to the QADC64E.
		I		Multiplexed Address [0:2] for QADC64E Module A. Provides a three-bit multiplexed address output to the external multiplexer chip to allow selection of one of the eight inputs.
		I/O		Port A_PQA[0:2]. This is a bidirectional general-purpose I/O.
A_AN[55:59] / A_PQA[3:7]	5	I	A_AN[55:59]	Analog Input [55:59]. Input-only. These inputs are passed on as separate signals to the QADC64E.
		I/O		Port A_PQA[3:7]. This is a bidirectional general-purpose I/O.
B_AN0 / B_ANw / B_PQB0	1	I	B_AN0	Analog Channel 0. Internally multiplexed input-only analog channel. Passed on as a separate signal to the QADC64E.
		I		Multiplexed Analog Input (B_ANw). Externally multiplexed analog input.
		I/O		Port B_PQB0. This is a bidirectional general-purpose I/O if the QADC64E is configured in enhanced mode, otherwise it is an input only.

Table 2-14. MPC561/MPC563 Signal Reset State (continued)

Signal List[1]	Voltage	Slew Rate Controlled Option?	Drive Load (pF)[2]	Reset State	Hysteresis Enabled?	Function After HRESET, PORESET/TRST
TXD2 /	5 V	Yes	50 ; 50	PU5 until PULL_DIS1 is set	No	QGPO2
QGPO2 /	5 V	Yes	50 ; 50		No	
C_CNTX0	5 V	Yes	50 ; 50		No	
RXD1 /	5 V	NA	NA	Must be driven or connected to a pull device	No	QGPI1
QGPI1	5 V	NA	NA		No	
RXD2 /	5 V	NA	NA	Must be driven or connected to a pull device	No	QGPI2
QGPI2 /	5 V	NA	NA		No	
C_CNRX0	5 V	NA	NA		No	
MIOS14						
MDA[11:15, 27:31]	5 V	Yes	50 ; 50	Pull device enabled until PULL_DIS0 is set[16]	Yes	MDA[11:15,27:31]
MPWM0 /	5 V	Yes	50 ; 50	Pull device enabled until PULL_DIS0 is set [16]	Yes	MPWM0 unless the Nexus (READI) port is enabled, then MDI1. See Section 2.5.
MDI1	2.6 V	No	NA		Yes	
MPWM1 [3] /	5 V	Yes	50 ; 50	Pull device enabled until PULL_DIS0 is set [16]	Yes	MPWM1 unless the Nexus (READI) port is enabled, then MDO2. See Section 2.5.
MDO2	2.6 V	No	50 ; 25		No	
MPWM2[3] /	5 V	Yes	50 ; 50	Pull device enabled until PULL_DIS0 is set [16]	Yes	MPWM2
	2.6 V	No	50 ; 25		No	
PPM_TX1	5 V	Yes	50 ; 25		No	
MPWM3/	5 V	Yes	50 ; 50	Pull device enabled until PULL_DIS0 is set [16]	Yes	MPWM3
PPM_RX1	2.6 V	No	NA		Yes	
MPWM16	5 V	Yes	50 ; 50	Pull device enabled until PULL_DIS0 is set [16]	Yes	MPWM16
MPWM17[3] /	5 V	Yes	50 ; 50	Pull device enabled until PULL_DIS0 is set [16]	Yes	MPWM17 unless the Nexus (READI) port is enabled. See Section 2.5.
MDO3	2.6 V	No	50 ; 25		No	

NOTE

The 8 Kbytes allocated for the original PowerPC ISA exception table can be almost fully utilized. This is possible if the MPC561/MPC563 system memory is *not* mapped to the exception address space, (i.e., the addresses 0xFFF0 0000 to 0xFFF0 1FFF are not used).

In such case, these 8 Kbytes can be fully utilized by the compiler, except for the lower 64 words (256 bytes) which are dedicated for the branch instructions.

If the RCPU, while executing an exception, issues any address between two successive exception entries (e.g., 0xFFF0 0104), then the operation of the MPC561/MPC563 is not guaranteed if the ETR is enabled.

In order to activate the exception table relocation feature, the following steps are required:

1. Set the RCPU MSR[IP] bit
2. Set the BBCMCR[ETRE] bit. See Section 4.6.2.1, "BBC Module Configuration Register (BBCMCR)," for programming details.

The ETR feature can be activated from reset, by setting corresponding bits in the reset configuration word.

Table 4-1. Exception Addresses Mapping

Name of Exception	Original Address Issues by Core	Mapped Address by Exception Table Relocation Logic	
Reserved	0xFFF0 0000	Page_Offset+0x000	
System Reset	0xFFF0 0100	Compression disabled	Compression enabled
		Page_Offset[1]+0x08	Page_Offset[1]+0x0B8
Machine Check	0xFFF0 0200	Page_Offset+0x010	
Reserved	0xFFF0 0300	Page_Offset+0x018	
Reserved	0xFFF0 0400	Page_Offset+0x020	
External Interrupt[2]	0xFFF0 0500	Page_Offset+0x028	
Alignment	0xFFF0 0600	Page_Offset+0x030	
Program	0xFFF0 0700	Page_Offset+0x038	
Floating Point unavailable	0xFFF0 0800	Page_Offset+0x040	
Decrementer	0xFFF0 0900	Page_Offset+0x048	
Reserved	0xFFF0 0A00	Page_Offset+0x050	
Reserved	0xFFF0 0B00	Page_Offset+0x058	
System Call	0xFFF0 0C00	Page_Offset+0x060	
Trace	0xFFF0 0D00	Page_Offset+0x068	
Floating Point Assist	0xFFF0 0E00	Page_Offset+0x070	
Implementation Dependent Software Emulation	0xFFF0 1000	Page_Offset+0x080	

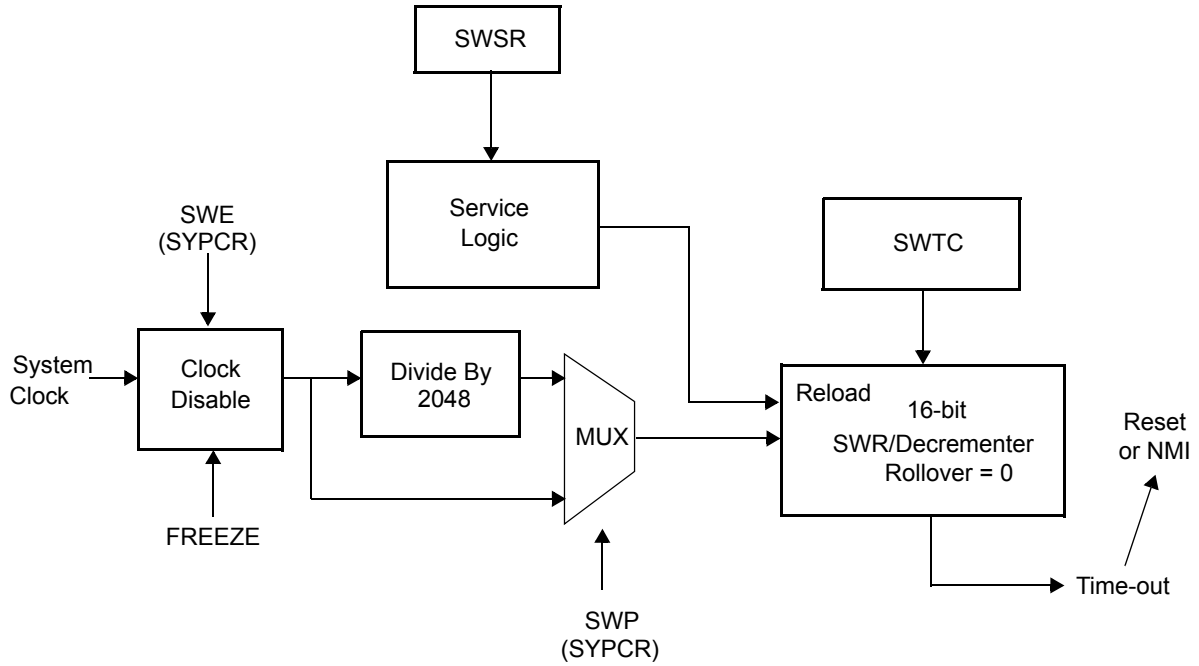


Figure 6-10. SWT Block Diagram

6.1.11 Freeze Operation

When the FREEZE line is asserted, the clocks to the software watchdog, the periodic interrupt timer, the real-time clock, the time base counter, and the decrementer can be disabled. This is controlled by the associated bits in the control register of each timer. If programmed to stop during FREEZE assertion, the counters maintain their values while FREEZE is asserted. The bus monitor remains enabled regardless of this signal.

6.1.12 Low Power Stop Operation

When the processor is set in a low-power mode (doze, sleep, or deep-sleep), the software watchdog timer is frozen. It remains frozen and maintains its count value until the processor exits this state and resumes executing instructions.

The periodic interrupt timer, decrementer, and time base are not affected by these low-power modes. They continue to run at their respective frequencies. These timers are capable of generating an interrupt to bring the MCU out of these low-power modes.

6.2 Memory Map and Register Definitions

This section provides the MPC561/MPC563 memory map, register diagrams and bit descriptions of the system configuration and protection registers.

6.2.1 Memory Map

The MPC561/MPC563 internal memory space can be assigned to one of eight locations.

7.5.2 Hard Reset Configuration Word (RCW)

Following is the hard reset configuration word that is sampled from the internal data bus, data_sgpiod(0:31) on the negation of HRESET. If the external reset config word is selected (RSTCONF = 0), the internal data bus will reflect the state of external data bus. If the internal reset config word is selected and neither of the Flash reset config words are enabled (UC3FCFIG[HC] = 1), the internal data bus is internally driven with all zeros. The reset configuration word is not a register in the memory map. Most of the bits in the configuration are located in registers in the SIU. Refer to Table 7-5 for a detailed description of each control bit.

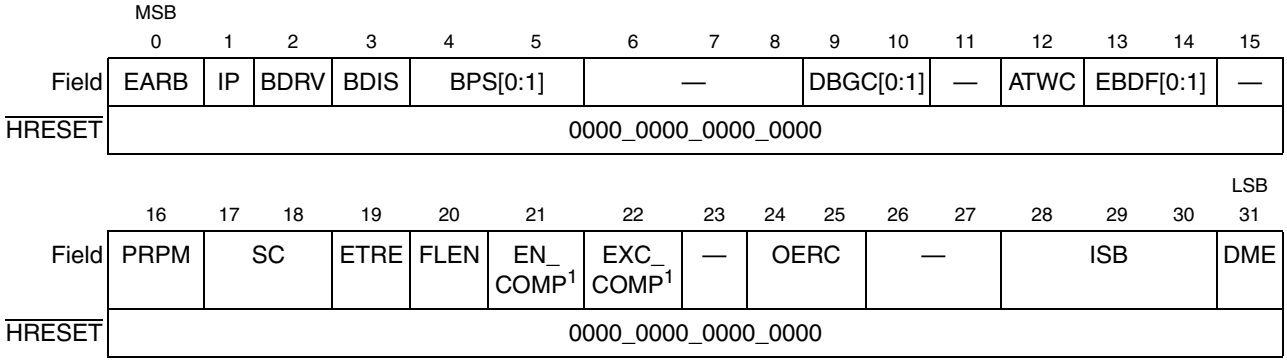


Figure 7-7. Reset Configuration Word (RCW)

[1] Available only on the MPC562/MPC564, software should write "0" to this bit for MPC561/MPC563.

Table 7-5. RCW Bit Descriptions

Bits	Name	Description
0	EARB	External Arbitration — Refer to Section 9.5.7, "Arbitration Phase," for a detailed description of Bus arbitration. The default value is that internal arbitration hardware is used. 0 Internal arbitration is performed 1 External arbitration is assumed
1	IP	Initial Interrupt Prefix — This bit defines the initial value of MSR[IP] immediately after reset. MSR[IP] defines the Interrupt Table location. If IP is zero then the initial value of MSR[IP] is zero, If the IP is one, then the initial value of MSR[IP] is one. Default value is zero. See Table 3-11 for more information. 0 MSR[IP] = 0 after reset 1 MSR[IP] = 1 after reset
2	BDRV	Bus Pins Drive Strength — This bit determines the bus pins (address, data and control) driving capability to be either full or reduced drive. The bus default drive strength is full; Upon default, it also effects the CLKOUT drive strength to be full. See Table 6-7 for more information. BDRV controls the default state of COM1 in the SIUMCR. 0 Full drive 1 Reduced drive
3	BDIS	Boot Disable — If the BDIS bit is set, then memory controller is not activated after reset. If it is cleared then the memory controller bank 0 is active immediately after reset such that it matches any addresses. If a write to the OR0 register occurs after reset this bit definition is ignored. The default value is that the memory controller is enabled to control the boot with the CS0 pin. See Section 10.7, "Global (Boot) Chip-Select Operation," for more information. 0 Memory controller bank 0 is active and matches all addresses immediately after reset 1 Memory controller is not activated after reset.

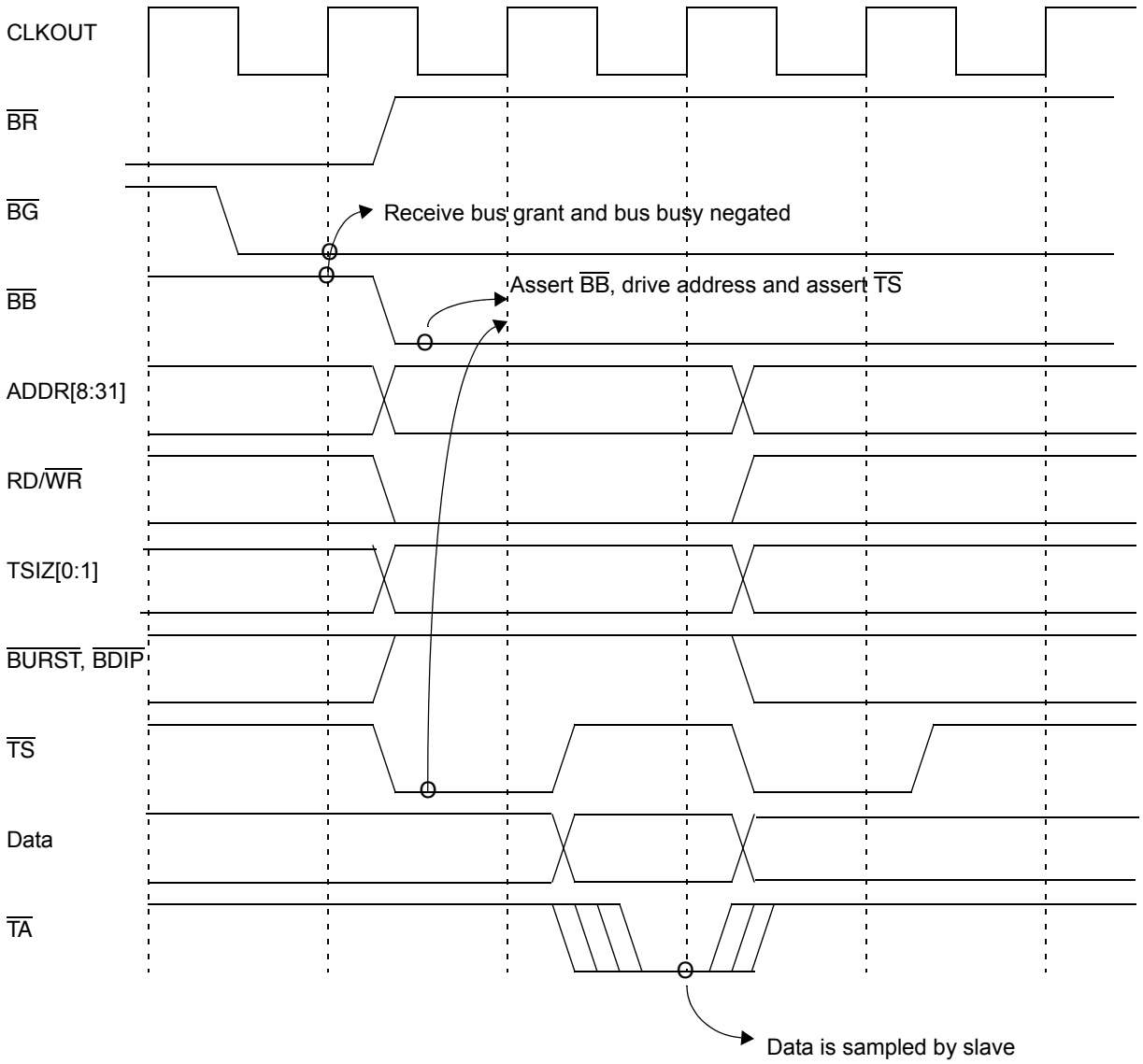
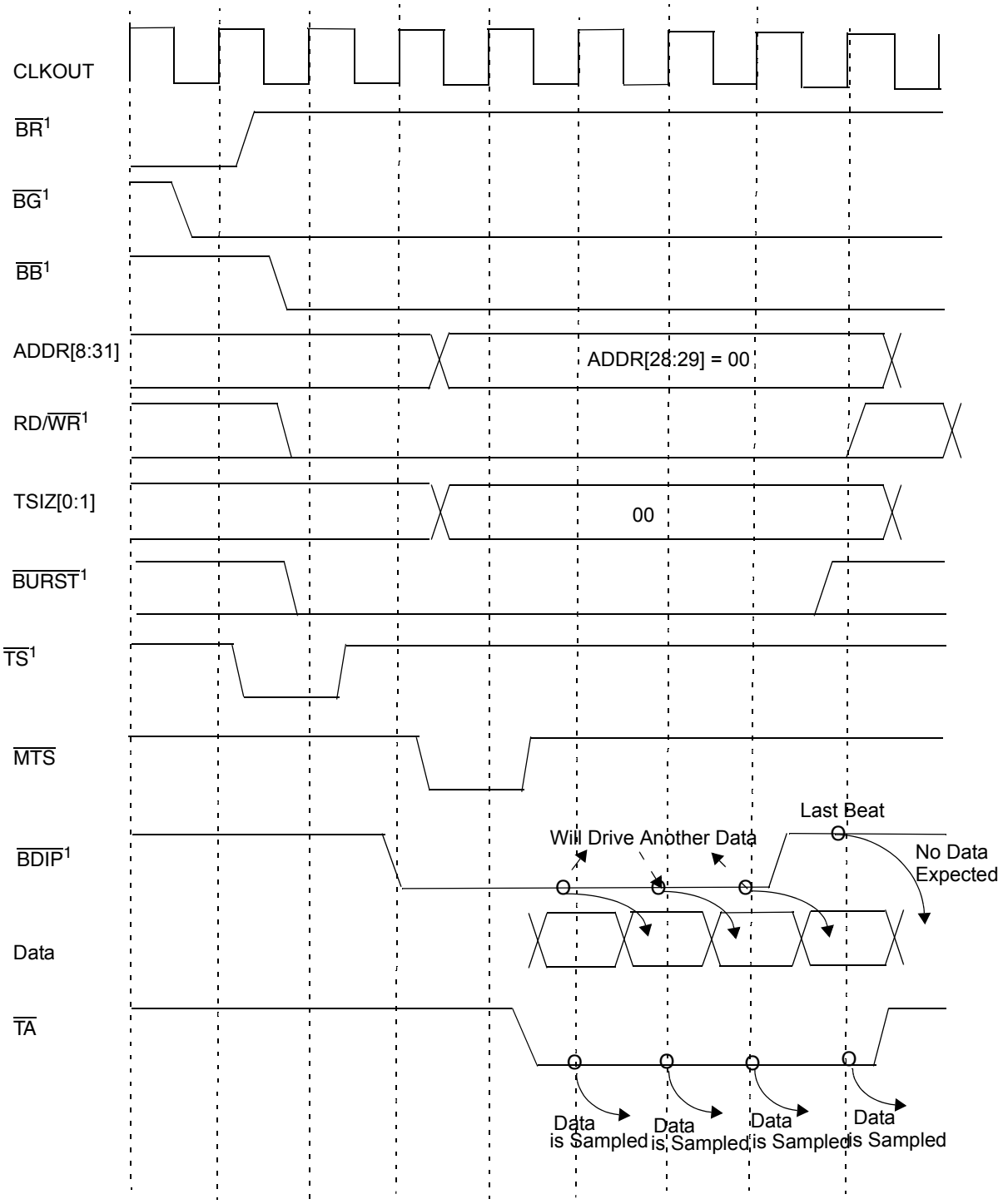


Figure 9-8. Single Beat Basic Write Cycle Timing – Zero Wait States

Figure 9-17. Basic Flow Diagram of a Burst-Write Cycle



[1]From external master

Figure 9-18. Burst-Write Cycle, 32-Bit Port Size, Zero Wait States (Only for External Master Memory Controller Service Support)

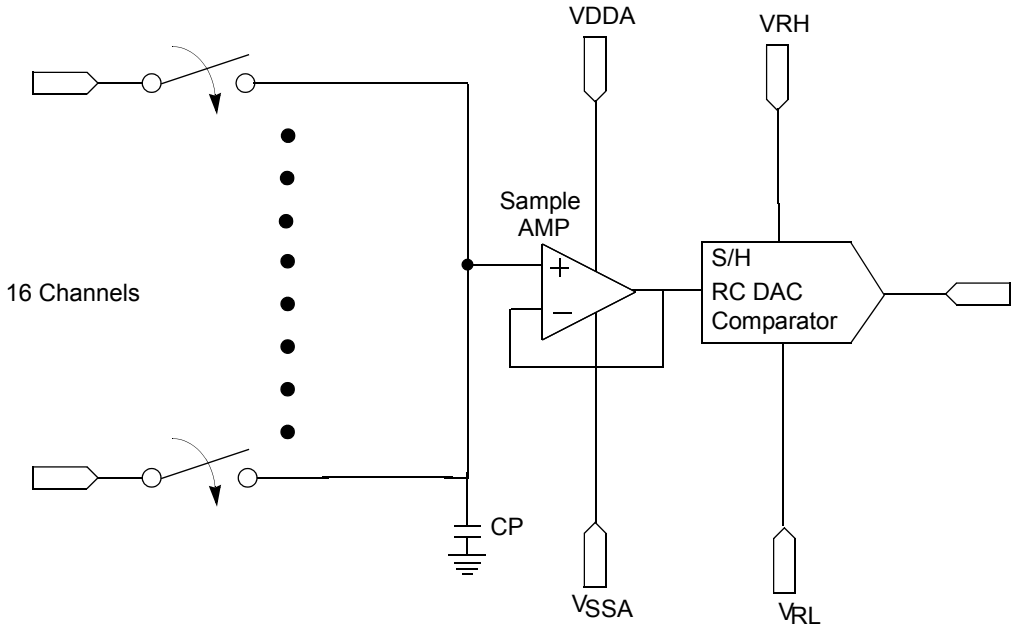


Figure 13-49. Equivalent Analog Input Circuitry

Since the sample amplifier is powered by V_{DDA} and V_{SSA}, it can accurately transfer input signal levels up to but not exceeding V_{DDA} and down to but not below $V_{SSA.}$ If the input signal is outside of this range, the output from the sample amplifier is clipped.

In addition, V_{RH} and V_{RL} must be within the range defined by V_{DDA} and V_{SSA}. As long as V_{RH} is less than or equal to V_{DDA} and V_{RL} is greater than or equal to V_{SSA} and the sample amplifier has accurately transferred the input signal, resolution is ratiometric within the limits defined by V_{RL} and V_{RH}. If V_{RH} is greater than V_{DDA}, the sample amplifier can never transfer a full-scale value. If V_{RL} is less than V_{SSA}, the sample amplifier can never transfer a zero value.

Figure 13-50 shows the results of reference voltages outside the range defined by V_{DDA} and V_{SSA}. At the top of the input signal range, V_{DDA} is 10 mV lower than V_{RH}. This results in a maximum obtainable 10-bit conversion value of 0x3FE. At the bottom of the signal range, V_{SSA} is 15 mV higher than V_{RL}, resulting in a minimum obtainable 10-bit conversion value of three.

Table 14-14. Queue 2 Operating Modes (continued)

MQ2[3:7]	Operating Modes
01010	Interval timer single-scan mode: time = QCLK period x 2^{13}
01011	Interval timer single-scan mode: time = QCLK period x 2^{14}
01100	Interval timer single-scan mode: time = QCLK period x 2^{15}
01101	Interval timer single-scan mode: time = QCLK period x 2^{16}
01110	Interval timer single-scan mode: time = QCLK period x 2^{17}
01111	Reserved mode
10000	Reserved mode
10001	Software triggered continuous-scan mode
10010	External trigger rising edge continuous-scan mode
10011	External trigger falling edge continuous-scan mode
10100	Periodic timer continuous-scan mode: time = QCLK period x 2^{7}
10101	Periodic timer continuous-scan mode: time = QCLK period x 2^{8}
10110	Periodic timer continuous-scan mode: time = QCLK period x 2^{9}
10111	Periodic timer continuous-scan mode: time = QCLK period x 2^{10}
11000	Periodic timer continuous-scan mode: time = QCLK period x 2^{11}
11001	Periodic timer continuous-scan mode: time = QCLK period x 2^{12}
11010	Periodic timer continuous-scan mode: time = QCLK period x 2^{13}
11011	Periodic timer continuous-scan mode: time = QCLK period x 2^{14}
11100	Periodic timer continuous-scan mode: time = QCLK period x 2^{15}
11101	Periodic timer continuous-scan mode: time = QCLK period x 2^{16}
11110	Periodic timer continuous-scan mode: time = QCLK period x 2^{17}
11111	Reserved mode

NOTE

If BQ2 was assigned to the CCW that queue 1 is currently working on, then that conversion is completed before BQ2 takes effect.

Each time a CCW is read for queue 1, the CCW location is compared with the current value of the BQ2 pointer to detect a possible end-of-queue condition. For example, if BQ2 is changed to CCW3 while queue 1 is converting CCW2, queue 1 is terminated after the conversion is completed. However, if BQ2 is changed to CCW1 while queue 1 is converting CCW2, the QADC64E would not recognize a BQ2 end-of-queue condition until queue 1 execution reached CCW1 again, presumably on the next pass through the queue.

but the data register (SC1DR) is still full. The data in the shifter that generated the OR assertion is overwritten by the next received data frame, but the data in the SC1DR is not lost.

Table 17-18. MDASM Address Map (continued)

Address	Register
0x30 605C	MDASM11 Status/Control Register Duplicated (MDASMSCRD) See Table 17-21 for bit descriptions.
0x30 605E	MDASM11 Status/Control Register (MDASMSCR) See Table 17-21 for bit descriptions.
MDASM12	
0x30 6060	MDASM12 Data A Register (MDASMAR)
0x30 6062	MDASM12 Data B Register (MDASMBR)
0x30 6064	MDASM12 Status/Control Register Duplicated (MDASMSCRD)
0x30 6066	MDASM12 Status/Control Register (MDASMSCR)
MDASM13	
0x30 6068	MDASM13 Data A Register (MDASMAR)
0x30 606A	MDASM13 Data B Register (MDASMBR)
0x30 606C	MDASM13 Status/Control Register Duplicated (MDASMSCRD)
0x30 606E	MDASM13 Status/Control Register (MDASMSCR)
MDASM14	
0x30 6070	MDASM14 Data A Register (MDASMAR)
0x30 6072	MDASM14 Data B Register (MDASMBR)
0x30 6074	MDASM14 Status/Control Register Duplicated (MDASMSCRD)
0x30 6076	MDASM14 Status/Control Register (MDASMSCR)
MDASM15	
0x30 6078	MDASM15 Data A Register (MDASMAR)
0x30 607A	MDASM15 Data B Register (MDASMBR)
0x30 607C	MDASM15 Status/Control Register Duplicated (MDASMSCRD)
0x30 607E	MDASM15 Status/Control Register (MDASMSCR)
MDASM27	
0x30 60D8	MDASM27 Data A Register (MDASMAR)
0x30 60DA	MDASM27 Data B Register (MDASMBR)
0x30 60DC	MDASM27 Status/Control Register Duplicated (MDASMSCRD)
0x30 60DE	MDASM27 Status/Control Register (MDASMSCR)
MDASM28	
0x30 60E0	MDASM28 Data A Register (MDASMAR)
0x30 60E2	MDASM28 Data B Register (MDASMBR)

Table 22-2. CALRAM Control Registers

Address	Register
0x38 0000	CRAMMCR
0x38 0004	for factory test
0x38 0008	CRAM_RBA0
0x38 000C	CRAM_RBA1
0x38 0010	CRAM_RBA2
0x38 0014	CRAM_RBA3
0x38 0018	CRAM_RBA4
0x38 001C	CRAM_RBA5
0x38 0020	CRAM_RBA6
0x38 0024	CRAM_RBA7
0x38 0028	CRAMOVLCR
0x38 002C	CRAMOTR/READI_OTR
0x38 0030	Reserved
0x38 0034	Reserved
0x38 0038	Reserved
0x38 003C	Reserved

Any unimplemented bits in CALRAM registers return 0's on a read and writes to these bits are ignored.

22.5.1 CALRAM Module Configuration Register (CRAMMCR)

The module configuration register (CRAMMCR) contains bits that allow the CALRAM to be configured for normal RAM accesses.

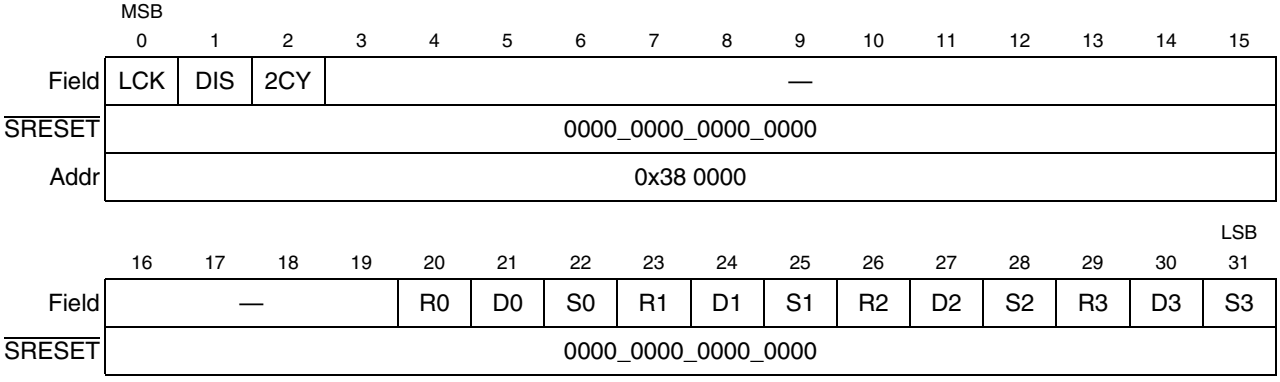


Figure 22-9. CALRAM Module Configuration Register (CRAMMCR)

A brief description of each bit is provided in Table 22-3

comparator when working in half-word mode and to the correct bytes of the data comparator when working in byte mode.

Since bytes and half-words can be accessed using a larger data width instruction, it is impossible to predict the exact value of the L-address lines when the requested byte/half-word is accessed, (e.g., if the matched byte is byte two of the word and it is accessed using a load word instruction), the L-address value will be of the word (byte zero). Therefore, the CPU masks the two least-significant bits of the L-address comparators whenever a word access is performed and the least-significant bit whenever a half-word access is performed.

Address range is supported only when aligned according to the access size. (See Section 23.2.1.3, "Examples").

23.2.1.3 Examples

- A fully supported scenario:
  - Looking for:
    Data size: Byte
    Address: 0x00000003
    Data value: greater than 0x07 and less than 0x0c
  - Programming options:
    One L-address comparator = 0x00000003 and program for equal
    One L-data comparator = 0x00000007 and program for greater than
    One L-data comparator = 0x0000000c and program for less than
    Both byte masks = 0xe
    Both L-data comparators program to byte mode
  - Result:

    The event will be correctly detected regardless of the load/store instruction the compiler chooses for this access
- A fully supported scenario:
  - Looking for:
    Data size: half-word
    Address: greater than 0x00000000 and less than 0x0000000c
    Data value: greater than 0x4e204e20 and less than 0x9c409c40
  - Programming option:
    One L-address comparator = 0x00000000 and program for greater than
    One L-address comparator = 0x0000000c and program for less than
    One L-data comparator = 0x4e204e20 and program for greater than
    One L-data comparator = 0x9c409c40 and program for less than
    Both byte masks = 0x0
    Both L-data comparators program to half-word mode
  - Result:

    The event will be correctly detected as long as the compiler does not use a load/store instruction with data size of byte.

Table 23-13. Debug Instructions / Data Shifted into Development Port Shift Register

Start	Mode	Control	Instruction / Data (32 Bits)		Function
			Bits 0:6	Bits 7:31	
1	0	0	CPU Instruction		Transfer Instruction to CPU
1	0	1	CPU Data		Transfer Data to CPU
1	1	0	Trap enable[1]	Does not exist	Transfer data to Trap Enable Control Register
1	1	1	0011111	Does not exist	Negate breakpoint requests to the CPU.
1	1	1	0	Does not exist	NOP

[1] Refer to Table 23-10

Data values in the last two functions other than those specified are reserved.

All transmissions from the debug port on DSDO begin with a “0” or “ready” bit. This indicates that the CPU is trying to read an instruction or data from the port. The external development tool must wait until it sees DSDO go low to begin sending the next transmission.

The control bit differentiates between instructions and data and allows the development port to detect that an instruction was entered when the CPU was expecting data and vice versa. If this occurs a sequence error indication is shifted out in the next serial transmission.

The trap enable function allows the development tool to transfer data to the trap enable control register.

The debug port command function allows the development tool to either negate breakpoint requests, reset the processor, activate or deactivate the fast down load procedure.

The NOP function provides a null operation for use when there is data or a response to be shifted out of the data register and the appropriate next instruction or command will be determined by the value of the response or data shifted out.

23.4.6.10 Serial Data Out of Development Port

The encoding of data shifted out of the development port shift register in debug mode (through the DSDO pin) is the same as for trap enable mode and is shown in Table 23-12.

Valid data encoding is used when data has been transferred from the CPU to the development port shift register. This is the result of an instruction to move the contents of a general purpose register to the debug port data register (DPDR). The valid data encoding has the highest priority of all status outputs and will be reported even if an interrupt occurs at the same time. Since it is not possible for a sequencing error to occur and also have valid data there is no priority conflict with the sequencing error status. Also, any interrupt that is recognized at the same time that there is valid data is not related to the execution of an

Table 25-2. MPC563 Boundary Scan Bit Definition (continued)

BSDL Bit	Cell Type	Pin/Port Name	BSDL Function	Safe Value	Control Cell	Disable Value	Disable Result	Pin Function	Pad Type
97	BC_7	A_AN56_PQA4	bidir	0	96	0	Z	IO	5vsa
98	BC_2	*	controlr	0					
99	BC_7	A_AN57_PQA5	bidir	0	98	0	Z	IO	5vsa
100	BC_2	*	controlr	0					
101	BC_7	A_AN58_PQA6	bidir	0	100	0	Z	IO	5vsa
102	BC_2	*	controlr	0					
103	BC_7	A_AN59_PQA7	bidir	0	102	0	Z	IO	5vsa
104	BC_2	*	controlr	0					
105	BC_7	B_AN0_ANW_PQB0	bidir	0	104	0	Z	IO	5vsa
106	BC_2	*	controlr	0					
107	BC_7	B_AN1_ANX_PQB1	bidir	0	106	0	Z	IO	5vsa
108	BC_2	*	controlr	0					
109	BC_7	B_AN2_ANY_PQB2	bidir	0	108	0	Z	IO	5vsa
110	BC_2	*	controlr	0					
111	BC_7	B_AN3_ANZ_PQB3	bidir	0	110	0	Z	IO	5vsa
112	BC_2	*	controlr	0					
113	BC_7	B_AN48_PQB4	bidir	0	112	0	Z	IO	5vsa
114	BC_2	*	controlr	0					
115	BC_7	B_AN49_PQB5	bidir	0	114	0	Z	IO	5vsa
116	BC_2	*	controlr	0					
117	BC_7	B_AN50_PQB6	bidir	0	116	0	Z	IO	5vsa
118	BC_2	*	controlr	0					
119	BC_7	B_AN51_PQB7	bidir	0	118	0	Z	IO	5vsa
120	BC_2	*	controlr	0					
121	BC_7	B_AN52_MA0_PQA0	bidir	0	120	0	Z	IO	5vsa
122	BC_2	*	controlr	0					
123	BC_7	B_AN53_MA1_PQA1	bidir	0	122	0	Z	IO	5vsa
124	BC_2	*	controlr	0					
125	BC_7	B_AN54_MA2_PQA2	bidir	0	124	0	Z	IO	5vsa
126	BC_2	*	controlr	0					
127	BC_7	B_AN55_PQA3	bidir	0	126	0	Z	IO	5vsa
128	BC_2	*	controlr	0					
129	BC_7	B_AN56_PQA4	bidir	0	128	0	Z	IO	5vsa
130	BC_2	*	controlr	0					
131	BC_7	B_AN57_PQA5	bidir	0	130	0	Z	IO	5vsa
132	BC_2	*	controlr	0					

configuration, and not again after that, the bank 1 entry table can be changed to the bank 0 entry table using the soft reset feature of the TPU3. This procedure is described in the following steps:

1. Set ETBANK field in TPUMCR2 to 0b01 to select the entry table in bank 1
2. Run the ID function
3. Stop the TPU3 by setting the STOP bit in the TPUMCR to one
4. Reset the TPU3 by setting the SOFTRST bit in the TPUMCR2 register
5. Wait at least nine clocks
6. Clear the SOFTRST bit in the TPUMCR2 register

The TPU3 stays in reset until the RCPU clears the SOFTRST bit. After the SOFTRST bit has been cleared, the TPU3 will be reset and the entry table in bank 0 will be selected by default. To select the bank 0 entry table, write 0b00 to the ETBANK field in TPUMCR2. Always initialize any write-once register to ensure that an incorrect value is not accidentally written.

The sections below document the bank 0 and bank 1 functions listed in Table D-1 of the TPU3 ROM module.

D.2 Programmable Time Accumulator (PTA)

PTA starts on a rising or falling edge and accumulates, over a programmable number of periods or pulses, a 32-bit sum of the total high time, low time, or input signal period. After the specified number of periods or pulses, the PTA generates an interrupt request.

One to 255 period measurements can be accumulated before the TPU3 interrupts the RCPU, providing instantaneous or average frequency measurement capability. See Freescale TPU Progamming Note *Programmable Time Accumulator TPU Function (PTA), (TPUPN06/D)*. Figure D-2 shows all of the host interface areas for the PTA function.

G.10.2 Keep-Alive RAM

$\overline{\text{PORESET}}$ or $\overline{\text{HRESET}}$ must be asserted during power-down prior to any supply dropping out of specified operating conditions.

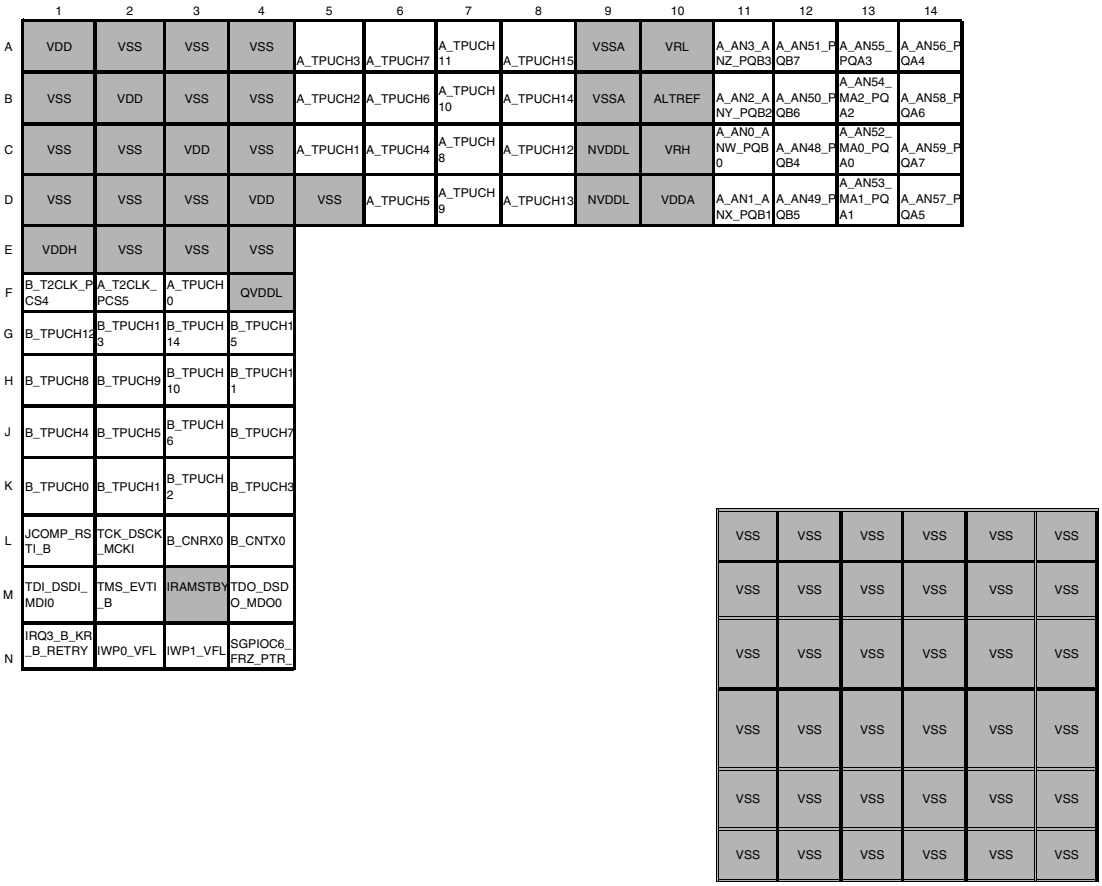
An additional constraint is placed on $\overline{\text{PORESET}}$ assertion since it is an asynchronous input. To assure that the assertion of $\overline{\text{PORESET}}$ does not potentially cause stores to keep-alive RAM to be corrupted (store single or store multiple) or non-coherent (store multiple), either of the following solutions is recommended:

- Assert $\overline{\text{HRESET}}$ at least 0.5 µs prior to when $\overline{\text{PORESET}}$ is asserted.
- Assert $\overline{\text{IRQ}}$0 (non-maskable interrupt) at least 0.5 µs prior to when $\overline{\text{PORESET}}$ is asserted. The service routine for $\overline{\text{IRQ}}$0 should not perform any writes to keep-alive RAM.

The amount of delay that should be added to $\overline{\text{PORESET}}$ assertion is dependent upon the frequency of operation and the maximum number of store multiples executed that are required to be coherent. If store multiples of more than 28 registers are needed and if the frequency of operation is lower that 66 MHz, the delay added to $\overline{\text{PORESET}}$ assertion will need to be greater than 0.5 µs. In addition, if KAPWR features are being used, $\overline{\text{PORESET}}$ should not be driven low while the V_{DDH} and V_{DDL} supplies are off.

G.11 AC Timing

Figure G-9 displays generic examples of MPC561/MPC563 timing. Specific timing diagrams are shown in Figure G-10 through Figure G-35.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	VDD	VSS	VSS	VSS	A_TPUCH3	A_TPUCH7	A_TPUCH11	A_TPUCH15	VSSA	VRL	A_AN3_ANZ_PQB3	A_AN51_PQB7	A_AN55_PQA3	A_AN56_PQA4
B	VSS	VDD	VSS	VSS	A_TPUCH2	A_TPUCH6	A_TPUCH10	A_TPUCH14	VSSA	ALTREF	A_AN2_ANY_PQB2	A_AN50_PQB6	A_AN54_MA2_PQA2	A_AN58_PQA6
C	VSS	VSS	VDD	VSS	A_TPUCH1	A_TPUCH4	A_TPUCH8	A_TPUCH12	NVDDL	VRH	A_AN0_ANW_PQB0	A_AN48_PQB4	A_AN52_MA0_PQA0	A_AN59_PQA7
D	VSS	VSS	VSS	VDD	VSS	A_TPUCH5	A_TPUCH9	A_TPUCH13	NVDDL	VDDA	A_AN1_ANX_PQB1	A_AN49_PQB5	A_AN53_MA1_PQA1	A_AN57_PQA5
E	VDDH	VSS	VSS	VSS										
F	B_T2CLK_PCS4	A_T2CLK_PCS5	A_TPUCH0	QVDDL										
G	B_TPUCH12	B_TPUCH13	B_TPUCH14	B_TPUCH15										
H	B_TPUCH8	B_TPUCH9	B_TPUCH10	B_TPUCH11										
J	B_TPUCH4	B_TPUCH5	B_TPUCH6	B_TPUCH7										
K	B_TPUCH0	B_TPUCH1	B_TPUCH2	B_TPUCH3										
L	JCOMP_RSTI_B	TCK_DSCK_MCKI	B_CNRX0	B_CNTX0										
M	TDI_DSDI_MDI0	TMS_EVTI_B	IRAMSTBY	TDO_DSDO_MDO0										
N	IRQ3_B_KR_B_RETRY	IWP0_VFL	IWP1_VFL	SGPIOC6_FRZ_PTR_										

VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS

Figure G-66. MPC561/MPC563 Ball Map (Black and White, page 1)