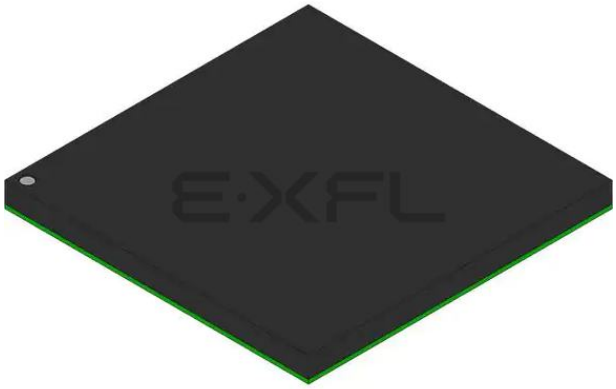

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Number of I/O	64
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 2.7V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	388-BBGA
Supplier Device Package	388-PBGA (27x27)
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Contents

Chapter 20
Dual-Port TPU3 RAM (DPTRAM)

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Table 2-10. Enhanced PCS 4 & 5 Pad Function

PDMCR2 [PCS5EN]	PDMCR2 [PCS4EN]	SHORT_REG [SH_T2CLK]	A_T2CLK/PCS5 PAD Function	B_T2CLK/PCS4 PAD Function	A_T2CLK internal TPU_A Connection	B_T2CLK internal TPU_B Connection
0	1	1	A_T2CLK	PCS4	A_T2CLK/PCS5 Pad	A_T2CLK/PCS5 Pad
1	0	0	PCS5	B_T2CLK	A_T2CLK Signal driven HI internally	B_T2CLK/PCS4 Pad
1	0	1	PCS5	B_T2CLK	A_T2CLK Signal driven HI internally	B_T2CLK Signal driven HI internally by connection to A_T2CLK
1	1	0	PCS5	PCS4	A_T2CLK Signal driven HI internally	B_T2CLK Signal driven HI internally
1	1	1	PCS5	PCS4	A_T2CLK Signal driven HI internally	B_T2CLK Signal driven HI internally by connection to A_T2CLK

1. If PCS4/5EN = 1 then A/B_T2CLK into the module is pulled up internally (enabling Div/8 clock, in gate mode).
2. If only PCS4EN=1, then A_T2CLK can be driven into B_T2CLK if PPM_SHORT[SH_T2CLK] is set.
3. If only PCS5EN=1 then A_T2CLK will be pulled up, if PPM_SHORT[SH_T2CLK] is set, then, B_T2CLK will be high regardless of pin state.

All of this is regardless of the Pull up/down state.

Note: The PPM shorting function has higher priority logic. If shorting is selected, then A_T2CLK → B_T2CLK. If A_T2CLK is selected as PCS then both A_T2CLK and B_T2CLK will be high regardless of B_T2CLK/PCS4 Pad state.

Table 2-11 details the functionality of the ETRIG1/PCS6 and ETRIG2/PCS7 pads dependent on the values of PDMCR2[PCS6EN], PDMCR2[PCS7EN], SHORT_REG [SH_ET1] and SHORT_REG [SH_ET2]. Also shown in this table is the internal connection of the ETRIG signals when the enhanced chip select function is used.

Table 5-1. USIU Address Map (continued)

Address	Register
0x2F C0FC–0x2F C0FF	Reserved
Memory Controller Registers	
0x2F C100	Base Register 0 (BR0) See Table 10-8 for bit descriptions.
0x2F C104	Option Register 0 (OR0) See Table 10-10 for bit descriptions.
0x2F C108	Base Register 1 (BR1) See Table 10-8 for bit descriptions.
0x2F C10C	Option Register 1 (OR1) See Table 10-10 for bit descriptions.
0x2F C110	Base Register 2 (BR2) See Table 10-8 for bit descriptions.
0x2F C114	Option Register 2 (OR2) See Table 10-10 for bit descriptions.
0x2F C118	Base Register 3 (BR3) See Table 10-8 for bit descriptions.
0x2F C11C	Option Register 3 (OR3) See Table 10-10 for bit descriptions.
0x2F C120–0x2F C13C	Reserved
0x2F C140	Dual-Mapping Base Register (DMBR) See Table 10-11 for bit descriptions.
0x2F C144	Dual-Mapping Option Register (DMOR) See Table 10-12 for bit descriptions.
0x2F C148–0x2F C174	Reserved
0x2F C178[1]	Memory Status (MSTAT) See Table 10-7 for bit descriptions.
0x2F C17A–0x2F C1FC	Reserved
System Integration Timers	
0x2F C200	Time Base Status and Control (TBSCR) See Table 6-18 for bit descriptions.
0x2F C204	Time Base Reference 0 (TBREF0) See Section 6.2.2.4.3, “Time Base Reference Registers (TBREF0 and TBREF1),” for bit descriptions.
0x2F C208	Time Base Reference 1 (TBREF1) See Section 6.2.2.4.3, “Time Base Reference Registers (TBREF0 and TBREF1),” for bit descriptions.
0x2F C20C–0x2F C21C	Reserved

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	IRM0[1]	LVM0	IRM1	LVM1	IRM2	LVM2	IRM3	LVM3	IRM4	LVM4	IRM5	LVM5	IRM6	LVM6	IRM7	LVM7
SRESET	0000_0000_0000_0000															
Addr	0x2F C014															

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	LSB 31
Field	—															
SRESET	0000_0000_0000_0000															

[1] IRQ0 of the SIPEND register is not affected by the setting or clearing of the IRM0 bit of the SIMASK register. IRQ0 is a non-maskable interrupt.

Figure 6-18. SIU Interrupt Mask Register (SIMASK)

6.2.2.2.5 SIU Interrupt Mask Register 2 (SIMASK2)

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	IRQ0[1]	LVL0	IMB IRQ0	IMB IRQ1	IMB IRQ2	IMB IRQ3	IRQ1	LVL1	IMB IRQ4	IMB IRQ5	IMB IRQ6	IMB IRQ7	IRQ2	LVL2	IMB IRQ8	IMB IRQ9
SRESET	0000_0000_0000_0000															
Addr	0x2F C048															

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	LSB 31
Field	IMB IRQ10	IMB IRQ11	IRQ3	LVL3	IMB IRQ12	IMB IRQ13	IMB IRQ14	IMB IRQ15	IRQ4	LVL4	IMB IRQ16	IMB IRQ17	IMB IRQ18	IMB IRQ19	IRQ5	LVL5
SRESET	0000_0000_0000_0000															

[1] $\overline{\text{IRQ0}}$ of the SIPEND2 register is not affected by the setting or clearing of the IRQ0 bit of the SIMASK2 register. $\overline{\text{IRQ0}}$ is a non-maskable interrupt

Figure 6-19. SIU Interrupt Mask Register 2 (SIMASK2)

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	RTCIRQ								SEC	ALR	—	4M	SIE	ALE	RTF	RTE
PORESET	0000_0000_000											U	000			U
Addr	0x2F C220															

Figure 6-35. Real-Time Clock Status and Control Register (RTCSC)

Table 6-19. RTCSC Bit Descriptions

Bits	Name	Description
0:7	RTCIRQ	Real-time clock interrupt request. Thee bits determine the interrupt priority level of the RTC. Refer to Section 6.1.4, “Enhanced Interrupt Controller” for interrupt level encoding.
8	SEC	Once per second interrupt. This status bit is set every second. It should be cleared by the software.
9	ALR	Alarm interrupt. This status bit is set when the value of the RTC equals the value programmed in the alarm register.
10	—	Reserved
11	4M	Real-time clock source 0 RTC assumes that it is driven by 20 MHz to generate the seconds pulse. 1 RTC assumes that it is driven by 4 MHz
12	SIE	Second interrupt enable. If this bit is set, the RTC generates an interrupt when the SEC bit is set.
13	ALE	Alarm interrupt enable. If this bit is set, the RTC generates an interrupt when the ALR bit is set.
14	RTF	Real-time clock freeze. If this bit is set, the RTC stops while FREEZE is asserted.
15	RTE	Real-time clock enable 0 RTC is disabled 1 RTC is enabled

6.2.2.4.6 Real-Time Clock Register (RTC)

The real-time clock register is a 32-bit read write register. It contains the current value of the real-time clock. A write to the RTC resets the seconds timer to zero. This register is locked after reset by default. Unlocking is accomplished by writing 0x55CC AA33 to its associated key register. See Section 8.8.3.2, “Keep-Alive Power Registers Lock Mechanism.”

	MSB 0	LSB 31
Field	RTC	
Reset	Unaffected	
Addr	0x2F C224	

Figure 6-36. Real-Time Clock Register (RTC)

Table 9-1. MPC561/MPC563 BIU Signals (continued)

Signal Name	Pins	Active	I/O	Description
$\overline{\text{BDIP}}$ Burst data in progress	1	Low	O	Driven by the MPC561/MPC563 when it owns the external bus. It is part of the burst protocol. When $\overline{\text{BDIP}}$ is asserted, the second beat in front of the current one is requested by the master. This signal is negated prior to the end of a burst to terminate the burst data phase early.
			I	Driven by an external master when it owns the external bus. When $\overline{\text{BDIP}}$ is asserted, the second beat in front of the current one is requested by the master. This signal is negated prior to the end of a burst to terminate the burst data phase early. The MPC561/MPC563 does not support burst accesses to internal slaves.
Transfer Start				
$\overline{\text{TS}}$ Transfer start	1	Low	O	Driven by the MPC561/MPC563 when it owns the external bus. Indicates the start of a transaction on the external bus.
			I	Driven by an external master when it owns the external bus. It indicates the start of a transaction on the external bus or (in show cycle mode) signals the beginning of an internal transaction.
Reservation Protocol				
$\overline{\text{CR}}$ Cancel reservation	1	Low	I	Each MPC500 CPU has its own $\overline{\text{CR}}$ signal. Assertion of $\overline{\text{CR}}$ instructs the bus master to clear its reservation; some other master has touched its reserved space. This is a pulsed signal.
$\overline{\text{KR}}$ Kill reservation	1	Low	I	In case of a bus cycle initiated by a STWCX instruction issued by the RCPU to a non-local bus on which the storage reservation has been lost, this signal is used by the non-local bus interface to back-off the cycle. Refer to Section 9.5.10, “Storage Reservation” for details.

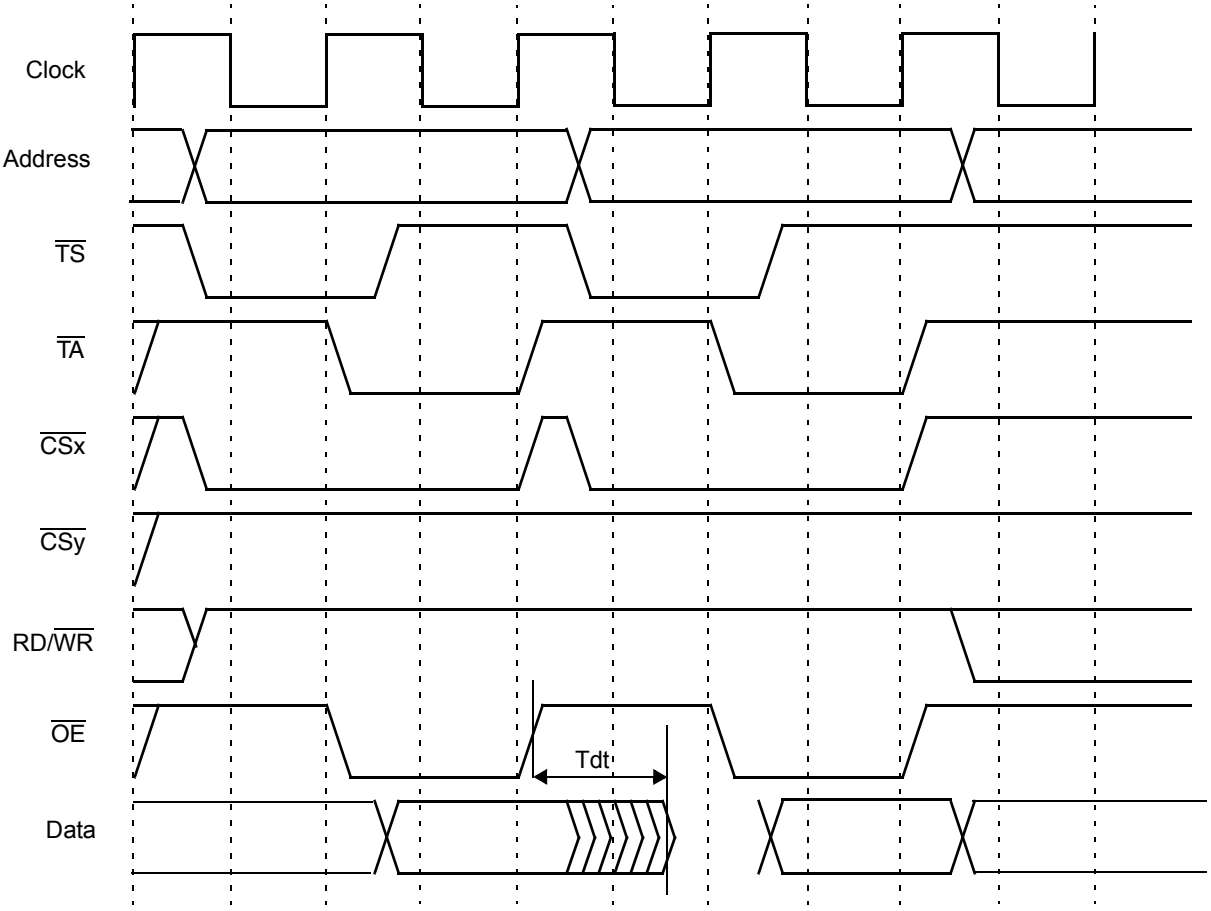

Figure 10-18. Consecutive Accesses (Read After Read from Same Bank, EHTR = 1)

10.3.5 Summary of GPCM Timing Options

Table 10-3 summarizes the different combinations of timing options.

Table 10-3. Programming Rules for Timing Strobes

TRLX	Access Type	ACS	CSNT	Address to CS Asserted	CS Negated to Add/Data Invalid	Address to WE/BE or OE Asserted	WE/BE Negated to Add/Data Invalid	OE Negated to Add/Data Invalid	Total Number of Cycles
0	read	00	X	0	1/4 * clock	3/4 * clock	X	1/4 * clock	2 + SCY
0	read	10	X	1/4 * clock	1/4 * clock	3/4 * clock	X	1/4 * clock	2 + SCY
0	read	11	X	1/2 * clock	1/4 * clock	3/4 * clock	X	1/4 * clock	2 + SCY
0	write	00	0	0	1/4 * clock	3/4 * clock	1/4 * clock	X	2 + SCY
0	write	10	0	1/4 * clock	1/4 * clock	3/4 * clock	1/4 * clock	X	2 + SCY
0	write	11	0	1/2 * clock	1/4 * clock	3/4 * clock	1/4 * clock	X	2 + SCY
0	write	00	1	0	1/4 * clock	3/4 * clock	1/2 * clock	X	2 + SCY
0	write	10	1	1/4 * clock	1/2 * clock	3/4 * clock	1/2 * clock	X	2 + SCY

Table 14-4 shows the total number of analog input channels supported with zero to four external multiplexer chips using one QADC module.

Table 14-4. Analog Input Channels

Number of Analog Input Channels Available Directly Connected + External Multiplexed = Total Channels				
No External MUX Chips	**One External MUX Chip**	**Two External MUX Chips**	**Three External MUX Chips**	**Four External MUX Chips**
16	20	27	34	41

NOTE: QADC64E External MUX Users

If a QADC64E module is in external multiplexing (EMUX) mode then the multiplexer address signal channels AN[52:54] should *not* be programmed into queues.

14.3 Programming the QADC64E Registers

The QADC64E has three global registers for configuring module operation.

- The module configuration register, QADCMCR (Section 14.3.1, “QADC64E Module Configuration Register”)
- The interrupt register, QADCINT (Section 14.3.2, “QADC64E Interrupt Register”)
- The test register, QADCTEST. This register is used for factory test only.

These global registers are always defined to be in supervisor-only data space. Refer to Table 14-1 for the QADC64E_A Address Map and Table 14-2 for QADC64E_B Address Map. See Section 14.3.1.4, “Supervisor/Unrestricted Address Space” for access modes for these registers.

The remaining five registers in the control register block control the operation of the queuing mechanism, and provide a means of monitoring the operation of the QADC64E.

- Control register 0 (QACR0) contains hardware configuration information (Section 14.3.5, “Control Register 0”)
- Control register 1 (QACR1) is associated with queue 1 (Section 14.3.6, “Control Register 1”)
- Control register 2 (QACR2) is associated with queue 2 (Section 14.3.7, “Control Register 2”)
- Status registers (QASR0 and QASR1) provide visibility on the status of each queue and the particular conversion that is in progress (Section 14.3.8, “Status Registers (QASR0 and QASR1)”)

The Conversion Command Word (CCW) table contains 64 entries to hold the software programmable analog conversion sequences. Each CCW table entry is a 16-bit entry, though only 10 bits are used.

The final block of address space belongs to the result word table, which appears in three places in the memory map. Each result word table location holds one 10-bit conversion value.

generated internally and the QADC64E immediately begins execution of the first CCW in the queue. If a pause occurs, another trigger event is generated internally, and then execution continues without pausing.

The QADC64E automatically performs the conversions in the queue until an end-of-queue condition is encountered. The queue remains idle until the software again sets the single-scan enable bit. While the time to internally generate and act on a trigger event is very short, software can momentarily read the status conditions, indicating that the queue is paused. The trigger overrun flag is never set while in the software initiated single-scan mode.

The software initiated single-scan mode is useful in the following applications:

- Allows software complete control of the queue execution
- Allows the software to easily alternate between several queue sequences.

14.4.4.3.2 External Trigger Single-Scan Mode

The external trigger single-scan mode is available on both queue 1 and queue 2. The software programs the polarity of the external trigger edge that is to be detected, either a rising or a falling edge. The software must enable the scan to occur by setting the single-scan enable bit for the queue.

The first external trigger edge causes the queue to be executed one time. Each CCW is read and the indicated conversions are performed until an end-of-queue condition is encountered. After the queue is completed, the QADC64E clears the single-scan enable bit. Software may set the single-scan enable bit again to allow another scan of the queue to be initiated by the next external trigger edge.

The external trigger single-scan mode is useful when the input trigger rate can exceed the queue execution rate. Analog samples can be taken in sync with an external event, even though the software is not interested in data taken from every edge. The software can start the external trigger single-scan mode and get one set of data, and at a later time, start the queue again for the next set of samples.

When a pause bit is encountered during external trigger single-scan mode, another trigger event is required for queue execution to continue. Software involvement is not needed to enable queue execution to continue from the paused state.

14.4.4.3.3 External Gated Single-Scan Mode

The QADC64E provides external gating for queue 1 only. When external gated single-scan mode is selected, the input level on the associated external trigger signal enables and disables queue execution. The polarity of the external gated signal is fixed so only a high level opens the gate and a low level closes the gate. Once the gate is open, each CCW is read and the indicated conversions are performed until the gate is closed. Software must enable the scan to occur by setting the single-scan enable bit for queue 1. If a pause in a CCW is encountered, the pause flag *will not set,* and execution continues without pausing.

While the gate is open, queue 1 executes one time. Each CCW is read and the indicated conversions are performed until an end-of-queue condition is encountered. When queue 1 completes, the QADC64E sets the completion flag (CF1) and clears the single-scan enable bit. Software may set the single-scan enable bit again to allow another scan of queue 1 to be initiated during the next open gate.

If the gate closes before queue 1 completes execution, the current CCW completes, execution of queue 1 stops, the single-scan enable bit is cleared, and the PF1 bit is set. Software can read the CWPQ1 to

Table 15-26. SCxSR Bit Descriptions (continued)

Bits	Name	Description
12	OR	Overrun error. OR is set when a new byte is ready to be transferred from the receive serial shifter to register RDRx, and RDRx is already full (RDRF is still set). Data transfer is inhibited until OR is cleared. Previous data in RDRx remains valid, but additional data received during an overrun condition (including the byte that set OR) is lost. Note that whereas the other receiver status flags (NF, FE, and PF) reflect the status of data already transferred to RDRx, the OR flag reflects an operational condition that resulted in a loss of data to RDRx. 0 RDRF is cleared before new data arrives. 1 RDRF is not cleared before new data arrives.
13	NF	Noise error flag. NF is set when the receiver detects noise on a valid start bit, on any of the data bits, or on the stop bit(s). It is not set by noise on the idle line or on invalid start bits. Each bit is sampled three times for noise. If the three samples are not at the same logic level, the majority value is used for the received data value, and NF is set. NF is not set until the entire frame is received and RDRF is set. Although no interrupt is explicitly associated with NF, an interrupt can be generated with RDRF, and the interrupt handler can check NF. 0 No noise detected in the received data. 1 Noise detected in the received data. For receiver queue operation NF is cleared when SCxSR is read with NF set, followed by a read of SCRQ[0:15].
14	FE	Framing error. FE is set when the receiver detects a zero where a stop bit (one) was expected. A framing error results when the frame boundaries in the received bit stream are not synchronized with the receiver bit counter. FE is not set until the entire frame is received and RDRF is set. Although no interrupt is explicitly associated with FE, an interrupt can be generated with RDRF, and the interrupt handler can check FE. 0 No framing error detected in the received data. 1 Framing error or break detected in the received data.
15	PF	Parity error. PF is set when the receiver detects a parity error. PF is not set until the entire frame is received and RDRF is set. Although no interrupt is explicitly associated with PF, an interrupt can be generated with RDRF, and the interrupt handler can check PF. 0 No parity error detected in the received data. 1 Parity error detected in the received data.

15.7.5 SCI Data Register (SCxDR)

The SCxDR consists of two data registers located at the same address. The receive data register (RDRx) is a read-only register that contains data received by the SCI serial interface. Data is shifted into the receive serial shifter and is transferred to RDRx. The transmit data register (TDRx) is a write-only register that contains data to be transmitted. Data is first written to TDRx, then transferred to the transmit serial shifter, where additional format bits are added before transmission.

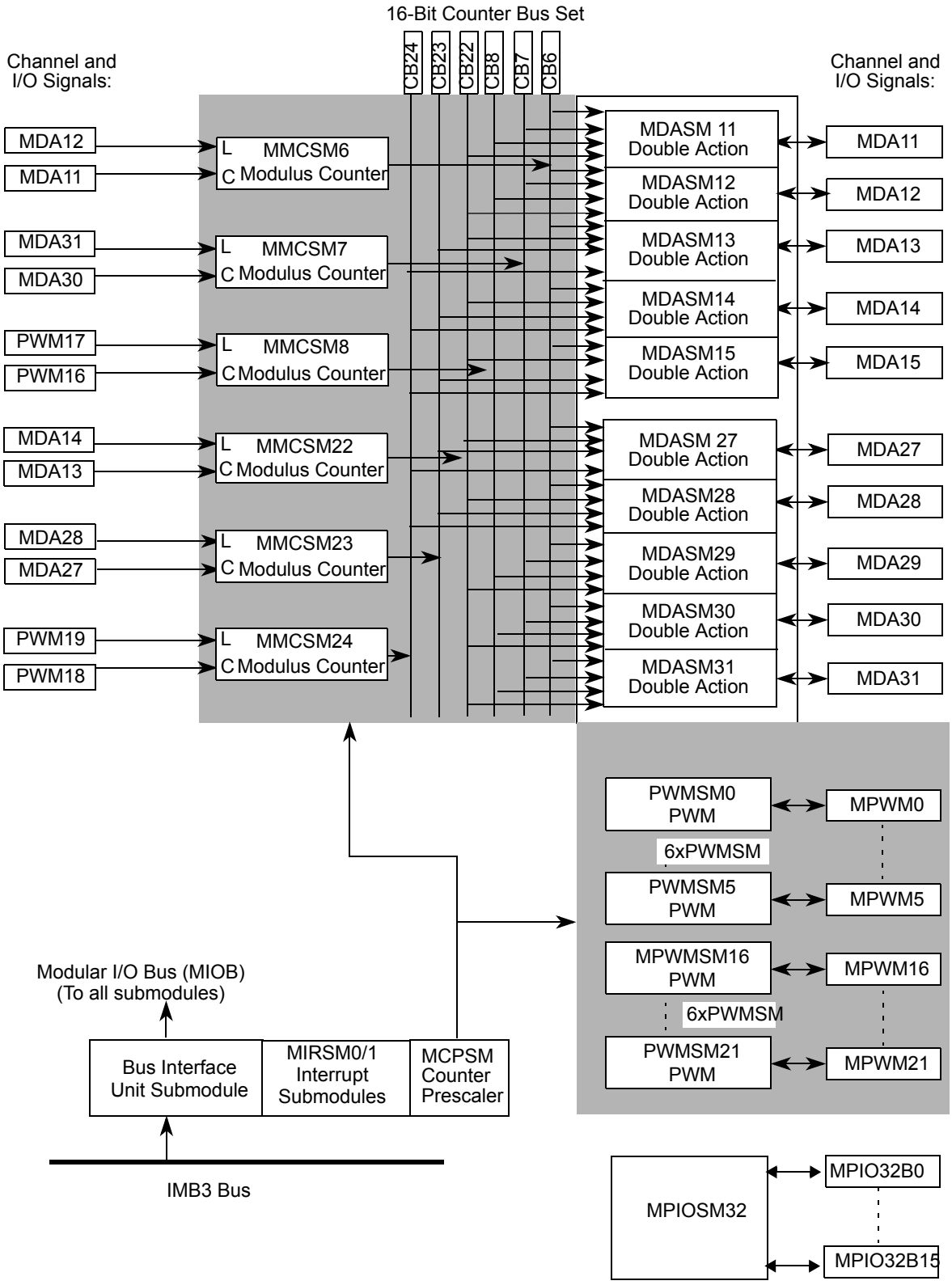

Figure 17-1. MPC561/MPC563 MIOS14 Block Diagram

21.2 Programming Model

The UC3F EEPROM module consists of a control register block, an addressable shadow row implemented in Flash, and an addressable main Flash memory array. The control registers are used to configure, program, erase and exercise the UC3F shadow row and Flash array.

21.2.1 UC3F EEPROM Control Registers

These supervisor-level control registers are used to control UC3F EEPROM module operation. On reset, the registers are loaded with default reset information. Several bits of the UC3F control registers are special Flash NVM registers which retain their state when power is removed from the UC3F EEPROM. These special NVM registers are identified in the individual register field and control bit descriptions.

21.2.1.1 Register Addressing

The UC3F module control registers, shown in Table 21-2, are selected with individual register selects generated from the BIU. As such, each Flash module that is designed using the UC3F EEPROM module may uniquely define the addressing of the control register block.

Table 21-2. UC3F Register Programming Model

Address	Register
0x2F C800	Module Configuration (UC3FMCR)
0x2F C804	Extended Module Configuration (UC3FMCRE)
0x2F C808	High Voltage Control (UC3FCTL)
0x2F C80C	Reserved

21.2.1.2 UC3F EEPROM Configuration Register (UC3FMCR)

The UC3F module configuration register is used to configure the operation and access restrictions of the UC3F array and shadow row.

MSB

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	STOP	$\overline{\text{LOCK}}$	—	FIC	SIE	ACCESS	CENSOR		SUPV							
$\overline{\text{HRESET}}$	0	1	0	0	0	0	1[1]	1[1]	1	1	1	1	1	1	1	1
Addr	0x2F C800															

LSB

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Field	DATA								PROTECT							
$\overline{\text{HRESET}}$	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

[1] Reset state determined by NVM registers. These bits will be set to 01 by the factory.

Figure 21-2. UC3F EEPROM Configuration Register (UC3FMCR)

Table 24-3. Terms and Definitions (continued)

Term	Description
Instruction Taken	An instruction is taken after it has been issued and recognized by the appropriate execution unit. All resources to perform the instruction are ready, and the processor begins to execute it.
Instruction Retire	Completion of the instruction issue, execution and writeback stages. An instruction is ready to be retired if it completes without generating an exception and all instructions ahead of it in history buffer have completed without generating an exception.
ICTRL	Instruction bus support control register (Refer to Table 23.6.11)
Ownership Trace Message (OTM)	Visibility of process/function that is currently executing.
Public Messages	Messages on the auxiliary signals for accomplishing common visibility and controllability requirements e.g. DRM and DWM.
RCPU	Processor that implements the PowerPC-based architecture used in the Freescale MPC500 family of microcontrollers.
READI	Real time Embedded Applications Development Interface.
READI signals	Refers to IEEE-ISTO 5001 auxiliary port.
RPM	Reduced Port Mode. This is the reduced port mode for READI.
run-time	RCPU is executing program code in normal mode
Sequential Instruction	Any instruction other than a flow-control instruction or isync.
Snooping	Monitoring addresses driven by a bus master to detect the need for coherency actions.
Standard	The phrase “according to the standard” implies according the IEEE-ISTO 5001 - 1999.
Superfield	One or more message “fields” delimited by $\overline{\text{MSEO}}$/$\overline{\text{MSEI}}$ assertion/negation. The information transmitted between “start-message” and “end-packet” states.
Show Cycle	An internal access (e.g., to an internal memory) reflected on the external bus using a special cycle (marked with a dedicated transfer code). For an internal memory “hit,” an address-only bus cycle is generated; for an internal memory “miss,” a complete bus cycle is generated.
Transfer Code (TCODE)	Message header that identifies the number and/or size of packets to be transferred, and how to interpret each of the packets.
TCK / DSCK / MCKI	Multiplexed signal: JTAG Clock or Development Port Clock. MCKI is a READI signal on the MPC561/MPC563
TDI / DSDI / MDI0	Multiplexed signal: JTAG Data In or Development Port Serial Data In. MDI0 is a READI signal on the MPC561/MPC563.
TDO / DSDO / MDO0	Multiplexed signal: JTAG Data Out or Development Port Serial Data Out. MDO0 is a READI signal on the MPC561/MPC563
Upload	Device sends information to the tool.
VSYNC	Internal RCPU signal
VF	Internal RCPU signal which indicates instruction queue status.
VFLS	Internal RCPU signal which indicates history buffer flush status.

Table 25-1. MPC561 Boundary Scan Bit Definition (continued)

BSDL Bit	Cell Type	Pin/Port Name	BSDL Function	Safe Value	Control Cell	Disable Value	Disable Result	Pin Function	Pad Type
170	BC_2	*	controlr	0					
171	BC_7	MPWM17_MDO3	bidir	0	170	0	Z	IO	26v5vs
172	BC_2	*	controlr	0					
173	BC_7	MPWM18_MDO6	bidir	0	172	0	Z	IO	26v5vs
174	BC_2	*	controlr	0					
175	BC_7	MPWM19_MDO7	bidir	0	174	0	Z	IO	26v5vs
176	BC_2	*	controlr	0					
177	BC_7	MPIO32B5_MDO5	bidir	0	176	0	Z	IO	26v5vs
178	BC_2	*	controlr	0					
179	BC_7	MPIO32B6_MPWM4_MDO6	bidir	0	178	0	Z	IO	26v5vs
180	BC_2	*	controlr	0					
181	BC_7	MPIO32B7_MPWM5	bidir	0	180	0	Z	IO	5vsa
182	BC_2	*	controlr	0					
183	BC_7	MPIO32B8_MPWM20	bidir	0	182	0	Z	IO	5vsa
184	BC_2	*	controlr	0					
185	BC_7	MPIO32B9_MPWM21	bidir	0	184	0	Z	IO	5vsa
186	BC_2	*	controlr	0					
187	BC_7	MPIO32B10_PPM_TSYNC	bidir	0	186	0	Z	IO	26v5vs
188	BC_2	*	controlr	0					
189	BC_7	MPIO32B11_C_CNRX0	bidir	0	188	0	Z	IO	5vfa
190	BC_2	*	controlr	0					
191	BC_7	MPIO32B12_C_CNTX0	bidir	0	190	0	Z	IO	5vfa
192	BC_2	*	controlr	0					
193	BC_7	MPIO32B13_PPM_TCLK	bidir	0	192	0	Z	IO	26v5vs
194	BC_2	*	controlr	0					
195	BC_7	MPIO32B14_PPM_RX0	bidir	0	194	0	Z	IO	26v5vs
196	BC_2	*	controlr	0					
197	BC_7	MPIO32B15_PPM_TX0	bidir	0	196	0	Z	IO	26v5vs
198	BC_2	*	controlr	0					
199	BC_7	VF0_MPIO32B0_MDO1	bidir	0	198	0	Z	IO	26v5vs
200	BC_2	*	controlr	0					
201	BC_7	VF1_MPIO32B1_MCKO	bidir	0	200	0	Z	IO	26v5vs
202	BC_2	*	controlr	0					
203	BC_7	VF2_MPIO32B2_MSEI_B	bidir	0	202	0	Z	IO	26v5vs
204	BC_2	*	controlr	0					

Table 25-2. MPC563 Boundary Scan Bit Definition (continued)

BSDL Bit	Cell Type	Pin/Port Name	BSDL Function	Safe Value	Control Cell	Disable Value	Disable Result	Pin Function	Pad Type
25	BC_7	B_TPUCH10	bidir	0	24	0	Z	IO	5vsa
26	BC_2	*	controlr	0					
27	BC_7	B_TPUCH11	bidir	0	26	0	Z	IO	5vsa
28	BC_2	*	controlr	0					
29	BC_7	B_TPUCH12	bidir	0	28	0	Z	IO	5vsa
30	BC_2	*	controlr	0					
31	BC_7	B_TPUCH13	bidir	0	30	0	Z	IO	5vsa
32	BC_2	*	controlr	0					
33	BC_7	B_TPUCH14	bidir	0	32	0	Z	IO	5vsa
34	BC_2	*	controlr	0					
35	BC_7	B_TPUCH15	bidir	0	34	0	Z	IO	5vsa
36	BC_2	*	controlr	0					
37	BC_7	B_T2CLK_PCS4	bidir	0	36	0	Z	IO	5vfa
38	BC_2	*	controlr	0					
39	BC_7	A_T2CLK_PCS5	bidir	0	38	0	Z	IO	5vfa
40	BC_2	*	controlr	0					
41	BC_7	A_TPUCH0	bidir	0	40	0	Z	IO	5vsa
42	BC_2	*	controlr	0					
43	BC_7	A_TPUCH1	bidir	0	42	0	Z	IO	5vsa
44	BC_2	*	controlr	0					
45	BC_7	A_TPUCH2	bidir	0	44	0	Z	IO	5vsa
46	BC_2	*	controlr	0					
47	BC_7	A_TPUCH3	bidir	0	46	0	Z	IO	5vsa
48	BC_2	*	controlr	0					
49	BC_7	A_TPUCH4	bidir	0	48	0	Z	IO	5vsa
50	BC_2	*	controlr	0					
51	BC_7	A_TPUCH5	bidir	0	50	0	Z	IO	5vsa
52	BC_2	*	controlr	0					
53	BC_7	A_TPUCH6	bidir	0	52	0	Z	IO	5vsa
54	BC_2	*	controlr	0					
55	BC_7	A_TPUCH7	bidir	0	54	0	Z	IO	5vsa
56	BC_2	*	controlr	0					
57	BC_7	A_TPUCH8	bidir	0	56	0	Z	IO	5vsa
58	BC_2	*	controlr	0					
59	BC_7	A_TPUCH9	bidir	0	58	0	Z	IO	5vsa
60	BC_2	*	controlr	0					

Table B-14. TouCAN A, B and C (CAN 2.0B Controller) (continued)

Address	Access	Symbol	Register	Size	Reset
0x30 74A2	S/U	IMASK_B	TouCAN_B Interrupt Masks	16	S
0x30 74A4	S/U	IFLAG_B	TouCAN_B Interrupt Flags	16	S
0x30 74A6	S/U	RXECTR_B/ TXECTR_B	TouCAN_B Receive Error Counter/ TouCAN_B Transmit Error Counter	16	S
0x30 7500 — 0x30 750F	S/U	MBUFF0_B[1]	TouCAN_B Message Buffer 0.	—	U
0x30 7510 — 0x30 751F	S/U	MBUFF1_B[1]	TouCAN_B Message Buffer 1.	—	U
0x30 7520 — 0x30 752F	S/U	MBUFF2_B[1]	TouCAN_B Message Buffer 2.	—	U
0x30 7530 — 0x30 753F	S/U	MBUFF3_B[1]	TouCAN_B Message Buffer 3.	—	U
0x30 7540 — 0x30 754F	S/U	MBUFF4_B[1]	TouCAN_B Message Buffer 4.	—	U
0x30 7550 — 0x30 755F	S/U	MBUFF5_B[1]	TouCAN_B Message Buffer 5.	—	U
0x30 7560 — 0x30 756F	S/U	MBUFF6_B[1]	TouCAN_B Message Buffer 6.	—	U
0x30 7570 — 0x30 757F	S/U	MBUFF7_B[1]	TouCAN_B Message Buffer 7.	—	U
0x30 7580 — 0x30 758F	S/U	MBUFF8_B[1]	TouCAN_B Message Buffer 8.	—	U
0x30 7590 — 0x30 759F	S/U	MBUFF9_B[1]	TouCAN_B Message Buffer 9.	—	U
0x30 75A0 — 0x30 75AF	S/U	MBUFF10_B[1]	TouCAN_B Message Buffer 10.	—	U
0x30 75B0 — 0x30 75BF	S/U	MBUFF11_B[1]	TouCAN_B Message Buffer 11.	—	U
0x30 75C0 — 0x30 75CF	S/U	MBUFF12_B[1]	TouCAN_B Message Buffer 12.	—	U
0x30 75D0 — 0x30 75DF	S/U	MBUFF13_B[1]	TouCAN_B Message Buffer 13.	—	U
0x30 75E0 — 0x30 75EF	S/U	MBUFF14_B[1]	TouCAN_B Message Buffer 14.	—	U
0x30 75F0 — 0x30 75FF	S/U	MBUFF15_B[1]	TouCAN_B Message Buffer 15.	—	U
TouCAN_C					
0x30 7880	S	CANMCR_C	TouCAN_C Module Configuration Register	16	S
0x30 7882	T	CANTCR_C	TouCAN_C Test Register	16	S

CONTROL BITS

	NAME	OPTIONS	ADDRESSES
0 1 2 3	Channel Function Select	xxxx – DIO Function Number. Assigned during microcode assembly. See Table D-1	0x30YY0C – 0x30YY12
0 1	Host Sequence	00 – Update on Transition 01 – Update at Match Rate 10 – Update on HSR 11 11 – Not Used	0x30YY14 – 0x30YY16
0 1	Host Service Request	00 – Not Used 01 – Drive Pin High 10 – Drive Pin Low 11 – Initialize	0x30YY18 – 0x30YY1A
0 1	Channel Priority	00 – Disabled 01 – Low Priority 10 – Medium Priority 11 – High Priority	0x30YY1C – 0x30YY1E
0	Channel Interrupt Enable	0 – Channel Interrupt Disabled 1 – Channel Interrupt Enabled	0x30YY0A
0	Channel Interrupt Status	0 – Channel Interrupt Not Asserted 1 – Channel Interrupt Asserted	0x30YY20

PARAMETER RAM

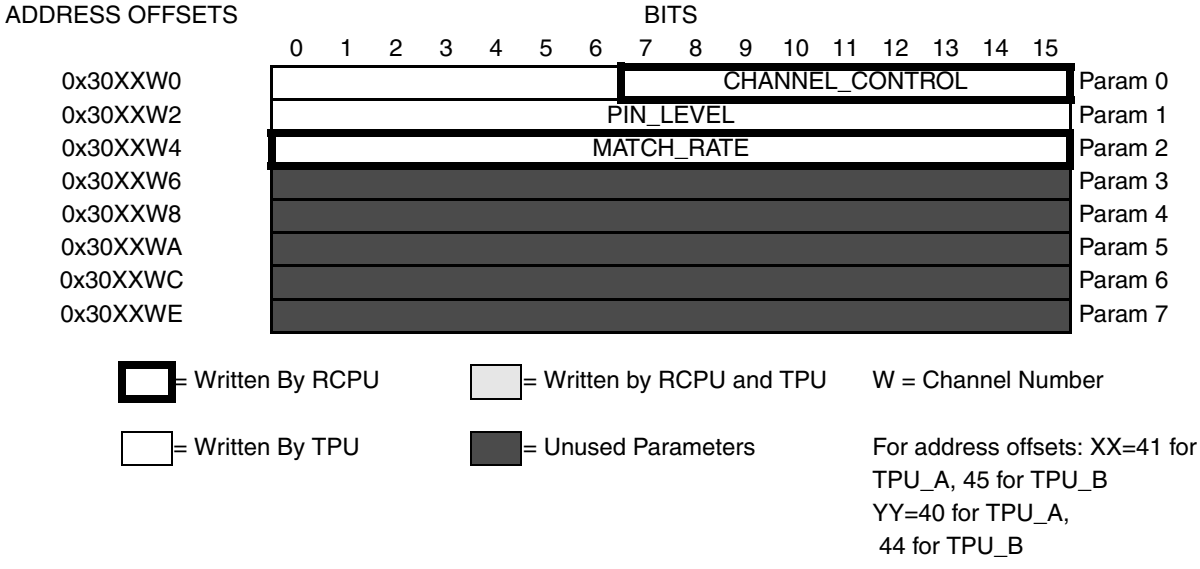

Figure D-28. DIO Parameters