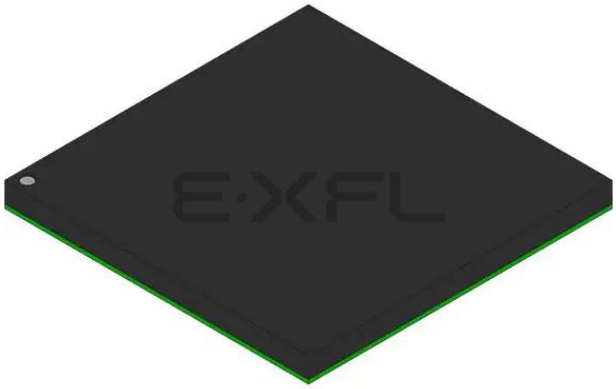

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Details	
Product Status	Active
Core Processor	PowerPC
Core Size	32-Bit Single-Core
Speed	56MHz
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Peripherals	POR, PWM, WDT
Number of I/O	64
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 2.7V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	388-BBGA
Supplier Device Package	388-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc562mzp56

Table 2-1. MPC561/MPC563 Signal Descriptions (continued)

Signal Name	No. of Signals	Type	Function after Reset[1]	Description
JTAG/BDM/READI				
TMS / $\overline{\text{EVTI}}$	1	I	TMS unless the Nexus (READI) port is enabled, then $\overline{\text{EVTI}}$. See Section 2.5.	Test Mode Select. This input controls test mode operations for on-board test logic (JTAG).
		I		$\overline{\text{EVTI}}$. Event in ($\overline{\text{EVTI}}$) is level sensitive when configured for breakpoint generation, otherwise it is edge sensitive.
TDI / DSDI / MDI0	1	I	DSDI unless the Nexus (READI) port (MDI0) or JTAG mode (TDI) is enabled. See Section 2.5.	Test Data In. This input is used for serial test instructions and test data for on-board test logic (JTAG).
		I		Development Serial Data Input. This input signal is the data in for the debug port interface. See Chapter 23, "Development Support," for details.
		I		Message Data In. MDI0 is a Nexus input signal used for downloading configuration information, writes to user resources, and so forth. Internal latching of MDI occurs on the rising edge of MCKI.
TCK / DSCK / MCKI	1	I	DSCK unless the Nexus (READI) port (MCKI) or JTAG mode (TCK) is enabled. See Section 2.5.	Test Clock. This input provides a clock for on-board test logic (JTAG).
		I		Development Serial Clock. This input signal is the clock for the debug port interface. See Chapter 23, "Development Support," for details.
		I		Message Clock In. This input line is the input clock to the READI module for the Nexus message clock input.
TDO / DSDO / MDO0	1	O	DSDO unless the Nexus (READI) port (MDO0) or JTAG mode (TDO) is enabled. See Section 2.5.	Test Data Out. This output is used for serial test instructions and test data for on-board test logic (JTAG).
		O		Development Serial Data Output. This output signal is the data-out line of the debug port interface. See Chapter 23, "Development Support," for details.
		O		READI Message Data Out. Message data out: MDO0 is an output signal used for uploading OTM, BTM, DTM, and read/write accesses. External latching of MDO occurs on rising edge of MCKO. Eight MDO signals are implemented.
JCOMP / $\overline{\text{RSTI}}$	1	I	See Section 2.5.	JTAG Compliancy. This signal enables the IEEE1149.1 JTAG compliant circuitry in the MPC561/MPC563. 0 JTAG disabled 1 JTAG enabled
		I		$\overline{\text{RSTI}}$. Reset input for the Nexus port.

Table 2-1. MPC561/MPC563 Signal Descriptions (continued)

Signal Name	No. of Signals	Type	Function after Reset[1]	Description
MPIO32B12 / C_CNTX0[6]	1	I/O	MPIO32B12	MIOS14 GPIO 12. This function allows the signals to be used as general-purpose inputs/outputs.
		O		TouCAN_C Transmit Data. This is the serial data output signal for the TouCAN_C module.
MPIO32B13 / PPM_TCLK	1	I/O	MPIO32B13	MIOS14 GPIO 13. This function allows the signals to be used as general-purpose inputs/outputs.
		O		PPM_TCLK. PPM bus clock
MPIO32B14 / PPM_RX0	1	I/O	MPIO32B14	MIOS14 GPIO 14. This function allows the signals to be used as general-purpose inputs/outputs.
		I		PPM_RX0. Receive data to the PPM channel number 0.
MPIO32B15 / PPM_TX0	1	I/O	MPIO32B15	MIOS14 GPIO 15. This function allows the signals to be used as general-purpose inputs/outputs.
		O		PPM_TX0. Transmit data from PPM channel number 0.
TPU				
A_TPUCH[0:15]	16	I/O	A_TPUCH[0:15]	Provides TPU module A with 16 input/output programmable timed events.
A_T2CLK / PCS5	1	I/O	A_T2CLK	This signal is used to clock or gate the timer count register 2 (TCR2) within the TPU module A. This signal is an output-only in special test mode.
		O		PCS5. This signal provides QSPI peripheral chip select when the enhanced PCS mode is selected.
B_TPUCH[0:15]	16	I/O	B_TPUCH[0:15]	Provides TPU module B with 16 input/output programmable timed events.
B_T2CLK / PCS4	1	I/O	B_T2CLK	This signal is used to clock or gate the timer count register 2 (TCR2) within the TPU module B. This signal is an output-only in special test mode.
		O		PCS4. This signal provides QSPI peripheral chip select when the enhanced PCS mode is selected.
Global Power				
NVDDL	1	I	NVDDL	NVDDL. Noisy 2.6-V voltage supply input. This signal supplies the final output stage of the 2.6-V pad output drivers. The NVDDL and QVDDL supplies should be connected to the same power supply in a user's system.
QVDDL	1	I	QVDDL	QVDDL. Quiet 2.6-V voltage supply input. This signal supplies all pad logic and pre-driver circuitry, except for the final output stage of the 2.6-V pad output drivers. The NVDDL and QVDDL supplies should be connected to the same power supply in a user's system.
VDDH	1	I	VDDH	VDDH. 5-V voltage supply input.
VDD	1	I	VDD	VDD. 2.6-V voltage supply input for internal logic.
KAPWR	1	I	KAPWR	Keep-Alive Power. 2.6-V voltage supply input for the oscillator and keep-alive registers.

Table 3-10. Integer Exception Register Bit Descriptions

Bits	Name	Description
2	CA	Carry (CA). In general, the carry bit is set to indicate that a carry out of bit 0 occurred during execution of an instruction. Add carrying, subtract from carrying, add extended, and subtract from extended instructions set CA if there is a carry out of bit 0, and clear it otherwise. The CA bit is not altered by compare instructions or other instructions that cannot carry, except that shift right algebraic instructions set the CA bit to indicate whether any ‘1’ bits have been shifted out of a negative quantity.
3:24	—	Reserved
25:31	BYTES	This field specifies the number of bytes to be transferred by a Load String Word Indexed (lswx) or Store String Word Indexed (stswx) instruction.

3.7.6 Link Register (LR)

The link register (LR), SPR 8, supplies the branch target address for the branch conditional to link register (bclrx) instruction, and can be used to hold the logical address of the instruction that follows a branch and link instruction.

Note that although the two least-significant bits can accept any values written to them, they are ignored when the LR is used as an address.

Both conditional and unconditional branch instructions include the option of placing the effective address of the instruction after the branch instruction in the LR. This is done regardless of whether the branch is taken.

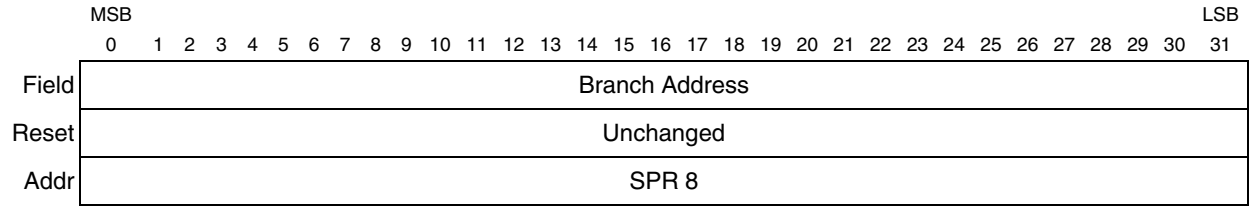


Figure 3-9. Link Register (LR)

3.7.7 Count Register (CTR)

The count register (CTR), SPR 9, is used to hold a loop count that can be decremented during execution of branch instructions with an appropriately coded BO field. If the value in CTR is 0 before being decremented, it is –1 afterward. The count register provides the branch target address for the branch conditional to count register (bcctrx) instructio

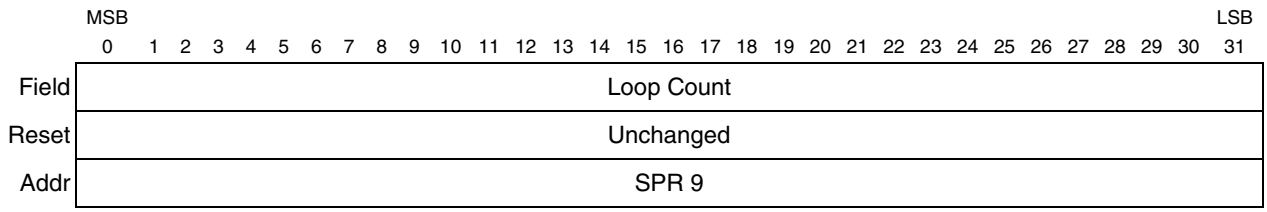


Figure 3-10. Count Register (CTR)

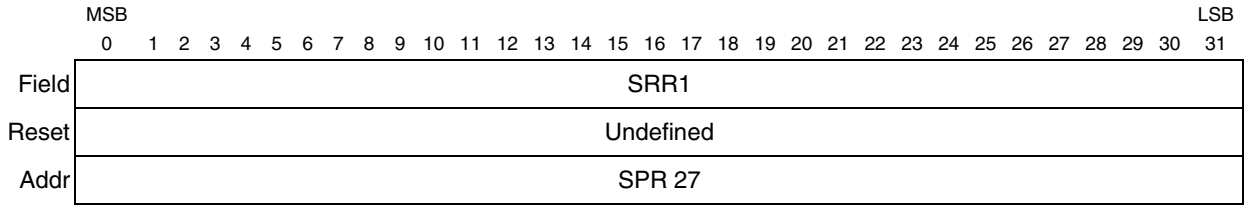


Figure 3-15. Machine Status Save/Restore Register 1 (SRR1)

In general, when an exception occurs, SRR1[0:15] are loaded with exception-specific information, and MSR[16:31] are placed into SRR1[16:31].

3.9.8 General SPRs (SPRG0–SPRG3)

SPRG0–SPRG3, SPRs 272-275, are provided for general operating system use, such as fast-state saves and multiprocessor-implementation support. SPRG0–SPRG3 are shown below.

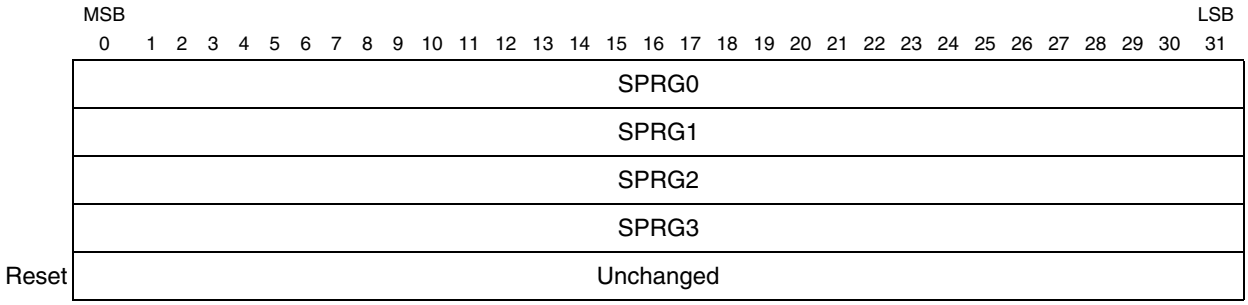


Figure 3-16. SPRG0–SPRG3 — General Special-Purpose Registers 0–3

Uses for SPRG0–SPRG3 are shown in Table 3-13.

Table 3-13. Uses of SPRG0–SPRG3

Register	Description
SPRG0	Software may load a unique physical address in this register to identify an area of memory reserved for use by the exception handler. This area must be unique for each processor in the system.
SPRG1	This register may be used as a scratch register by the exception handler to save the content of a GPR. That GPR then can be loaded from SPRG0 and used as a base register to save other GPRs to memory.
SPRG2	This register may be used by the operating system as needed.
SPRG3	This register may be used by the operating system as needed.

MPC561/MPC563, and RCPU access is terminated with a data error, causing a machine check state or exception.

The bus monitor timing bit in the system protection control register (SYPCR[BMT]) defines the bus monitor time-out period. The programmability of the time-out allows for variation in system peripheral response time. The timing mechanism is clocked by the external bus clock divided by eight. The maximum value is 2040 system clock cycles.

SYPCR[BME] enables or disables the bus monitor. But regardless of the state of this bit the bus monitor is always enabled when freeze is asserted in debug mode.

6.1.6 Decrementer (DEC)

The decrementer (DEC) is a 32-bit decrementing counter defined by the MPC561/MPC563 architecture to provide a decrementer interrupt. This binary counter is clocked by the same frequency as the time base (also defined by the MPC500 architecture). The operation of the time base and decrementer are therefore coherent. The DEC is clocked by the TMBCLK clock. The decrementer period is computed as follows:

$$T_{DEC} = \frac{2^{32}}{F_{TMBCLK}}$$

The state of the DEC is not affected by any resets and should be initialized by software. The DEC runs continuously after power-up once the time base is enabled by setting the TBE bit of the TBSCR (see Table 6-18) (unless the clock module is programmed to turn off the clock). The decrementer continues counting while reset is asserted.

Reading from the decrementer has no effect on the counter value. Writing to the decrementer replaces the value in the decrementer with the value in the GPR.

Whenever bit 0 (the MSB) of the decrementer changes from zero to one, a decrementer exception occurs. If software alters the decrementer such that the content of bit 0 is changed to a value of 1, a decrementer exception occurs.

A decrementer exception causes a decrementer interrupt request to be pending in the RCPU. When the decrementer exception is taken, the decrementer interrupt request is automatically cleared.

Table 6-6 illustrates some of the periods available for the decrementer, assuming a 4-MHz or 20-MHz crystal, and TBS = 0 which selects TMBCLK division to 4.

NOTE

Time base must be enabled to use the decrementer. See Section 6.2.2.4.4, "Time Base Control and Status Register (TBSCR)," for more information.

Table 6-6. Decrementer Time-Out Periods

Count Value	Time-Out @ 4 MHz	Time-Out @ 20 MHz
0	1.0 µs	0.2 µs
9	10 µs	2.0 µs

Table 8-11. PLPRCR Bit Descriptions (continued)

Bits	Name	Description
25	LOLRE	Loss of lock reset enable 0 Loss of lock does not cause HRESET assertion 1 Loss of lock causes HRESET assertion Note: if limp mode is enabled, use the COLIR feature instead of setting the LOLRE bit. See Section 8.11.3, “Change of Lock Interrupt Register (COLIR).”
26	—	Reserved
27:31	DIVF	The DIVF bits control the value of the pre-divider in the SPLL circuit. The DIVF bits can be read and written at any time. However, the DIVF field can be write-protected by setting the MF and pre-divider lock (MFPDL) bit in the SCCR. Changing the DIVF bits causes the SPLL to lose lock.

8.11.3 Change of Lock Interrupt Register (COLIR)

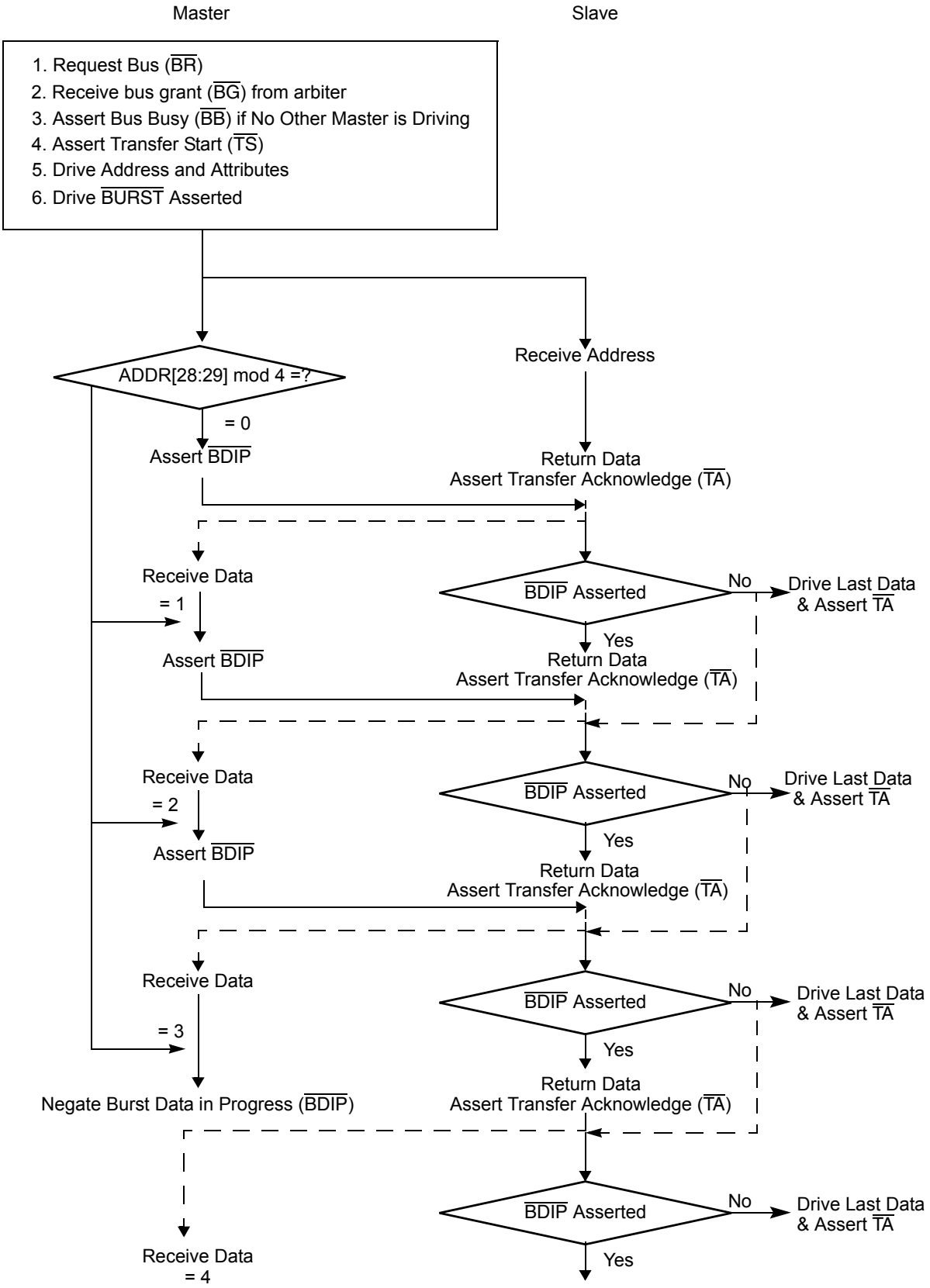
The COLIR is 16-bit read/write register. It controls the change of lock interrupt generation, and is used for reporting a loss of lock interrupt source. It contains the interrupt request level and the interrupt status bit. This register is readable and writable at any time. A status bit is cleared by writing a one (writing a zero does not affect a status bit’s value). The COLIR is mapped into the MPC561/MPC563 USIU register map.

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	COLIRQ								COLIS	—	COLIE	—				
SRESET	0000_0000_00										Unaffected					
Addr	0x2F C28C															

Figure 8-18. Change of Lock Interrupt Register (COLIR)

Table 8-12. COLIR Bit Descriptions

Bits	Name	Description
0:7	COLIRQ	Change of lock interrupt request level. These bits determine the interrupt priority level of the change of lock. To specify a certain level, the appropriate one of these bits should be set.
8	COLIS	If set (1), the bit indicates that a change in the PLL lock status was detected. The PLL was locked and lost lock, or the PLL was unlocked and got locked. The bit should be cleared by writing a one.
9	—	Reserved
10	COLIE	Change of Lock Interrupt enable. If COLIE bit is asserted, an interrupt will be generated when the COLIS bit is asserted. 0 Change of lock Interrupt disable 1 Change of lock Interrupt enable
11:15	—	Reserved


Master
Slave
1. Request Bus (BR)
2. Receive bus grant (BG) from arbiter
3. Assert Bus Busy (BB) if No Other Master is Driving
4. Assert Transfer Start (TS)
5. Drive Address and Attributes
6. Drive BURST Asserted
ADDR[28:29] mod 4 =?
= 0
Assert BDIP
Receive Address
Return Data
Assert Transfer Acknowledge (TA)
Receive Data
= 1
Assert BDIP
BDIP Asserted
No
Drive Last Data
& Assert TA
Yes
Return Data
Assert Transfer Acknowledge (TA)
Receive Data
= 2
Assert BDIP
BDIP Asserted
No
Drive Last Data
& Assert TA
Yes
Return Data
Assert Transfer Acknowledge (TA)
Receive Data
= 3
Negate Burst Data in Progress (BDIP)
BDIP Asserted
No
Drive Last Data
& Assert TA
Yes
Return Data
Assert Transfer Acknowledge (TA)
Receive Data
= 4
BDIP Asserted
No
Drive Last Data
& Assert TA
Yes

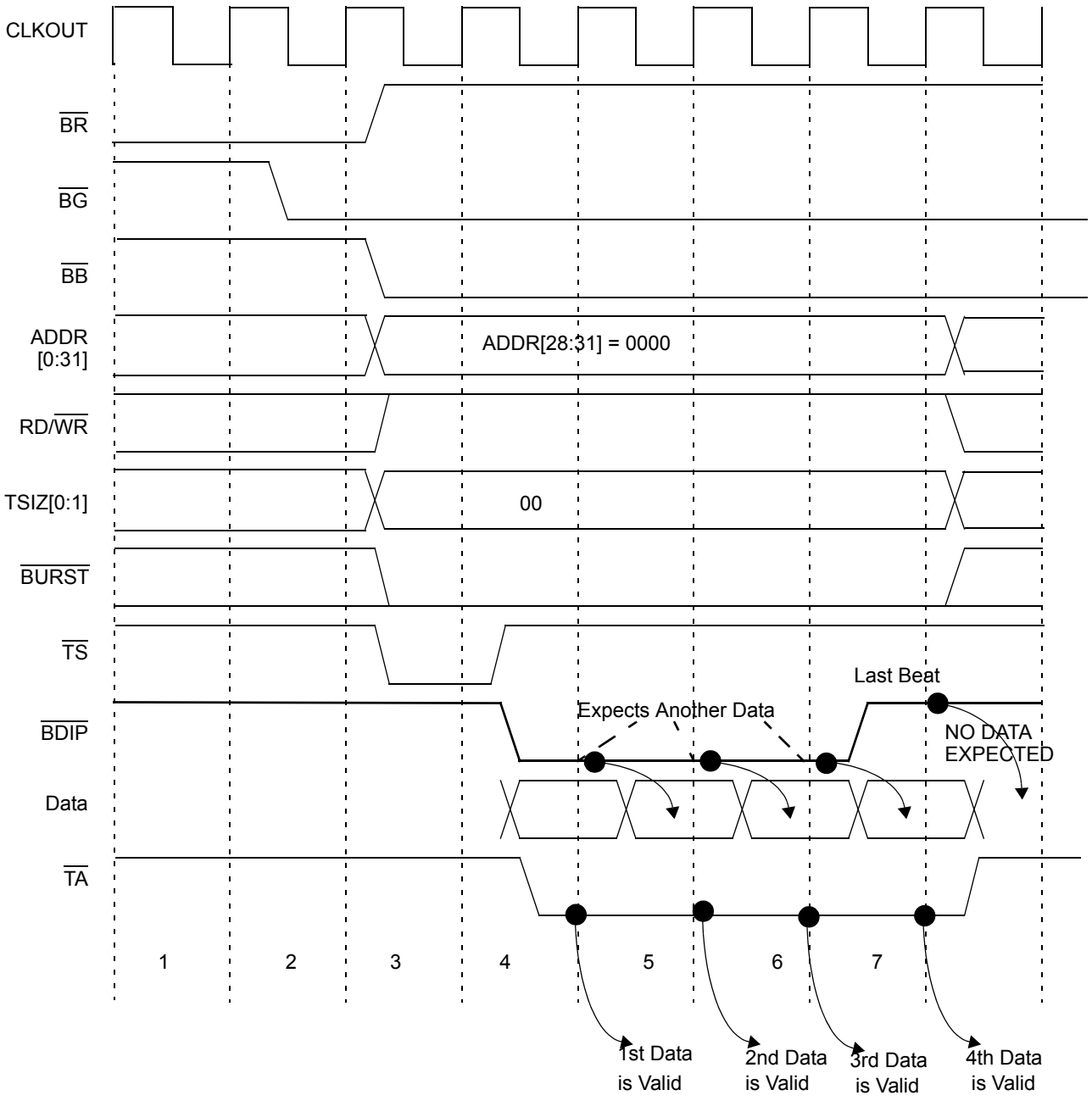


Figure 10-6. 4 Beat Burst Read with Short Setup Time (Zero Wait State)

NOTE

An extra clock cycle is required to enable short set-up time, resulting in a 4-1-1-1 cycle.

10.3 Chip-Select Timing

The general-purpose chip-select machine (GPCM) allows a glueless and flexible interface between the MPC561/MPC563 and external SRAM, EPROM, EEPROM, ROM peripherals. When an address and

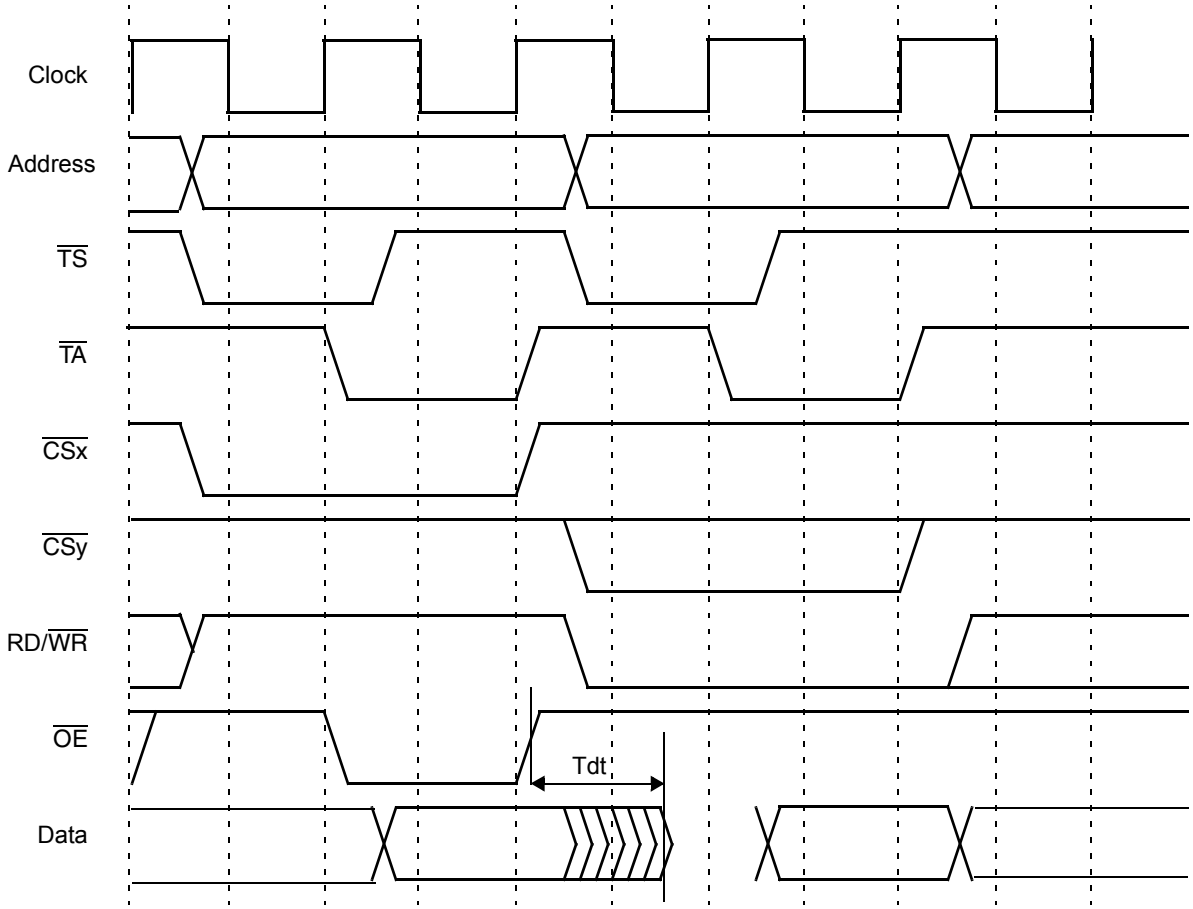


Figure 10-15. Consecutive Accesses (Write After Read, EHTR = 0)

Figure 10-16 shows a write access following a read access when EHTR = 1. An extra clock is inserted between the cycles. For a write cycle following a read, this is true regardless of whether both accesses are to the same region.

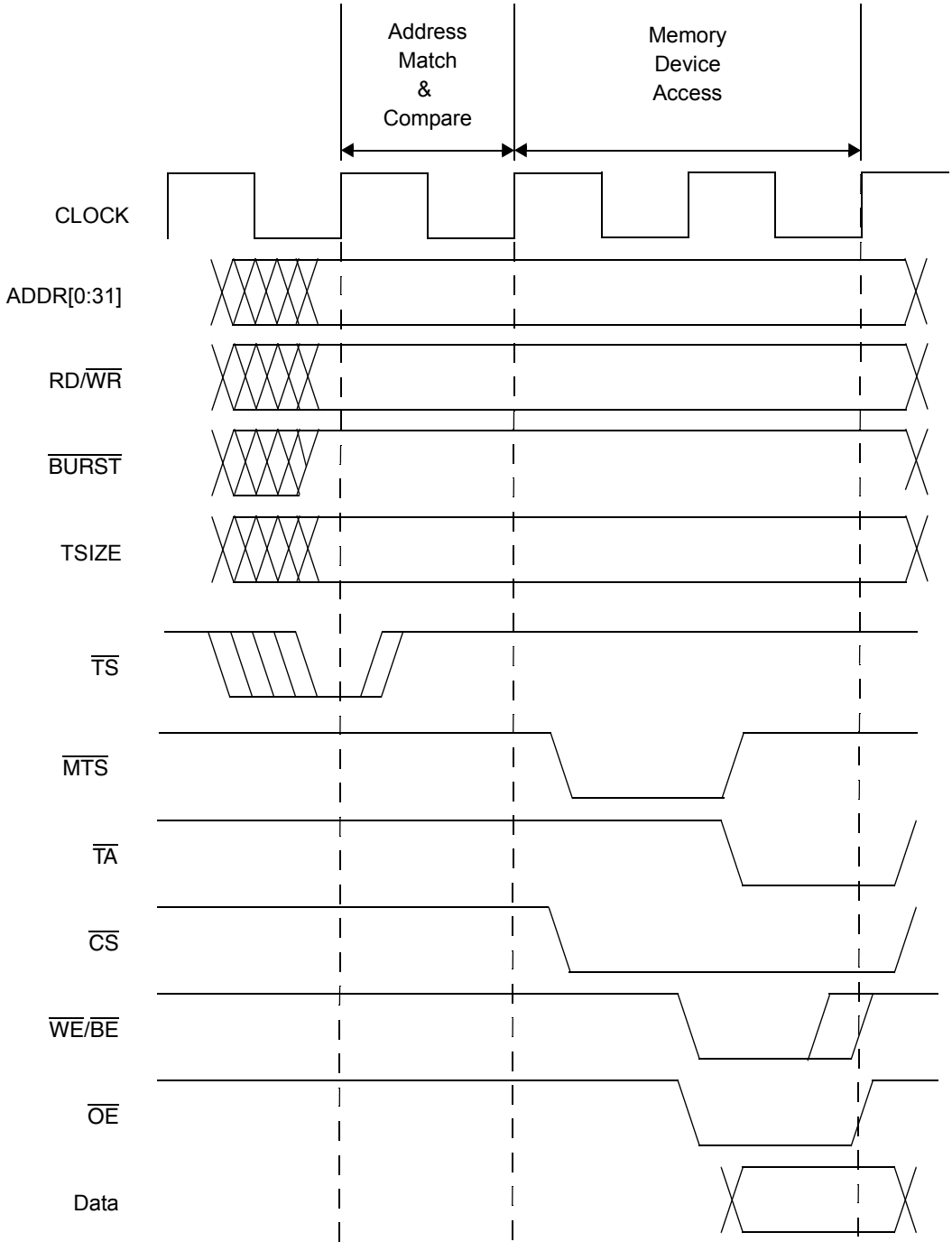


Figure 10-21. Synchronous External Master Basic Access (GPCM Controlled)

NOTE

Because the MPC561/MPC563 has only 24 address signals, the eight most significant internal address lines are driven as 0b0000_0000, and so compared in the memory controller's regions.

all of the status register fields contain read-only data. The four flag bits and the two trigger overrun bits are cleared by writing a zero to the bit after the bit was previously read as a one.

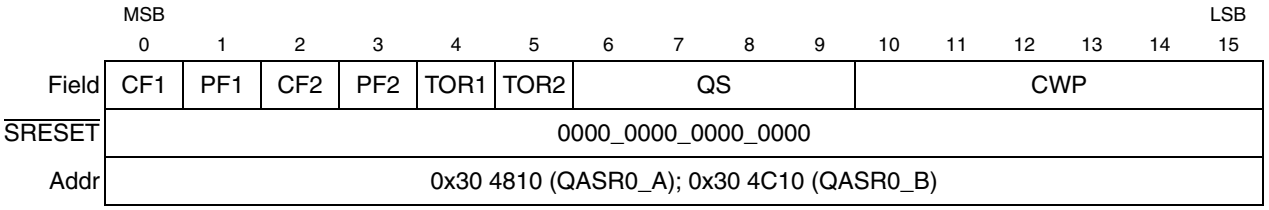


Figure 13-12. Status Register 0 (QASR0)

Table 13-14. QASR0 Bit Descriptions

Bits	Name	Description
0	CF1	Queue 1 Completion Flag. CF1 indicates that a queue 1 scan has been completed. The scan completion flag is set by the QADC64E when the input channel sample requested by the last CCW in queue 1 is converted, and the result is stored in the result table. The end-of-queue 1 is identified when execution is complete on the CCW in the location prior to that pointed to by BQ2, when the current CCW contains an end-of-queue code instead of a valid channel number, or when the currently completed CCW is in the last location of the CCW RAM. When CF1 is set and interrupts are enabled for that queue completion flag, the QADC64E asserts an interrupt request at the level specified by IRL1 in the interrupt register (QADCINT). The software reads the completion flag during an interrupt service routine to identify the interrupt request. The interrupt request is cleared when the software writes a zero to the completion flag bit, when the bit was previously read as a one. Once set, only software or reset can clear CF1. CF1 is maintained by the QADC64E regardless of whether the corresponding interrupt is enabled. The software polls for CF1 bit to see if it is set. This allows the software to recognize that the QADC64E is finished with a queue 1 scan. The software acknowledges that it has detected the completion flag being set by writing a zero to the completion flag after the bit was read as a one.

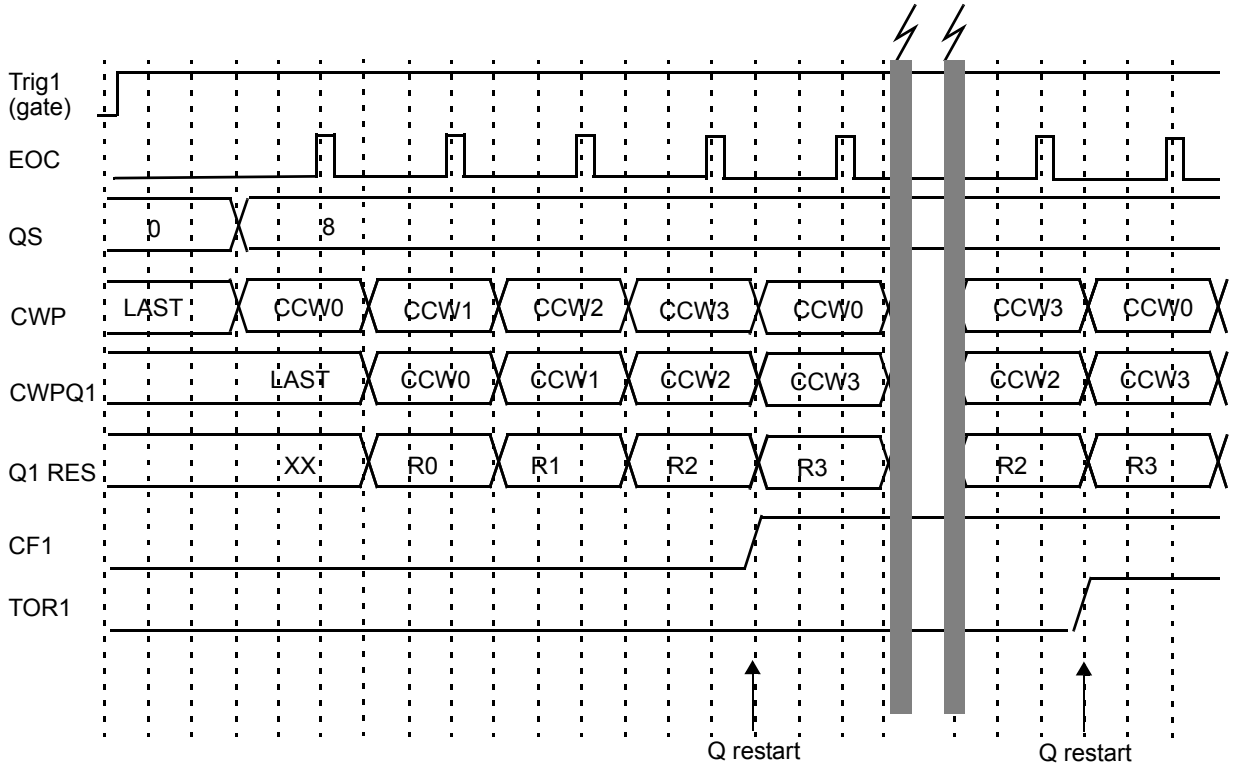


Figure 13-48. Gated Mode, Continuous Scan Timing

13.7 QADC64E Integration Requirements

The QADC64E requires accurate, noise-free input signals for proper operation. This section discusses the design of external circuitry to maximize QADC64E performance.

The QADC64E uses the external signals shown in Figure 13-1. There are 16 channel signals that can also be used as general-purpose digital input signals, 8 of which can be configured as either digital input or output signals.

13.7.1 Port Digital Input/Output Signals

The 16 port signals on the QADC64E module can be used as analog inputs. Port A signals can be configured as digital input or digital output signals and Port B signals can be used as 8-bit digital input signals.

Port A signals are referred to as PQA[7:0] when used as a bidirectional 8-bit digital input/output port. These eight signals may be used for general-purpose digital input signals or push-pull digital output signals. Port B signals are referred to as PQB[7:0] when used as digital input signals.

Port A and B signals are connected to a digital input synchronizer during reads and may be used as general purpose digital inputs when the applied voltages meet high voltage input (V_{IH}) and low voltage input (V_{IL}) requirements. Refer to Appendix F, “Electrical Characteristics,” for more information on voltage requirements.

14.6.5.2 Settling Time for the External Circuit

The values for R_{SRC}, R_F and C_F in the external circuitry determine the length of time required to charge C_F to the source voltage level (V_{SRC}). At time t = 0, V_{SRC} changes in Figure 14-50 while S1 is open, disconnecting the internal circuitry from the external circuitry. Assume that the initial voltage across C_F is zero. As C_F charges, the voltage across it is determined by the following equation, where t is the total charge time:

As t approaches infinity, V_{CF} will equal V_{SRC}. (This assumes no internal leakage.) With 10-bit resolution, 1/2 of a count is equal to 1/2048 full-scale value. Assuming worst case (V_{SRC} = full scale), Table 14-25 shows the required time for C_F to charge to within 1/2 of a count of the actual source voltage during 10-bit conversions. Table 14-25 is based on the RC network in Figure 14-50.

NOTE

The following times are completely independent of the A/D converter architecture (assuming the QADC64E is not affecting the charging).

Table 14-25. External Circuit Settling Time to 1/2 LSB (10-Bit Conversions)

Filter Capacitor (CF)	Source Resistance ($R_F + R_{SRC}$)			
	100 Ω	**1 kΩ**	**10 kΩ**	**100 kΩ**
1 µF	760 µs	7.6 ms	76 ms	760 ms
.1 µF	76 µs	760 µs	7.6 ms	76 ms
.01 µF	7.6 µs	76 µs	760 µs	7.6 ms
.001 µF	760 ns	7.6 µs	76 µs	760 µs
100 pF	76 ns	760 ns	7.6 µs	76 µs

The external circuit described in Table 14-25 is a low-pass filter. A user interested in measuring an AC component of the external signal must take the characteristics of this filter into account.

14.6.5.3 Error Resulting from Leakage

A series resistor limits the current to a signal, therefore input leakage acting through a large source impedance can degrade A/D accuracy. The maximum input leakage current is specified in Appendix F, "Electrical Characteristics." Input leakage is greater at higher operating temperatures. In the temperature range from 125° C to 50° C, the leakage current is halved for every 8 – 12° C reduction in temperature.

Assuming $V_{RH} - V_{RL}$ = 5.12 V, one count (assuming 10-bit resolution) corresponds to 5 mV of input voltage. A typical input leakage of 200 nA acting through 10 kΩ of external series resistance results in an error of 0.4 count (2.0 mV). If the source impedance is 100 kΩ and a typical leakage of 100 nA is present, an error of two counts (10 mV) is introduced.

In addition to internal junction leakage, external leakage (e.g., if external clamping diodes are used) and charge sharing effects with internal capacitors also contribute to the total leakage current. Table 14-26 illustrates the effect of different levels of total leakage on accuracy for different values of source impedance. The error is listed in terms of 10-bit counts.

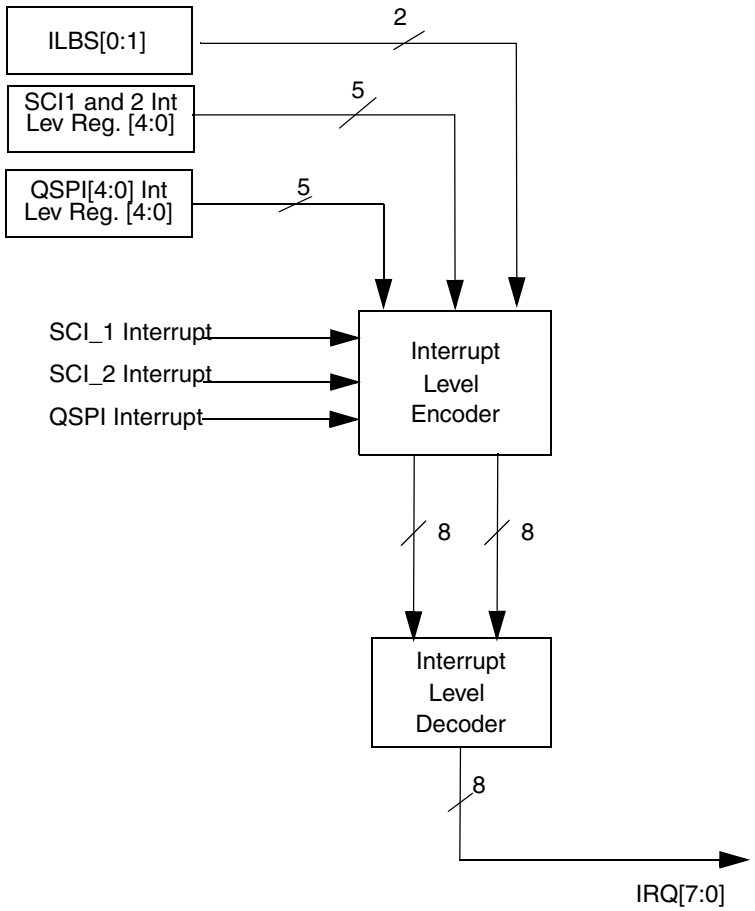


Figure 15-3. Interrupt Hardware Block Diagram

15.4.5 QSPI Interrupt Generation

15.4.6 QSMCM Configuration Register (QSMCMMCR)

The QSMCMMCR contains parameters for interfacing to the CPU and the intermodule bus. This register can be modified only when the CPU is in supervisor mode.

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	STOP	FRZ1	—						SUPV	—						
$\overline{\text{SRESET}}$	0	0	00_0000						1	000_0000						
Addr	0x30 5000															

Figure 15-4. QSMCM Configuration Register (QSMCMMCR)

15.8.2.1 QSCI1 Control Register (QSCI1CR)

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	QTPNT				QTHFI	QBHFI	QTHEI	QBHEI	—	QTE	QRE	QTWE	QTSZ			
SRESET	0000_0000_0000_0000															
Addr	0x30 5028															

Figure 15-31. QSCI1 Control Register (QSCI1CR)

Table 15-32. QSCI1CR Bit Descriptions

Bits	Name	Description
0:3	QTPNT	Queue transmit pointer. QTPNT is a 4-bit counter used to indicate the next data frame within the transmit queue to be loaded into the SC1DR. This feature allows for ease of testability. This field is writable in test mode only; otherwise it is read-only.
4	QTHFI	Receiver queue top-half full interrupt. When set, QTHFI enables an SCI1 interrupt whenever the QTHF flag in QSCI1SR is set. The interrupt is blocked by negating QTHFI. This bit refers to the queue locations SCRQ[0:7]. 0 QTHF interrupt inhibited 1 Queue top-half full (QTHF) interrupt enabled
5	QBHFI	Receiver queue bottom-half full interrupt. When set, QBHFI enables an SCI1 interrupt whenever the QBHF flag in QSCI1SR is set. The interrupt is blocked by negating QBHFI. This bit refers to the queue locations SCRQ[8:15]. 0 QBHF interrupt inhibited 1 Queue bottom-half full (QBHF) interrupt enabled
6	QTHEI	Transmitter queue top-half empty interrupt. When set, QTHEI enables an SCI1 interrupt whenever the QTHE flag in QSCI1SR is set. The interrupt is blocked by negating QTHEI. This bit refers to the queue locations SCTQ[0:7]. 0 QTHE interrupt inhibited 1 Queue top-half empty (QTHE) interrupt enabled
7	QBHEI	Transmitter queue bottom-half empty interrupt. When set, QBHEI enables an SCI1 interrupt whenever the QBHE flag in QSCI1SR is set. The interrupt is blocked by negating QBHEI. This bit refers to the queue locations SCTQ[8:15]. 0 QBHE interrupt inhibited 1 Queue bottom-half empty (QBHE) interrupt enabled
8	—	Reserved
9	QTE	Queue transmit enable. When set, the transmit queue is enabled and the TDRE bit should be ignored by software. The TC bit is redefined to indicate when the entire queue is finished transmitting. When clear, the SCI1 functions as described in the previous sections and the bits related to the queue (Section 5.5 and its subsections) should be ignored by software with the exception of QTE. 0 Transmit queue is disabled 1 Transmit queue is enabled

but the data register (SC1DR) is still full. The data in the shifter that generated the OR assertion is overwritten by the next received data frame, but the data in the SC1DR is not lost.

Table 23-8. Load/Store Watchpoints Programming Options

Name	Description	Instruction Events Programming Options	L-address Events Programming Options	L-data Events Programming Options
LWP0	First Load/store watchpoint	IWP0, IWP1, IWP2, IWP3, ignore instruction events	Comparator E Comparator F Comparators (E&F) Comparators (E | F) ignore L-addr events	Comparator G Comparator H Comparators (G&H) Comparators (G | H) ignore L-data events
LWP1	Second Load/store watchpoint	IWP0, IWP1, IWP2, IWP3, ignore instruction events	Comparator E Comparator F Comparators (E&F) Comparators (E | F) ignore I-addr events	Comparator G Comparator H Comparators (G&H) Comparators (G | H) ignore L-data events

Note that when programming the load/store watchpoints to ignore L-addr events and L-data events, it does not reduce the load/store watchpoints detection logic to be instruction watchpoint detection logic since the instruction must be a load/store instruction for the load/store watchpoint event to trigger.

- L-bus data phase error.
- U-bus address phase error (for a L-bus to U-bus cycle).
- U-bus data phase error (for a L-bus to U-bus cycle).

L-bus data error conditions are signalled along with the transfer acknowledge for the access. L-bus data error conditions may occur because of privilege violations, access to protected memory, etc. In such cases, for a read access, the ERR bit of the UDI is set, and the DV bit in the UDI is reset at the termination of the access. For a write access, an error public message (TCODE = 8) is transmitted (error code 0b00011).

24.10.6 Exception Sequences

The following cases are defined for sequences of the read/write protocol that differ from those described in the above sections:

1. If the SC bit is set to start READI read/write accesses, without valid values in the RWAD, then an L-bus address error may occur, which is handled as described above.
2. If a block access is in progress with all the cycles not yet completed, and the RWA is written to again, (with or without modifications), then the block access is terminated at the boundary of the nearest completed access. The resulting data is discarded and not written to the UDI. If a new access has been programmed in the RWA register, then that access will start once the controller has recovered.
3. When a block access is in progress with all the cycles not yet completed, writing the SC bit to 0 in RWA register will terminate the block access and device will send out device ready for upload/download message.
4. If a any type (single/block) of access is in progress with the cycles not yet completed, and system reset occurs, the device will send out an error message. The access will be terminated and the SC bit will be reset. Refer to Table 24-20.
5. If any type of (single/block) of access is requested while system is in reset, the device will send out an error message. The access will not be started and the SC bit will be reset.

24.10.7 Secure Mode

For details refer to Section 24.2.2, “Security.”

24.10.8 Error Messages

24.10.8.1 Read/Write Access Error

An error message is sent out when an L-bus access error or data error on a write access occurs. The error code within the error message indicates that an L-bus address or L-bus data error occurred. For other error handling, see Section 24.10.5, “Error Handling.” For a list of error codes, refer to Table 24-20.

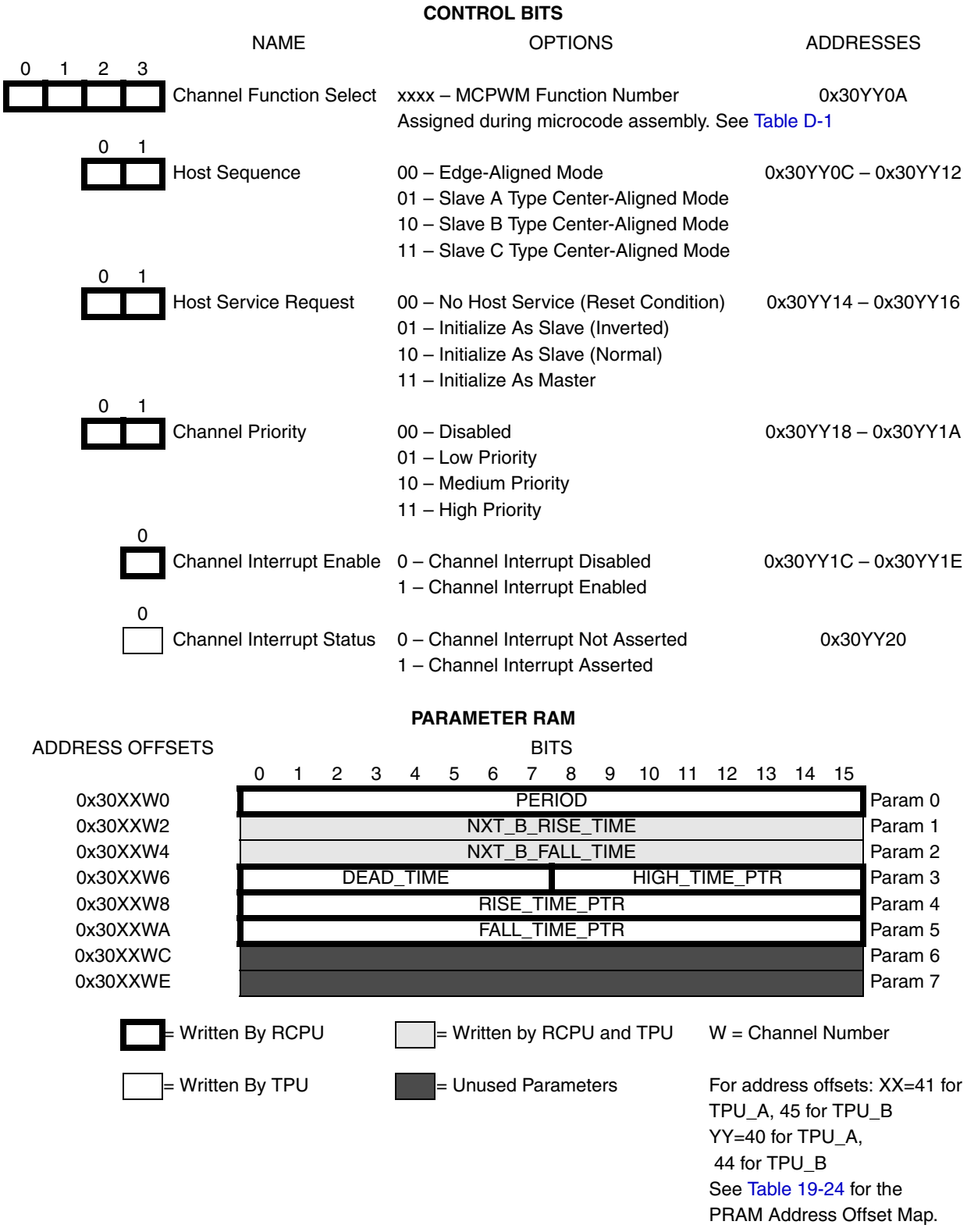
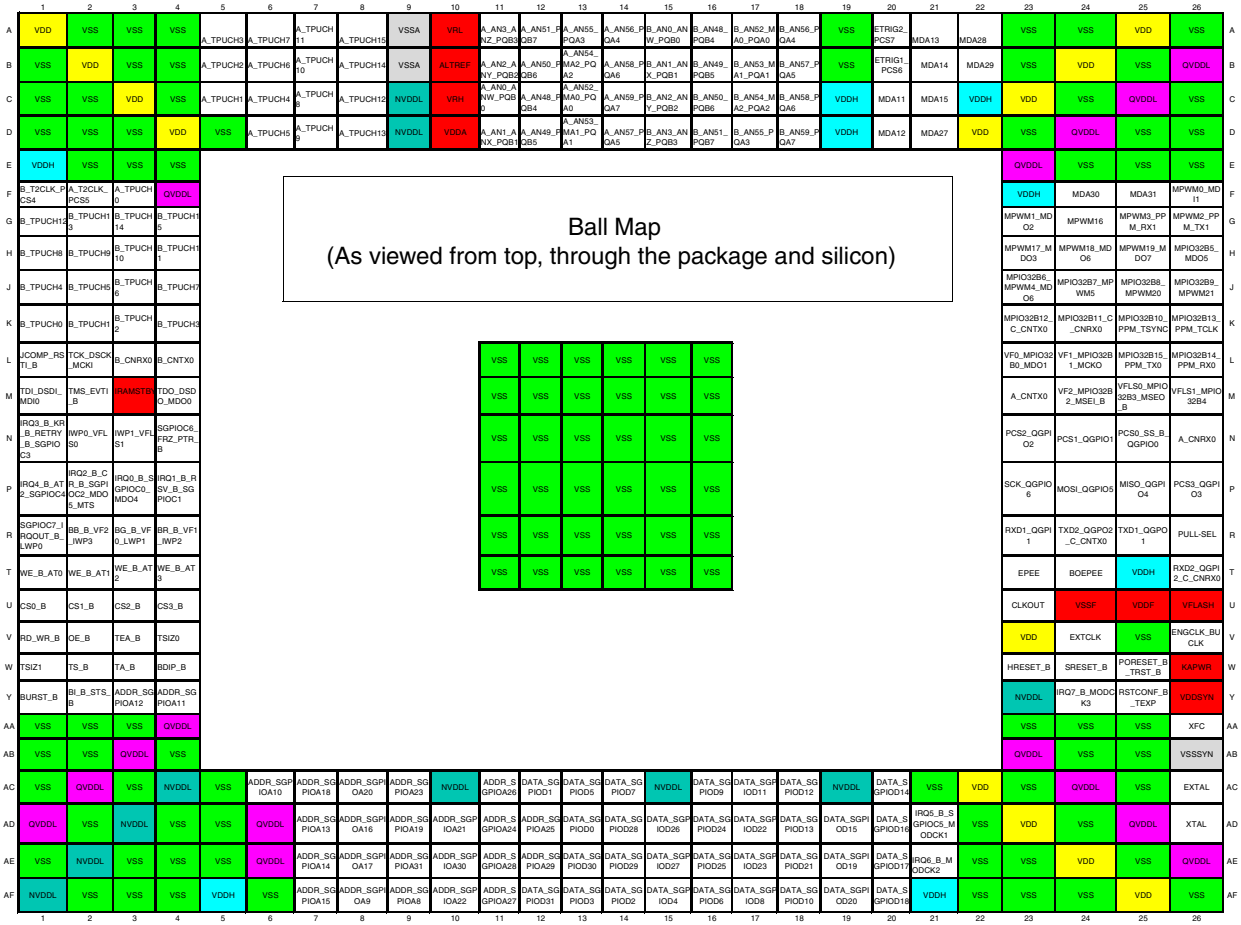


Figure D-16. MCPWM Parameters — Slave Ch A Inverted Center-Aligned Mode

G.23.1.1 MPC561/MPC563 Ball Map

The ball diagram of the MPC561/MPC563 is shown in Figure G-65.



NOTE: The Flash balls are only available on the MPC563 and MPC564. These are no connects on the MPC561 and MPC562. Flash supplies and inputs are located on the following balls: T23, T24, U24, U25. U26.

Figure G-65. MPC561/MPC563 Ball Map