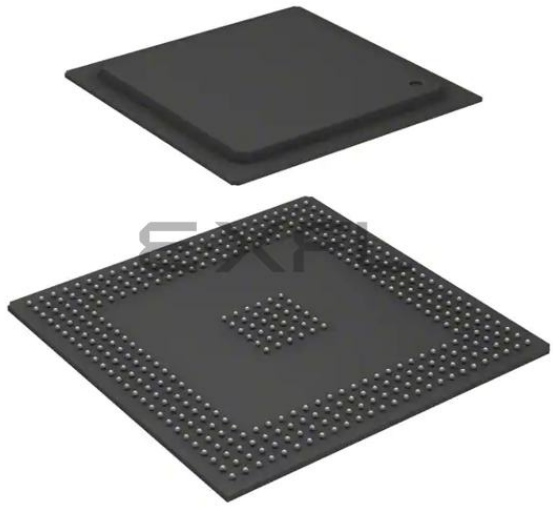

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Details	
Product Status	Obsolete
Core Processor	PowerPC
Core Size	32-Bit Single-Core
Speed	56MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	64
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 2.7V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	388-BBGA
Supplier Device Package	388-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc562mzp56r2

provide maximum system safeguards against hardware and software faults. This chapter provides a detailed explanation of this functionality.

- Chapter 7, “Reset.” This section describes the MPC561/MPC563 reset sources, operation, control, and status.
- Chapter 8, “Clocks and Power Control,” describes the main timing and power control reference for the MPC561/MPC563.
- Chapter 9, “External Bus Interface,” describes the functionality of the MPC561/MPC563 external bus.
- Chapter 10, “Memory Controller,” generates interface signals to support a glueless interface to external memory and peripheral devices.
- Chapter 11, “L-Bus to U-Bus Interface (L2U),” describes the interface between the load/store bus (L-bus) and the unified bus (U-bus). The L2U module includes the Data Memory Protection Unit (DMPU), which provides protection for data memory accesses.
- Chapter 12, “U-Bus to IMB3 Bus Interface (UIMB).” The U-bus to IMB3 bus interface (UIMB) structure is used to connect the CPU internal unified bus (U-bus) to the intermodule bus 3 (IMB3). It controls bus communication between the U-bus and the IMB3.
- Chapter 13, “QADC64E Legacy Mode Operation.” The two queued analog-to-digital converter (QADC) modules on MPC561/MPC563 devices are 10-bit, unipolar, successive approximation converters. The modules can be configured to operate in one of two modes, legacy mode (MPC555 compatible) and enhanced mode. This chapter describes how the modules operate in legacy mode, which is the default mode of operation.
- Chapter 14, “QADC64E Enhanced Mode Operation.” The two queued analog-to-digital converter (QADC) modules on the MPC561/MPC563 devices are 10-bit, unipolar, successive approximation converters. The modules can be configured to operate in one of two modes, legacy mode (for MPC555 compatibility) and enhanced mode. This chapter describes how the module operates in enhanced mode.
- Chapter 15, “Queued Serial Multi-Channel Module.” The MPC561/MPC563 contains one queued serial multi-channel module (QSMCM) which provides three serial communication interfaces: the queued serial peripheral interface (QSPI) and two serial communications interfaces (SCI/UART). This chapter describes the functionality of each.
- Chapter 16, “CAN 2.0B Controller Module,” describes the three CAN 2.0B controller modules (TouCAN) implemented on the MPC561/MPC563. Each TouCAN is a communication controller that implements the Controller Area Network (CAN) protocol, an asynchronous communications protocol used in automotive and industrial control systems. It is a high speed (one Mbit/sec), short distance, priority based protocol that can run over a variety of mediums.
- Chapter 17, “Modular Input/Output Subsystem (MIOS14).” The modular I/O system (MIOS) consists of a library of flexible I/O and timer functions including I/O port, counters, input capture, output compare, pulse and period measurement, and PWM. Because the MIOS14 is composed of submodules, it is easily configurable for different kinds of applications.
- Chapter 18, “Peripheral Pin Multiplexing (PPM) Module.” The PPM functions as a parallel-to-serial communications module that reduces the number of signals required to connect

2.2 Signal Summary

Table 2-1 describes individual MPC561/MPC563 signals, grouped by functional module.

Table 2-1. MPC561/MPC563 Signal Descriptions

Signal Name	No. of Signals	Type	Function after Reset[1]	Description
Bus Interface				
ADDR[8:31] / SGPIOA[8:31]	24	I/O	Controlled by RCW[SC]. See Table 6-10.	Address Bus [8:31]. Specifies the physical address of the bus transaction. The address is driven onto the bus and kept valid until a transfer acknowledge is received from the slave. ADDR8 is the MSB for this bus.
		I/O		Port SGPIOA[8:31]. Allows the signals to be used as general-purpose inputs/outputs.
DATA[0:31] / SGPIOD[0:31]	32	I/O	Controlled by RCW[SC]. See Table 6-10.	Data Bus [0:31]. Provides the general-purpose data path between the MPC561/MPC563 and all other devices. Although the data path is a maximum of 32 bits wide, it can be sized to support 8-, 16-, or 32-bit transfers. DATA0 is the MSB of the data bus.
		I/O		Port SGPIOD[0:31]. Allows the signals to be used as general-purpose inputs/outputs.
TSIZ[0:1]	2	I/O	TSIZ[0:1]	Transfer Size [0:1]. Indicates the size of the requested data transfer in the current bus cycle.
RD/$\overline{WR}$	1	I/O	RD/$\overline{WR}$	Read/Write. Indicates the direction of the data transfer for a transaction. A logic one indicates a read from a slave device; a logic zero indicates a write to a slave device.
$\overline{BURST}$	1	I/O	$\overline{BURST}$	Burst Indicator. Driven by the bus master to indicate that the currently initiated transaction is a burst.
$\overline{BDIP}$	1	I/O	$\overline{BDIP}$	Burst Data In Progress. Indicates to the slave that there is a data beat following the current data beat.
$\overline{TS}$	1	I/O	$\overline{TS}$	Transfer Start. Indicates the start of a bus cycle that transfers data to/from a slave device. This signal is driven by the master only when it has gained ownership of the bus. Every master should negate this signal before relinquishing the bus. This is an active-low signal and needs an external pull-up resistor to ensure proper operation and meet signal timing specifications.
$\overline{TA}$	1	I/O	$\overline{TA}$	Transfer Acknowledge. This line indicates that the slave device addressed in the current transaction has accepted the data transferred by the master (write) or has driven the data bus with valid data (read). The slave device negates the $\overline{TA}$ signal after the end of the transaction. The slave device will then immediately three-state the $\overline{TA}$ signal to prevent contention on the line in case a new transfer that addresses another slave device(s) is initiated. This signal is an active-low signal and needs an external pull-up resistor to ensure proper operation and conform to signal timing specifications.

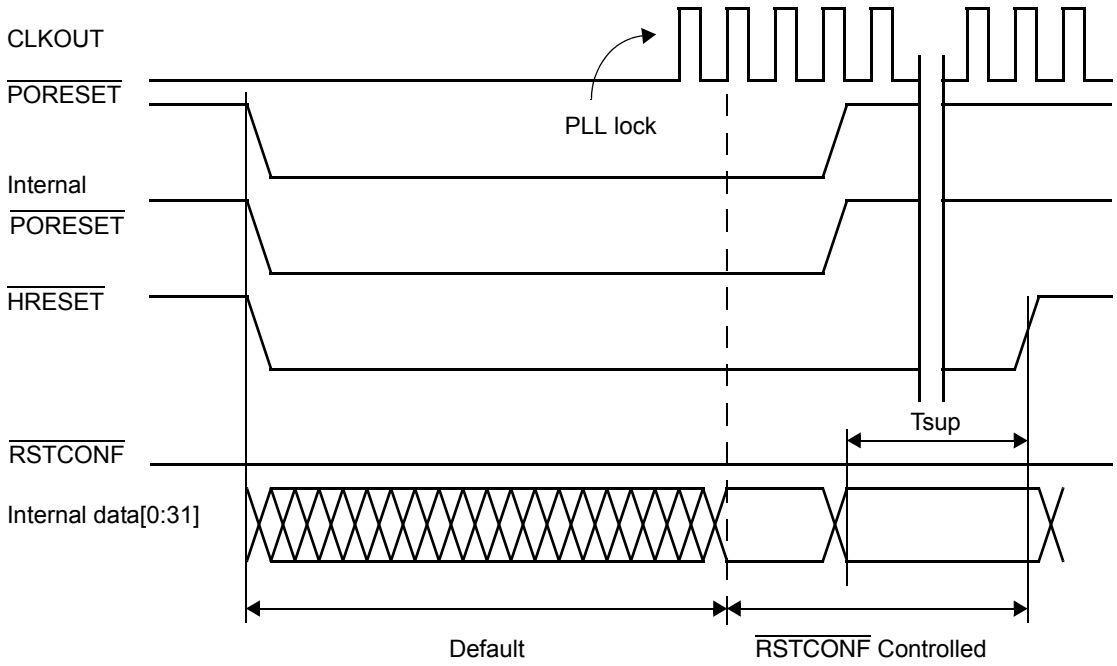

Figure 7-5. Reset Configuration Timing for "Long" PORESET Assertion, Limp Mode Disabled

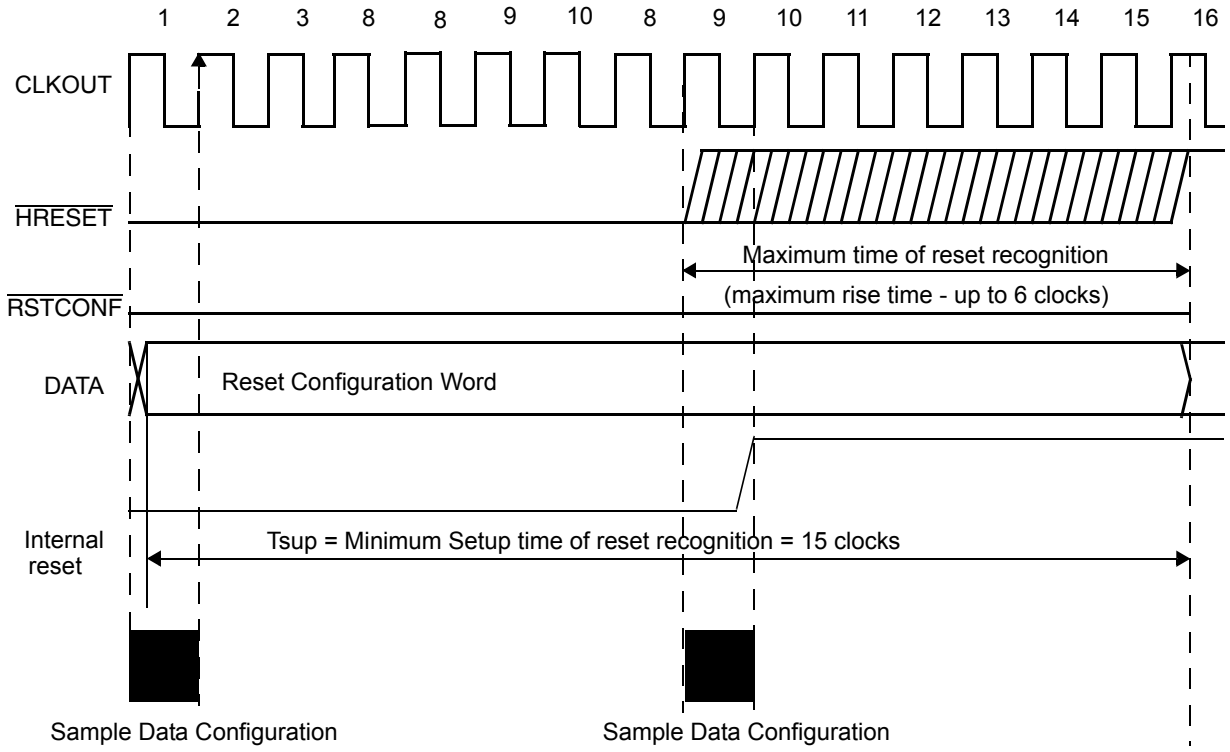

Figure 7-6. Reset Configuration Sampling Timing Requirements

Table 7-5. RCW Bit Descriptions (continued)

Bits	Name	Description
24:25	OERC	Other Exceptions Relocation Control — These bits effect only if ETRE was enabled. See Table 4-2. Relocation offset: 00 Offset 0 01 Offset 64 Kbytes 10 Offset 512 Kbytes 11 Offset to 0x003F E000
26:27	—	Reserved
28:30	ISB	Internal Space Base Select — This field defines the initial value of the ISB field in the IMMR register. A detailed description is in Table 6-12. The default state is that the internal memory map is mapped to start at address 0x0000_0000. This bit must not be high in the reset configuration word.
31	DME	Dual Mapping Enable — This bit determines whether Dual mapping of the internal Flash is enabled. For a detailed description refer to Table 10-11. The default state is that dual mapping is disabled. 0 Dual mapping disabled 1 Dual mapping enabled

1 Bit 15 always comes from the internal Flash Reset Configuration Word (MPC563 only).

2 This bit should not be set on the MPC561/MPC562.

3 This bit is $\overline{\text{HC}}$ if read from the internal Flash Reset Configuration Word. See Section 21.2.3.1, “Reset Configuration Word (UC3FCFIG).”

4 Available only on the MPC562/MPC564, software should write "0" to this bit for MPC561/MPC563.

7.5.3 Soft Reset Configuration

When a soft reset event occurs, the MPC561/MPC563 reconfigures the development port. Refer to Chapter 23, “Development Support,” for details.

the input source to the SPLL (main system oscillator or EXTCLK). MODCK1, MODCK2, and MODCK3 together determine the multiplication factor at reset and the functionality of limp mode.

If the configuration of PITRTCLK and TMBCLK and the SPLL multiplication factor is to remain unchanged in power-down low-power mode, the MODCK signals should not be sampled at wake-up from this mode. In this case the $\overline{\text{PORESET}}$ pin should remain negated and $\overline{\text{HRESET}}$ should be asserted during the power supply wake-up stage.

When MODCK1 is cleared, the output of the main oscillator is selected as the input to the SPLL. When MODCK1 is asserted, the external clock input (EXTCLK pin) is selected as the input to the SPLL. In all cases, the system clock frequency ($freq_{gclk2}$) can be reduced by the DFNH[0:2] bits in the SCCR. Note that $freq_{gclk2(max)}$ occurs when the DFNH bits are cleared.

The TBS bit in the SCCR selects the time base clock to be either the SPLL input clock or GCLK2. When the backup clock is functioning as the system clock, the backup clock is automatically selected as the time base clock source.

The PITRTCLK frequency and source are specified by the RTDIV and RTSEL bits in the SCCR. When the backup clock is functioning as the system clock, the backup clock is automatically selected as the time base clock source.

When the $\overline{\text{PORESET}}$ pin is negated (driven to a high value), the MODCK1, MODCK2, and MODCK3 values are not affected. They remain the same as they were defined during the most recent power-on reset.

Table 8-1 shows the clock configuration modes during power-on reset ($\overline{\text{PORESET}}$ asserted).

NOTE

The MODCK[1:3] are shared functions with IRQ[5:7]. If $\overline{\text{IRQ}}$[5:7] are used as interrupts, the interrupt source should be removed during $\overline{\text{PORESET}}$ to insure the MODCK pins are in the correct state on the rising edge of $\overline{\text{PORESET}}$.

Table 8-1. Reset Clocks Source Configuration

MODCK[1:3][1]	Default Values after $\overline{\text{PORESET}}$						SPLL Options
	LME	RTSEL	RTDIV	MF + 1	PITCLK Division	TMBCLK Division	
000	0	0	0	1	4	4	Used for testing purposes.
001	0	0	1	1	256	16	Normal operation, PLL enabled. Main timing reference is crystal osc (20 MHz). Limp mode disabled.
010	1	0	1	5	256	4	Normal operation, PLL enabled. Main timing reference is crystal osc (4 MHz). Limp mode enabled.
011	1	0	1	1	256	16	Normal operation, PLL enabled. Main timing reference is crystal osc (20 MHz). Limp mode enabled.

then controls the length of the cycle with the signal(s) used to terminate the cycle. A strobe signal for the address lines indicates the validity of the address.

The MPC561/MPC563 bus is synchronous with a synchronous support. The bus and control input signals must be timed to setup and hold times relative to the rising edge of the clock. Bus cycles can be completed in two clock cycles.

For all inputs, the MPC561/MPC563 latches the level of the input during a sample window around the rising edge of the clock signal. This window is illustrated in Figure 9-1, where t_{su} and t_{ho} are the input setup and hold times, respectively. To ensure that an input signal is recognized on a specific rising edge of the clock, that input must be stable during the sample window. If an input makes a transition during the window time period, the level recognized by the MPC561/MPC563 is not predictable; however, the MPC561/MPC563 always resolves the latched level to either a logic high or low before using it. In addition to meeting input setup and hold times for deterministic operation, all input signals must obey the protocols described in this section.

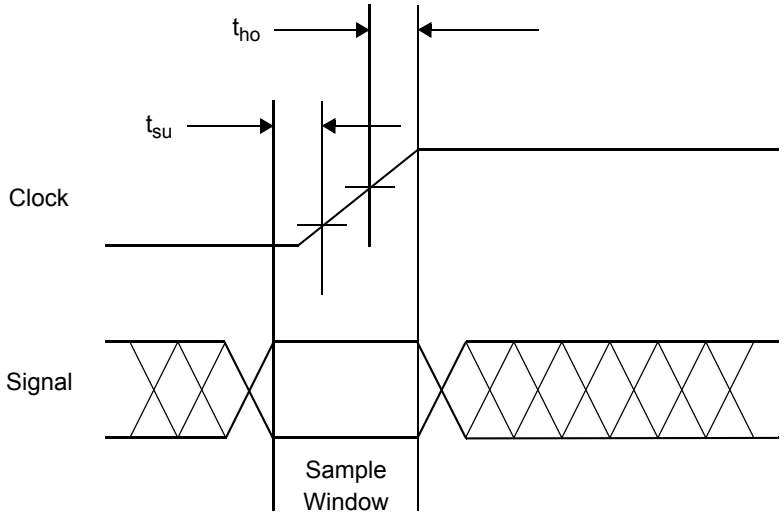

Figure 9-1. Input Sample Window

9.3 Bus Control Signals

The MPC561/MPC563 initiates a bus cycle by driving the address, size, address type, cycle type, and read/write outputs. At the beginning of a bus cycle, TSIZ[0:1] are driven with the address type signals. TSIZ0 and TSIZ1 indicate the number of bytes remaining to be transferred during an operand cycle (consisting of one or more bus cycles). These signals are valid at the rising edge of the clock in which the transfer start ($\overline{TS}$) signal is asserted.

The read/write (RD/$\overline{WR}$) signal determines the direction of the transfer during a bus cycle. Driven at the beginning of a bus cycle, RD/$\overline{WR}$ is valid at the rising edge of the clock in which $\overline{TS}$ is asserted. The logic level of RD/$\overline{WR}$ only changes when a write cycle is preceded by a read cycle or vice versa. The signal may remain low for consecutive write cycles.

Table 14-13. QACR2 Bit Descriptions

Bits	Name	Description
0	CIE2	Queue 2 Completion Software Interrupt Enable. CIE2 enables an interrupt upon completion of queue 2. The interrupt request is initiated when the conversion is complete for the CCW in queue 2. 0 Disable the queue completion interrupt associated with queue 2 1 Enable an interrupt after the conversion of the sample requested by the last CCW in queue 2
1	PIE2	Queue 2 Pause Software Interrupt Enable. PIE2 enables an interrupt when queue 2 enters the pause state. The interrupt request is initiated when conversion is complete for a CCW that has the pause bit set. 0 Disable the pause interrupt associated with queue 2 1 Enable an interrupt after the conversion of the sample requested by a CCW in queue 2 which has the pause bit set
2	SSE2	Queue 2 Single-Scan Enable Bit. SSE2 enables a single-scan of queue 2 to start after a trigger event occurs. The SSE2 bit may be set to a one during the same write cycle when the MQ2 bits are set for one of the single-scan queue operating modes. The single-scan enable bit can be written as a one or a zero, but is always read as a zero. The SSE2 bit enables a trigger event to initiate queue execution for any single-scan operation on queue 2. The QADC64E clears the SSE2 bit when the single-scan is complete. Refer to Table 14-14 for more information. 0 Trigger events are not accepted for single-scan modes 1 Accept a trigger event to start queue 2 in a single-scan mode
3:7	MQ2	Queue 2 Operating Mode. The MQ2 field selects the queue operating mode for queue 2. Refer to Table 14-14 for more information.
8	RESUME	0 After suspension, begin executing with the first CCW in queue 2 or the current sub-queue 1 After suspension, begin executing with the aborted CCW in queue 2

Another pause and end-of-queue boundary condition occurs when the pause and an end-of-queue condition occur in the same CCW. Both the pause and end-of-queue conditions are recognized simultaneously. The end-of-queue condition has precedence so a conversion is not performed for the CCW and the pause flag is not set. The QADC64E sets the completion flag and the queue status becomes idle. Examples of this situation are:

- The pause bit is set in CCW10 and EOQ is programmed into CCW10
- During queue 1 operation, the pause bit set in CCW32, which is also BQ2

14.4.4 Scan Modes

The QADC64E queuing mechanism allows the application to utilize different requirements for automatically scanning input channels.

In single-scan mode, a single pass through a sequence of conversions defined by a queue is performed. In continuous-scan mode, multiple passes through a sequence of conversions defined by a queue are executed. The possible modes are:

- Disabled and reserved mode
- Single-scan modes
  - Software initiated single-scan mode
  - External trigger single-scan mode
  - External gated single-scan mode
  - Periodic/Interval timer single-scan mode
- Continuous-scan modes
  - Software initiated continuous-scan mode
  - External trigger continuous-scan mode
  - External gated continuous-scan mode
  - Periodic/Interval timer continuous-scan mode

14.4.4.1 Disabled Mode

When the disabled mode is selected, the queue is not active. Trigger events cannot initiate queue execution. When both queue 1 and queue 2 are disabled, wait states are not encountered for IMB3 accesses of the RAM. When both queues are disabled, it is safe to change the QCLK prescaler values.

14.4.4.2 Reserved Mode

Reserved mode allows for future mode definitions. When the reserved mode is selected, the queue is not active. It functions the same as disabled mode.

WARNING

Do not use a reserved mode. Unspecified operations may result.

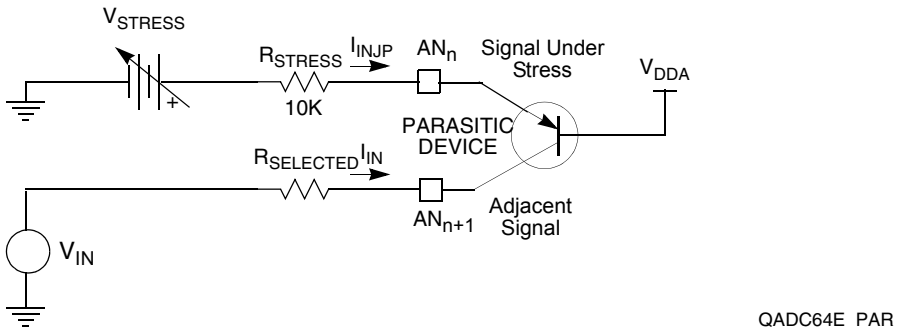

Figure 14-53. Input Signal Subjected to Positive Stress

The current into the signal (I_{INJN} or I_{INJP}) under negative or positive stress is determined by the following equations:

$$I_{INJN} = \frac{-(V_{STRESS} - V_{BE})}{R_{STRESS}} \qquad \textit{Eqn. 14-1}$$

$$I_{INJP} = \frac{V_{STRESS} - V_{EB} - V_{DDA}}{R_{STRESS}} \qquad \textit{Eqn. 14-2}$$

where:

V_{STRESS} = Adjustable voltage source

V_{EB} = Parasitic PNP emitter/base voltage
(refer to $V_{NEGCLAMP}$ in Appendix F, “Electrical Characteristics”)

V_{BE} = Parasitic NPN base/emitter voltage
(refer to $V_{NEGCLAMP}$ in Appendix F, “Electrical Characteristics”))

R_{STRESS} = Source impedance
(10-kΩ resistor in Figure 14-52 and Figure 14-53 on stressed channel)

$R_{SELECTED}$ = Source impedance on channel selected for conversion

The current into (I_{IN}) the neighboring signal is determined by the K_N (current coupling ratio) of the parasitic bipolar transistor ($K_N << 1$). The I_{IN} can be expressed by the following equation:

$$I_{IN} = - K_N * I_{INJ}$$

where I_{INJ} is either I_{INJN} or I_{INJP}.

A method for minimizing the impact of stress conditions on the QADC64E is to strategically allocate QADC64E inputs so that the lower accuracy inputs are adjacent to the inputs most likely to see stress conditions.

Also, suitable source impedances should be selected to meet design goals and minimize the effect of stress conditions.

The SPIFIE bit in SPCR2 enables the QSPI to generate an interrupt request upon assertion of the SPIF status flag. Because it is buffered, the value written to SPIFIE applies only upon completion of the queue (the transfer of the entry indicated by ENDPQ). Thus, if a single sequence of queue entries is to be transferred (i.e., no WRAP), then SPIFIE should be set to the desired state before the first transfer.

If a sub-queue is to be used, the same CPU write that causes a branch to the sub-queue may enable or disable the SPIF interrupt for the sub-queue. The primary queue retains its own selected interrupt mode, either enabled or disabled.

The SPIF interrupt must be cleared by clearing SPIF. Subsequent interrupts may then be prevented by clearing SPIFIE. Clearing SPIFIE does not immediately clear an interrupt already caused by SPIF.

15.6.4.3 QSPI Flow

The QSPI operates in either master or slave mode. Master mode is used when the MCU initiates data transfers. Slave mode is used when an external device initiates transfers. Switching between these modes is controlled by MSTR in SPCR0. Before entering either mode, appropriate QSMCM and QSPI registers must be initialized properly.

In master mode, the QSPI executes a queue of commands defined by control bits in each command RAM queue entry. Chip-select pins are activated, data is transmitted from the transmit RAM and received by the receive RAM.

In slave mode, operation proceeds in response to $\overline{SS}$ pin assertion by an external SPI bus master. Operation is similar to master mode, but no peripheral chip selects are generated, and the number of bits transferred is controlled in a different manner. When the QSPI is selected, it automatically executes the next queue transfer to exchange data with the external device correctly.

Although the QSPI inherently supports multi-master operation, no special arbitration mechanism is provided. A mode fault flag (MODF) indicates a request for SPI master arbitration. System software must provide arbitration. Note that unlike previous SPI systems, MSTR is not cleared by a mode fault being set nor are the QSPI pin output drivers disabled. The QSPI and associated output drivers must be disabled by clearing SPE in SPCR1.

Figure 15-18 shows QSPI initialization. Figure 15-19 through Figure 15-23 show QSPI master and slave operation. The CPU must initialize the QSMCM global and pin registers and the QSPI control registers before enabling the QSPI for either mode of operation. The command queue must be written before the QSPI is enabled for master mode operation. Any data to be transmitted should be written into transmit RAM before the QSPI is enabled. During wraparound operation, data for subsequent transmissions can be written at any time.

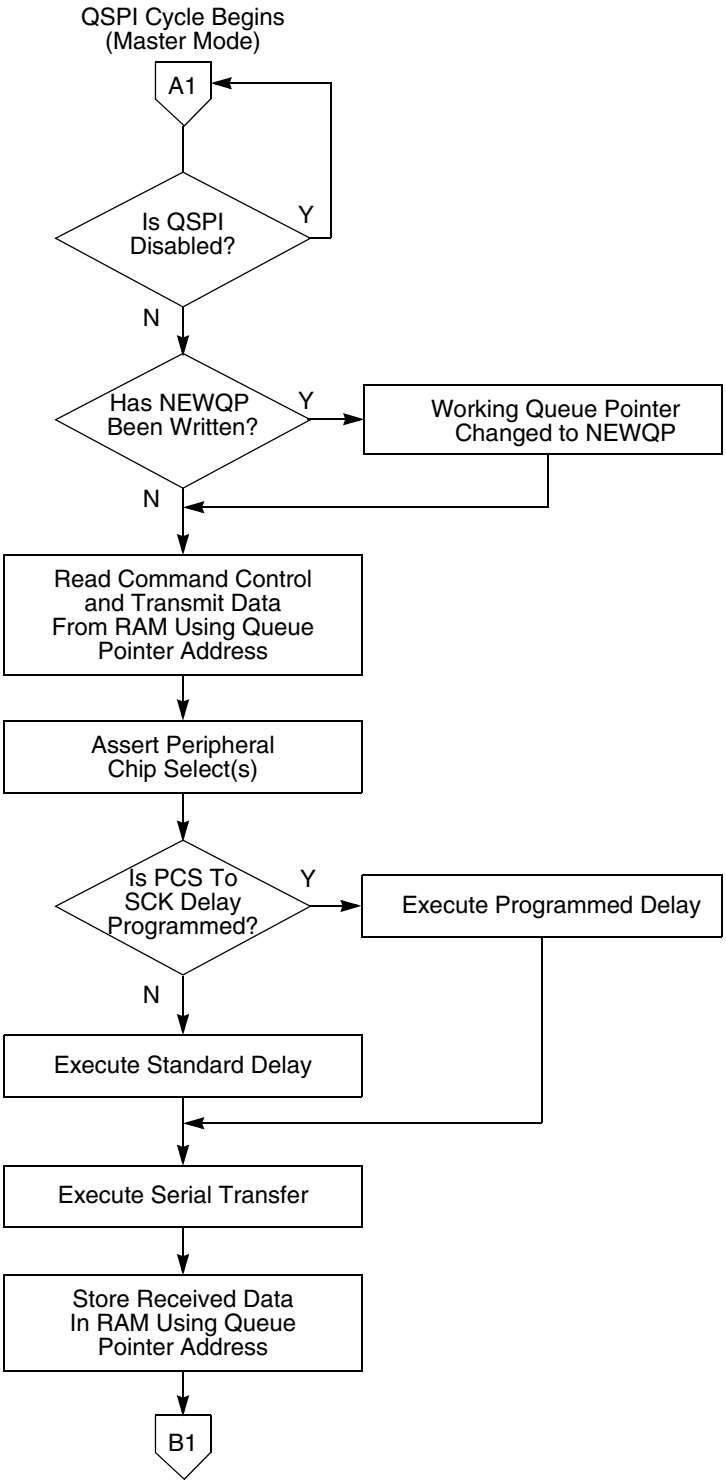

Figure 15-19. Flowchart of QSPI Master Operation (Part 1)

15.8.6 Example QSCI1 Transmit for 17 Data Bytes

Figure 15-36 below shows a transmission of 17 data frames. The bold type indicates the current value for QTPNT and QPEND. The italic type indicates the action just performed by hardware. Regular type indicates the actions that should be performed by software before the next event.

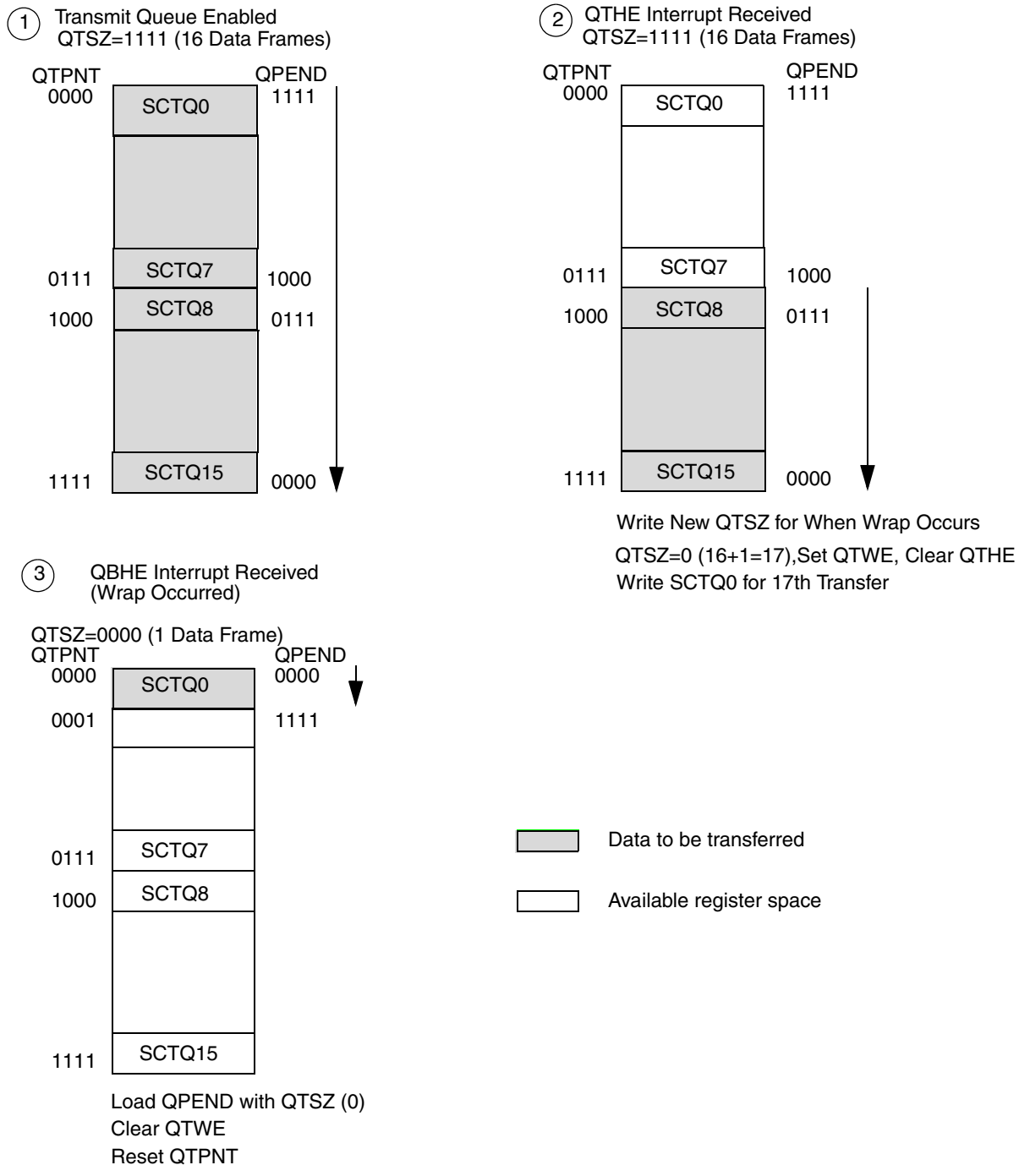

Figure 15-36. Queue Transmit Example for 17 Data Bytes

Table 16-23. ESTAT Bit Descriptions (continued)

Bits	Name	Description
13	BOFFINT	Bus off interrupt. The BOFFINT bit is used to request an interrupt when the TouCAN enters the bus off state. 0 No bus off interrupt requested 1 When the TouCAN state changes to bus off, this bit is set, and if the BOFFMSK bit in CANCTRL0 is set, an interrupt request is generated. This interrupt is not requested after reset.
14	ERRINT	Error Interrupt. The ERRINT bit is used to request an interrupt when the TouCAN detects a transmit or receive error. 0 No error interrupt request 1 If an event which causes one of the error bits in the error and status register to be set occurs, the error interrupt bit is set. If the ERRMSK bit in CANCTRL0 is set, an interrupt request is generated. To clear this bit, first read it as a one, then write as a zero. Writing a one has no effect.
15	WAKEINT	Wake interrupt. The WAKEINT bit indicates that bus activity has been detected while the TouCAN module is in low-power stop mode. 0 No wake interrupt requested 1 When the TouCAN is in low-power stop mode and a recessive to dominant transition is detected on the CAN bus, this bit is set. If the WAKEMSK bit is set in CANMCR, an interrupt request is generated.

Table 16-24. Transmit Bit Error Status

BITERR[1:0]	Bit Error Status
00	No transmit bit error
01	At least one bit sent as dominant was received as recessive
10	At least one bit sent as recessive was received as dominant
11	Not used

Table 16-25. Fault Confinement State Encoding

FCS[1:0]	Bus State
00	Error active
01	Error passive
1X	Bus off

16.7.13 Interrupt Mask Register (IMASK)

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	IMASKH								IMASKL							
SRESET	0000_0000_0000_0000															
Addr	0x30 70A2 (IMASK_A); 0x30 74A2 (IMASK_B); 0x30 78A2 (IMASK_C)															

Figure 16-20. Interrupt Mask Register (IMASK)

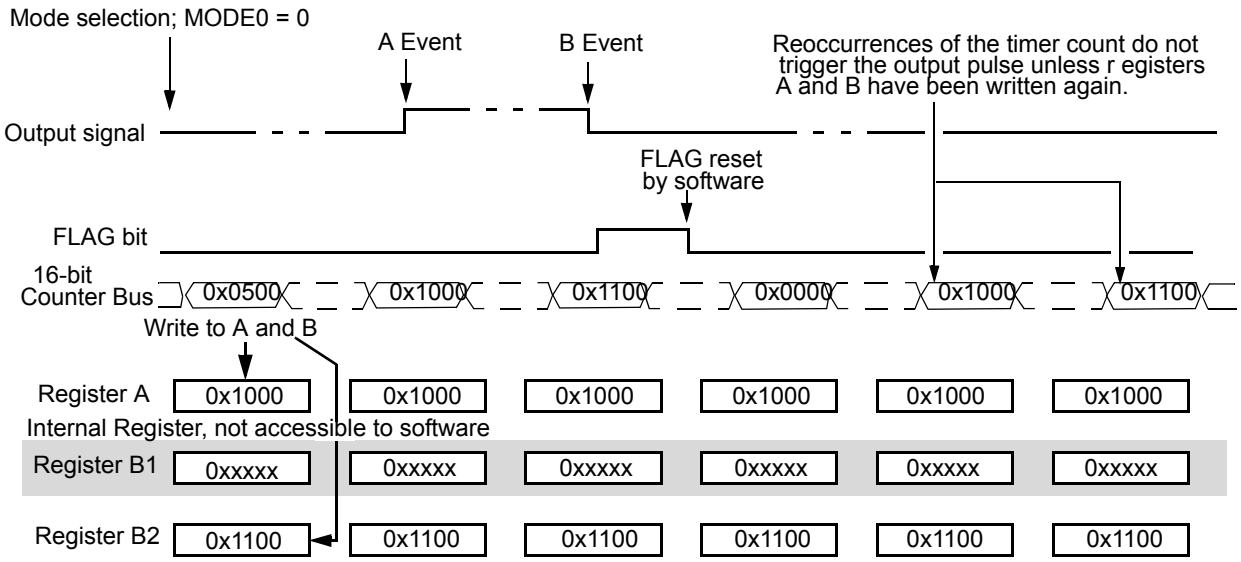

Figure 17-19. Single Shot Output Pulse Example

17.9.3.5.2 Single Output Compare Operation

The single output compare operation is selected by writing to only one of the two data registers (A or B), thus enabling only one of the comparators. Following the first successful match on the enabled channel, the output level is fixed and remains at the same level indefinitely with no further software intervention being required. To generate a single output compare, the OCAB mode should be used to generate a flag on both the A and the B match.

NOTE

In this mode, registers A and B2 are accessible to the user software (at consecutive addresses).

Figure 17-20 provides an example of how the MDASM can be used to perform a single output compare.

- The value 0x0000 in the period register, causes the counter to act like a free running counter. This condition creates a period of 65536 PWM clock periods.
- The value 0x0001 in the period register will always cause a period match to occur and the counter will never decrement below 0x0001. This condition is defined as a period of "1" PWM clock count. The output flip-flop is always set unless MPWMPULR = 0x0000, when the output flip-flop is always reset. Refer to Section 17.10.3.5, "Duty Cycles (0% and 100%)" for details about 0% and 100% duty cycles.
- Writing value 0x0002 in the period register causes a period match to occur every two clock periods. The counter decrements from 0x0002 to 0x0001, and then it is initialized back to 0x0002. This condition is defined as a period of 2 clock counts. Note that the value 0x0002 loaded in the period register and a value of 0x0001 in the pulse width register is the condition to obtain the maximum possible output frequency for a given clock period.

The relationship between the output frequency obtained (F_{PWMO}) and the MIOS14 CLOCK frequency (f_{SYS}), the MCPSM clock divide ratio (N_{MCPSM}), the counter divide ratio (N_{MPWMSM}) and the value loaded in the counter ($V_{COUNTER}$) is given by the following equation:

$$f_{PWMO} = \frac{f_{SYS}}{N_{MCPSM} \cdot N_{MPWMSM} \cdot V_{COUNTER}}$$

17.10.3.4 Pulse Width Registers

The pulse width section is composed of two 16-bit data registers (MPWMPULR1 and MPWMPULR2). Only MPWMPULR1 is accessible by software. The software establishes the pulse width of the MPWMSM output signal in MPWMPULR1. MPWMPULR2 is used as a double buffer of MPWMPULR1.

When the MPWMSM is running in transparent mode, the pulse width value in MPWMPULR1 is immediately transferred in MPWMPULR2 so that the new value takes effect immediately.

NOTE

When the MPWMSM is in disable mode, writing to MPWMPULR1 will write automatically to MPWMPULR2.

When the MPWMSM is not running in double-buffered mode, the pulse width value in MPWMPULR1 can be changed at any time without affecting the current pulse width of the output signal. The new value in MPWMPULR1 will be transferred to MPWMPULR2 only when the down-counter reaches the value of 0x0001.

When the counter first reaches the value in MPWMPULR2, the output flip-flop is set. The output is reset when the counter reaches 0x0001. The pulse width match starts the width of the output signal, it does not affect the counter. MPWMPULR1 is software readable and writable at any time. The MPWMSM does not modify the content of MPWMPULR1.

The PWM output pulse width can be as wide as one period minus one MPWMSM clock count: (i.e., MPWMPULR2 = MPWMPERR — [one MPWMSM clock count]). At the other end of the pulse width range, MPWMPULR2 can contain 0x0001 to create a pulse width of one PWM clock count.

24.8.2.2 Indirect Branch Messages

Indirect branches include interrupts, exceptions, and all taken branches whose destination is determined at run time. For the RCPU, certain sequential instructions are tagged with the indirect change-of-flow attribute because these instruction affect the machine in a similar manner to true indirect change-of-flow instructions. These instructions are the rfi, isync, mtmsr and certain mtspr (to CMPA – CMPF, ICTRL, ECR and DER)

The program trace indirect branch message has the following format:

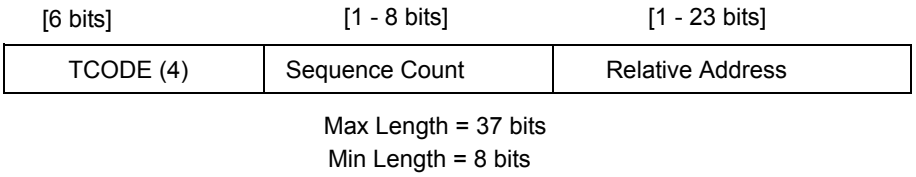

Figure 24-20. Indirect Branch Message Format

For compressed code support, six additional bits indicate the starting bit address within the word of the compressed instruction.

The program trace indirect branch with compressed code message has the format shown in Figure 24-21. The format of the bit address field is shown in Figure 24-22. The bit definitions are shown in Table 24-26.

NOTE

On the MPC562/MPC564, the bit pointer should be multiplied by 2 (shift left on bit) for the actual starting bit position.

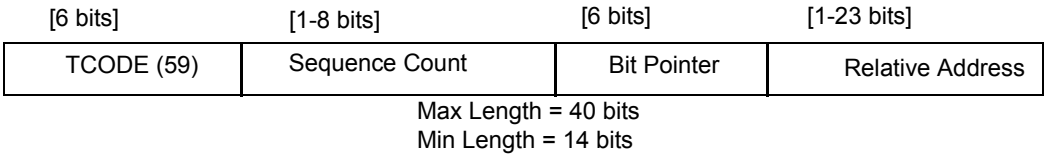

Figure 24-21. Indirect Branch Message Format with Compressed Code

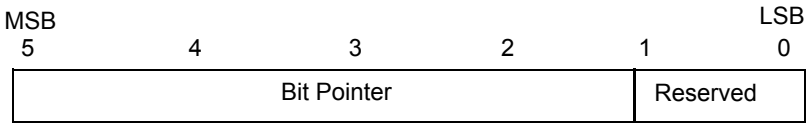

Figure 24-22. Bit Pointer Format with Compressed Code

Table 24-26. Bit Pointer Format

RCPU Bits	Nexus Bits	Name	Description
4:5	0:1	—	Reserved (Unused)
0:3	2:5	BP	Bit pointer. This value is 1/2 of the actual bit position on which the instruction starts.

CONTROL BITS

	NAME	OPTIONS	ADDRESSES
0 1 2 3	Channel Function Select	xxxx – TSM Function Number. Assigned during microcode assembly. See Table D-1	0x30YY0C – 0x30YY12
0 1	Host Sequence	x0 – Rotate Pin_Sequence Once Between Steps x1 – Split Mode Acceleration Table 1x – Rotate Pin_Sequence Once Between Steps 1x – Rotate Pin_Sequence Twice Between Steps	0x30YY14 – 0x30YY16
0 1	Host Service Request	00 – No Host Service (Reset Condition) 01 – Initialize, Pin Low 10 – Initialize, Pin High 11 – Move Request (Master Only)	0x30YY18 – 0x30YY1A
0 1	Channel Priority	00 – Disabled 01 – Low Priority 10 – Medium Priority 11 – High Priority	0x30YY1C – 0x30YY1E
0	Channel Interrupt Enable	0 – Channel Interrupt Disabled 1 – Channel Interrupt Enabled	0x30YY0A
0	Channel Interrupt Status	0 – Channel Interrupt Not Asserted 1 – Channel Interrupt Asserted	0x30YY20

PARAMETER RAM

ADDRESS OFFSETS	BITS 0 1 2 3 4 5 6 7	BITS 8 9 10 11 12 13 14 15	
0x30XX(W+1)0	ACCEL_RATIO_2	ACCEL_RATIO_1	Param 0
0x30XX(W+1)2	ACCEL_RATIO_4	ACCEL_RATIO_3	Param 1
0x30XX(W+1)4	ACCEL_RATIO_6	ACCEL_RATIO_5	Param 2
0x30XX(W+1)6	ACCEL_RATIO_8	ACCEL_RATIO_7	Param 3
0x30XX(W+1)8	ACCEL_RATIO_10	ACCEL_RATIO_9	Param 4
0x30XX(W+1)A	ACCEL_RATIO_12	ACCEL_RATIO_11	Param 5
0x30XX(W+1)C[1]	ACCEL_RATIO_14[1]	ACCEL_RATIO_13[1]	Param 6
:	:	:	:
0x30XX(W+3)A[1]	ACCEL_RATIO_36[1]	ACCEL_RATIO_35[1]	Param 29

1. Optional additional parameters not available in all cases. Refer to Freescale Programming Note TPUPN04/D for details.

= Written By RCPU
= Written by RCPU and TPU
W = Channel Number
= Written By TPU
= Unused Parameters
For address offsets: XX=41 for TPU_A, 45 for TPU_B
YY=40 for TPU_A, 44 for TPU_B
See Table 19-24 for the PRAM Address Offset Map.

Figure D-5. TSM Parameters — Slave Mode

NOTE

Only the clock channel requires any programming. The data-in and data-out channels are entirely under TPU3 microcode control.

Table F-28. MPC561/MPC563 Signal Names and Pin Names (continued)

Signal Name	Pin Name	Ball Assignment
Global Power Supplies		
NVDDL	nvddl	AC10
		AC15
		AC19
		AC4
		AD3
		AE2
		AF1
		C9
		D9
		Y23
VDD	vdd	A1
		A25
		AC22
		AD23
		AE24
		AF25
		B2
		B24
		C23
		C3
		D22
		D4
		V23
VDDH	vddh	AF21
		AF5
		C19
		C22
		D19
		E1
		F23
		T25

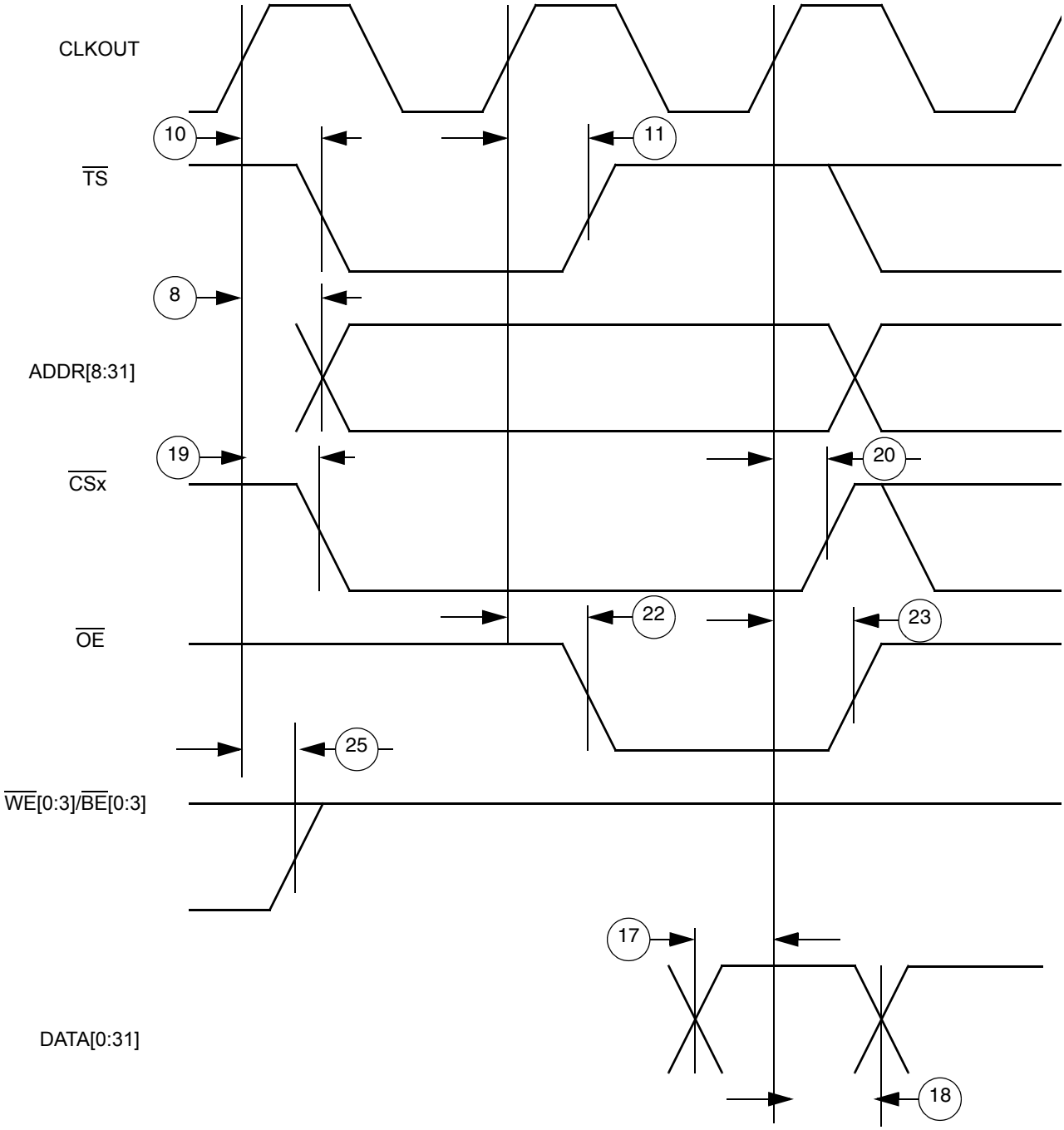

Figure G-15. External Bus Read Timing (GPCM Controlled – ACS = '00')