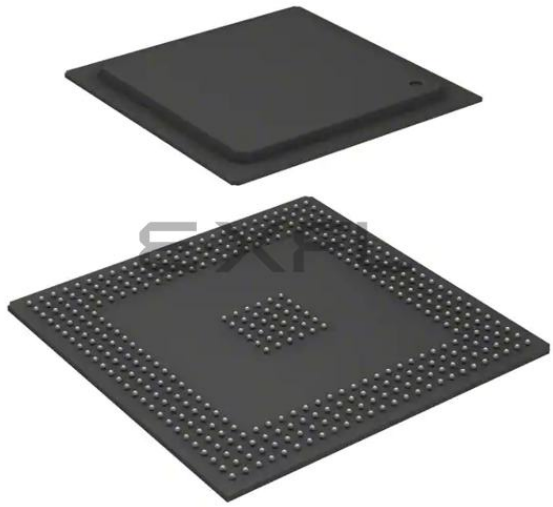

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PowerPC
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	64
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 2.7V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	388-BBGA
Supplier Device Package	388-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc562mzp66r2

Table 2-1. MPC561/MPC563 Signal Descriptions (continued)

Signal Name	No. of Signals	Type	Function after Reset[1]	Description
Clocks and PLL				
XTAL	1	O	XTAL	XTAL. This output signal is one of the connections to an external crystal for the internal oscillator circuitry.
EXTAL	1	I	EXTAL	EXTAL. This signal is one of the connections to an external crystal for the internal oscillator circuitry. If EXTAL is unused, it must be grounded.
XFC	1	I	XFC	External Filter Capacitance. This input signal is the connection for an external capacitor filter for the PLL circuitry.
CLKOUT	1	O	CLKOUT	Clock Out. This output signal is the clock system frequency. The CLKOUT drive strength can be configured to full strength, half strength, quarter strength, or disabled. The drive strength is configured using the COM[0:1] bits and CQDS bits in the SCCR register in the USIU.
EXTCLK	1	I	EXTCLK	EXTCLK. This is the external frequency source for the MPC561/MPC563. If EXTCLK is unused, it must be grounded.
ENGCLK / BUCLK	1	O	ENGCLK (2.6 V)	ENGCLK. This is the engineering clock output. Drive voltage can be configured to 2.6 V, 5 V (with slew-rate control), or disabled. The drive voltage is configured using the EECLK[0:1] bits in the SCCR register in the SIU.
		O		BUCLK. When the MPC561/MPC563 is in limp mode, it is operating from a less precise on-chip ring oscillator to allow the system to continue minimum functionality until the system clock is fixed. This backup clock can be seen externally if selected by the values of the EECLK[0:1] bits in the SCCR register in the USIU.
VDDSYN	1	I	VDDSYN	VDDSYN. This is the power supply of the PLL circuitry.
VSSSYN	1	I	VSSSYN	VSSSYN. This is the ground reference of the PLL circuitry.
Configuration				
PULL_SEL[3]	1	I	PULL_SEL	Pull Select. PULL_SEL determines whether the pull devices on the MIOS and TPU signals are pull-ups or pull-downs. When pull-ups are selected, the pull-ups are to 5.0 V except the following MIOS signals will be pulled to 2.6V: VF[0:2]/MPIO32B[0:2], VFLS[0:1]/MPIO32B[3:4], and MDO[7:4]/MPIO32B[7:10]. When this pin is low, pull-downs are selected.
TouCAN				
A_CNTX0	1	O	A_CNTX0	TouCAN_A Transmit Data. This signal is the serial data output.
A_CNRX0	1	I	A_CNRX0	TouCAN_A Receive Data. This signal is the serial data input.
B_CNTX0	1	O	B_CNTX0	TouCAN_B Transmit Data. This signal is the serial data output.

Refer to Section 2.4, “Pad Module Configuration Register (PDMCR2),” and Section 10.9.4, “Memory Controller Option Registers (OR0–OR3),” for more information on PREDIS_EN, and EHTR configuration bits.

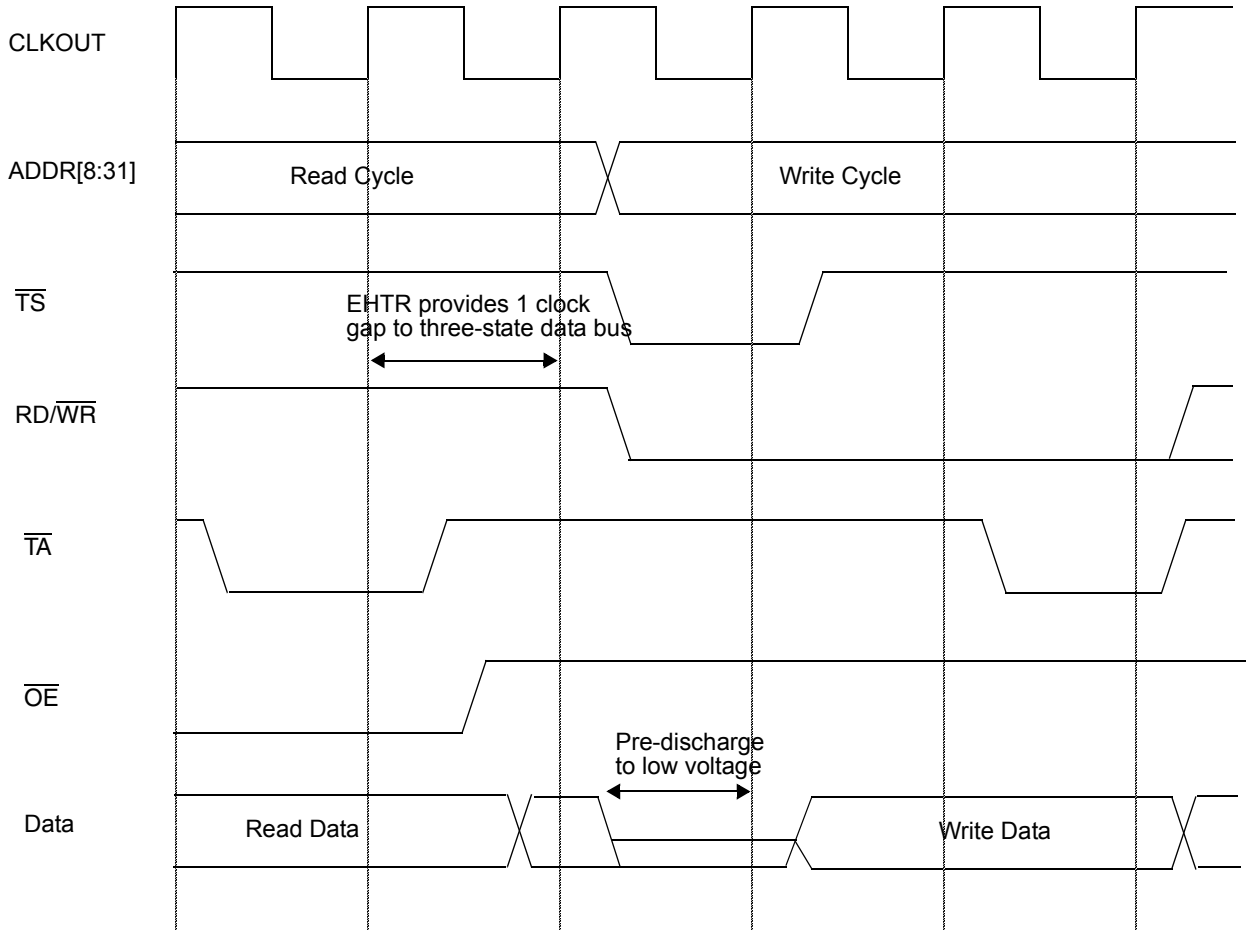


Figure 9-11. Read Followed by Write when Pre-Discharge Mode is Enabled, and EHTR is Set

9.5.4 Burst Transfer

The MPC561/MPC563 uses non-wrapping burst transfers to access operands of up to 32 bytes (eight words). A non-wrapping burst access stops accessing the external device when the word address is modulo four/eight. Burst configuration is determined by the value of BURST_EN in the SIUMCR register. See Chapter 5, “Unified System Interface Unit (USIU) Overview” for further details. The MPC561/MPC563 begins the access by supplying a starting address that points to one of the words in the array and requires the memory to sequentially drive or sample each word on the data bus. The selected slave device must internally increment ADDR28 and ADDR29 (and ADDR30 in the case of a 16-bit port slave device, and also ADDR31 in the case of an 8-bit port slave device) of the supplied address for each transfer, causing the address to reach a four/eight word boundary, and then stop. The address and transfer attributes supplied by the MPC561/MPC563 remain stable during the transfers. The selected device terminates each transfer by driving or sampling the word on the data bus and asserting $\overline{TA}$.

10.2.6.2 Case 2: Short Setup Time

Initial access:

Enabling short setup time requires one clock cycle:

Initial access time of memory + Data setup time of CPU + Delays = 49 + 3 + 1= 53ns

The number of clocks required = $\frac{53}{17.9} = 2.96 + 1(\text{SST Enable Clock}) = 3.96$ therefore 4 clocks are required.

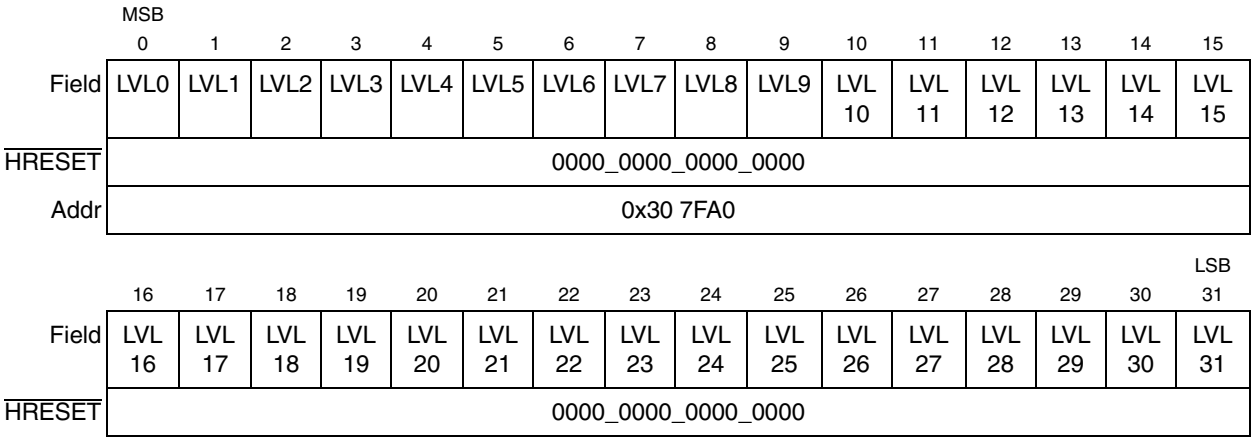


Figure 12-8. Pending Interrupt Request Register (UIPEND)

Table 12-7. UIPEND Bit Descriptions

Bits	Name	Description
0:31	LVL*x*	Pending interrupt request level. Accessible only in supervisor mode. LVL*x* identifies the interrupt source as UIMB LVL*x*, where *x* is the interrupt number.

Table 14-19. CCW Bit Descriptions (continued)

Bits	Name	Description
8	IST	Input Sample Time. The IST field allows software to specify the length of the sample window. Provision is made to vary the input sample time, through software control, to offer flexibility in the source impedance of the circuitry providing the QADC64E analog channel inputs. Longer sample times permit more accurate A/D conversions of signals with higher source impedances. The programmable sample time can also be used to increase the time interval between conversions to adjust the queue execution time or the sampling rate. 0 QCLK period x 2 1 QCLK period x 8
9:15	CHAN[6:0]	Channel Number. The CHAN field selects the input channel number. The software programs the channel field of the CCW with the channel number corresponding to the analog input signal to be sampled and converted. The analog input signal channel number assignments and the signal definitions vary depending on whether the multiplexed or non-multiplexed mode is used by the application. As far as the queue scanning operations are concerned, there is no distinction between an internally or externally multiplexed analog input. Refer to Section 14.2.5, “External Multiplexing” for more information on external multiplexing. Table 14-20 and Table 14-21 show the channel number assignments

Table 14-20. QADC64E_A Multiplexed Channel Assignments and Signal Designations

Multiplexed Input Signals				Channel Number in CCW CHAN Field	
Port Signal Name	Analog Signal Name	Other Functions / Descriptions	Signal Type	Binary	Decimal
ANw/A_PQB0	AN00 to AN07	—	Input	0000000 to 0000111	0 to 7
ANx/A_PQB1	AN08 to AN15	—	Input	0001000 to 0001111	8 to 15
ANy/A_PQB2	AN16 to AN23	—	Input	0010000 to 0010111	16 to 23
ANz/A_PQB3	AN24 to AN31	—	Input	0011000 to 0011111	24 to 31
—	RESERVED	—	—	0100000 to 0101001	32 to 41
—	RESERVED	—	—	0101010	42
—	RESERVED	—	—	0101011	43
A_PQB0 A_PQB1 A_PQB2 A_PQB3	AN44 AN45 AN46 AN47	ANw ANx ANy ANz	Input/Output Input/Output Input/Output Input/Output	0101100 0101101 0101110 0101111	44 45 46 47
A_PQB4 A_PQB5 A_PQB6 A_PQB7	AN48 AN47 AN50 AN51	— — — —	Input/Output Input/Output Input/Output Input/Output	0110000 0110001 0110010 0110011	48 49 50 51

Analog supplies should be isolated from digital supplies as much as possible. This necessity stems from the higher performance requirements often associated with analog circuits. Therefore, deriving an analog supply from a local digital supply is not recommended. However, if for economic reasons digital and analog power are derived from a common regulator, filtering of the analog power is recommended in addition to the bypassing of the supplies already mentioned.

NOTE

An RC low pass filter could be used to isolate the digital and analog supplies when generated by a common regulator. If multiple high precision analog circuits are locally employed (i.e., two A/D converters), the analog supplies should be isolated from each other as sharing supplies introduces the potential for interference between analog circuits.

Grounding is the most important factor influencing analog circuit performance in mixed signal systems (or in stand-alone analog systems). Close attention must be paid not to introduce additional sources of noise into the analog circuitry. Common sources of noise include ground loops, inductive coupling, and combining digital and analog grounds together inappropriately.

The problem of how and when to combine digital and analog grounds arises from the large transients which the digital ground must handle. If the digital ground is not able to handle the large transients, the current from the large transients can return to ground through the analog ground. It is the excess current overflowing into the analog ground which causes performance degradation by developing a differential voltage between the true analog ground and the microcontroller's ground signal. The end result is that the ground observed by the analog circuit is no longer true ground and often ends in skewed results.

Two similar approaches designed to improve or eliminate the problems associated with grounding excess transient currents involve star-point ground systems. One approach is to star-point the different grounds at the power supply origin, thus keeping the ground isolated. Refer to Figure 14-49.

15.3 Memory Maps

The QSMCM memory maps, shown in Table 15-1 and Table 15-2, includes the global registers, the QSPI and dual SCI control and status registers, and the QSPI RAM. The QSMCM memory map can be divided into supervisor-only data space and assignable data space. The address offsets shown are from the base address of the QSMCM module. Refer to Figure 1-4 for a diagram of the MPC561/MPC563 internal memory map.

Table 15-1. QSMCM Register Map

Access[1]	Address	MSB[2] 0	LSB 15
S	0x30 5000	QSMCM Module Configuration Register (QSMCMMCR) See Table 15-7 for bit descriptions.	
T	0x30 5002	QSMCM Test Register (QTEST)	
S	0x30 5004	Dual SCI Interrupt Level (QDSCI_IL) See <XrefBlue>Table 15-5 for bit descriptions.	Reserved
S	0x30 5006	Reserved	Queued SPI Interrupt Level (QSPI_IL) See <XrefBlue>Table 15-6 for bit descriptions.
S/U	0x30 5008	SCI1Control Register 0 (SCC1R0) See <XrefBlue>Table 15-24 for bit descriptions.	
S/U	0x30 500A	SCI1Control Register 1 (SCC1R1) See <XrefBlue>Table 15-25 for bit descriptions.	
S/U	0x30 500C	SCI1 Status Register (SC1SR) See <XrefBlue>Table 15-26 for bit descriptions.	
S/U	0x30 500E	SCI1 Data Register (SC1DR) See <XrefBlue>Table 15-27 for bit descriptions.	
S/U	0x30 5010	Reserved	
S/U	0x30 5012	Reserved	
S/U	0x30 5014	Reserved	QSMCM Port Q Data Register (PORTQS) See Section 15.5.1, “Port QS Data Register (PORTQS),” for bit descriptions.
S/U	0x30 5016	QSMCM Pin Assignment Register (PQSPAR) See <XrefBlue>Table 15-10 for bit descriptions.	QSMCM Data Direction Register (DDRQS) See <XrefBlue>Table 15-11 for bit descriptions.
S/U	0x30 5018	QSPI Control Register 0 (SPCR0) See <XrefBlue>Table 15-13 for bit descriptions.	
S/U	0x30 501A	QSPI Control Register 1 (SPCR1) See <XrefBlue>Table 15-15 for bit descriptions.	
S/U	0x30 501C	QSPI Control Register 2 (SPCR2) See <XrefBlue>Table 15-16 for bit descriptions.	
S/U	0x30 501E	QSPI Control Register 3 (SPCR3) See <XrefBlue>Table 15-17 for bit descriptions.	QSPI Status Register (SPSR) See <XrefBlue>Table 15-18 for bit descriptions.

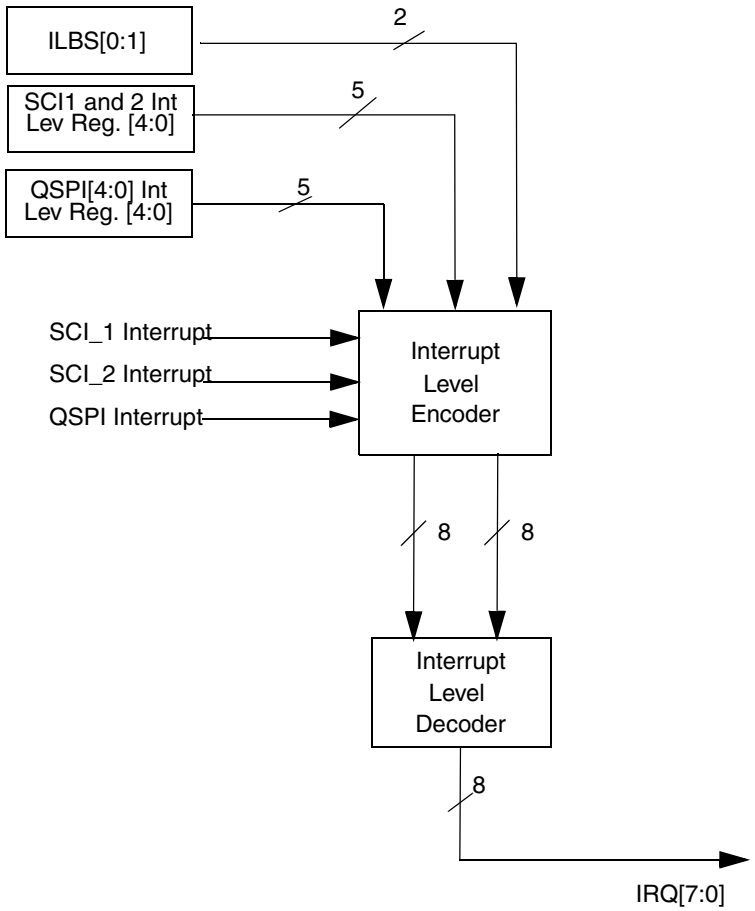


Figure 15-3. Interrupt Hardware Block Diagram

15.4.5 QSPI Interrupt Generation

15.4.6 QSMCM Configuration Register (QSMCMMCR)

The QSMCMMCR contains parameters for interfacing to the CPU and the intermodule bus. This register can be modified only when the CPU is in supervisor mode.

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	STOP	FRZ1	—						SUPV	—						
$\overline{\text{SRESET}}$	0	0	00_0000						1	000_0000						
Addr	0x30 5000															

Figure 15-4. QSMCM Configuration Register (QSMCMMCR)

Table 15-14. Bits Per Transfer (continued)

Bits[3:0]	Bits per Transfer
1011	11
1100	12
1101	13
1110	14
1111	15

15.6.1.2 QSPI Control Register 1 (SPCR1)

SPCR1 enables the QSPI and specifies transfer delays. The CPU has read/write access to SPCR1, but the QSPI has read access only to all bits except SPE. SPCR1 must be written last during initialization because it contains SPE. The QSPI automatically clears this bit after it completes all serial transfers or when a mode fault occurs. Writing a new value to SPCR1 while the QSPI is enabled disrupts operation.

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	SPE	DSCKL							DTL							
$\overline{\text{SRESET}}$	0	000_0100							0000_0100							
Addr	0x30 501A															

Figure 15-12. SPCR1 — QSPI Control Register

Table 15-15. SPCR1 Bit Descriptions

Bits	Name	Description
0	SPE	QSPI enable. Refer to Section 15.6.4.1, “Enabling, Disabling, and Halting the SPI. 0 = QSPI is disabled. QSPI pins can be used for general-purpose I/O. 1 = QSPI is enabled. Pins allocated by PQSPAR are controlled by the QSPI.
1:7	DSCKL	Delay before SCK. When the DSCK bit is set in a command RAM byte, this field determines the length of the delay from PCS valid to SCK transition. The following equation determines the actual delay before SCK: $\text{PCS to SCK Delay} = \frac{\text{DSCKL}}{f_{SYS}}$ where DSCKL equals is in the range of 1 to 127. Refer to Section 15.6.5.3, “Delay Before Transfer for more information.
8:15	DTL	Length of delay after transfer. When the DT bit is set in a command RAM byte, this field determines the length of the delay after a serial transfer. The following equation is used to calculate the delay: $\text{Delay after Transfer} = \frac{32\text{XDTL}}{f_{SYS}}$ where DTL is in the range of 1 to 255. A zero value for DTL causes a delay-after-transfer value of $8192 \div f_{SYS}$ (204.8 µs with a 40-MHz IMB3 clock). Refer to Section 15.6.5.4, “Delay After Transfer for more information.

24.2.2 Security

Security is provided via the UC3F censorship mechanism. If a UC3F array is in censored mode, reads or writes to the UC3F will not be allowed (RCPU will not be able to fetch instructions from the UC3F) once any of the following cases are detected:

- Program trace and/or data trace are enabled
- Read/write access is attempted (can be to any address location)
- RCPU development access is enabled.

24.2.3 Normal

Normal operation of the READI module allows for developement support features to be available. These features include control of the device, access to registers, and the ability to perform data or instruction trace.

24.2.4 Disabled

If $\overline{\text{EVTI}}$ is negated at negation of $\overline{\text{RSTI}}$, the READI module will be disabled. No trace output will be provided, and output auxiliary port will be three-stated. Any message sent by the tool is ignored.

24.3 Parametrics

With 32-deep message queues, throughput numbers were calculated for the following benchmark codes [assuming full port mode]:

- For an example benchmark which had 10.9% direct branches, 2.5% indirect branches, 10.4% data writes, and 19.3% data reads, approximately 20% of total data trace accesses will be traced.
- For another example benchmark which had 9.8% direct branches, 2.8% indirect branches, 6.6% data writes, and 18.3% data reads, approximately 27% of total data trace accesses will be traced.

NOTE

The queue is only 16 messages deep on revisions prior to Rev. D of the MPC561 and is 16 deep in Rev. B and earlier versions of the MPC563.

For reduced port mode, the data trace feature should not be used, or used sparingly, so as not to cause queue overruns.

24.4 Messages

The READI module implements messaging via the auxiliary port according to the IEEE-ISTO 5001 - 1999. Messaging will be implemented via transfer codes (TCODEs) on the auxiliary port. The TCODE number for the message identifies the transfer format (the number and/or size of packets to be transferred) and the purpose of each packet.

Public messages outlined in Table 24-1 are supported by READI.

Table 24-19. Public Messages Supported (continued)

Message Name	Minimum Packet Size (bits)	Maximum Packet Size (bits)	Packet Type	Packet Description	Direction
Resource Full Message[2]	6	6	Fixed	TCODE number = 27 (0x1B)	From Device
	1	4	Variable	resource code	

1 Refer to Table 24-20 for the error message codes.

2 Not available on the MPC561 prior to revision D and not available on MPC563 revision B and earlier.

Table 24-20. Error Message Codes

Error Code	Description
00000	Ownership trace overrun[1]
00001	Program trace overrun[1]
00010	Data trace overrun[1]
00011	Read/write access error
00100	Invalid message
00101	Invalid access opcode
00110	Watchpoint overrun
00111	Program/data/ownership trace overrun
01000-10111	Reserved
11000-11111	Vendor Defined

1 This error message is not available on the MPC561 prior to revision D and is not available on the MPC563 revision B and earlier.

Vendor-defined messages outlined in Table 24-21 are also supported by READI.

Table 24-21. Vendor-Defined Messages Supported

TCODE Name	Minimum Packet Size (bits)	Maximum Packet Size (bits)	Packet Type	Packet Description	Direction
Dev Port Access — DSDI Data Message	6	6	Fixed	TCODE number = 56 (0x38)	From Tool
	10	35	Variable	BDM Development Serial Data In (DSDI)	
Dev Port Access —DSDO Data Message	6	6	Fixed	TCODE number = 57 (0x39)	From Device
	10	35	Variable	BDM Development Serial Data Out (DSDO)	
Dev Port Access — BDM Status Message	6	6	Fixed	TCODE number = 58 (0x3A)	From Device
	1	1	Fixed	BDM status	

Figure 24-16. Enabling Program Trace Out of System Reset

24.7.7 READI Signals

The READI signals support Nexus (IEEE-ISTO 5001-1999) auxiliary port interface for debug. There are two modes available, full port mode and reduced port mode. Reduced port mode allows for a 1 bit input stream and a 2 bit output stream. Full port mode allows for a 2 bit input stream and an 8 bit output stream. See Figure 24-11 for READI mode selection.

Steps to Enter READI (Nexus) mode:

1. Negate PORESET while holding JCOMP/$\overline{\text{RSTI}}$ low.
2. Configure TMS/$\overline{\text{EVTI}}$ and TDI/DSDI/MDI[0] while JCOMP/$\overline{\text{RSTI}}$ is low. ($\overline{\text{EVTI}}$ = low to enable Nexus)
3. Negate JCOMP/$\overline{\text{RSTI}}$.
4. If MDI[0] is high at JCOMP/$\overline{\text{RSTI}}$ negation, then full port mode is enabled otherwise Reduced mode is selected.

To exit READI mode:

1. Reassert JCOMP/$\overline{\text{RSTI}}$ to disable READI.

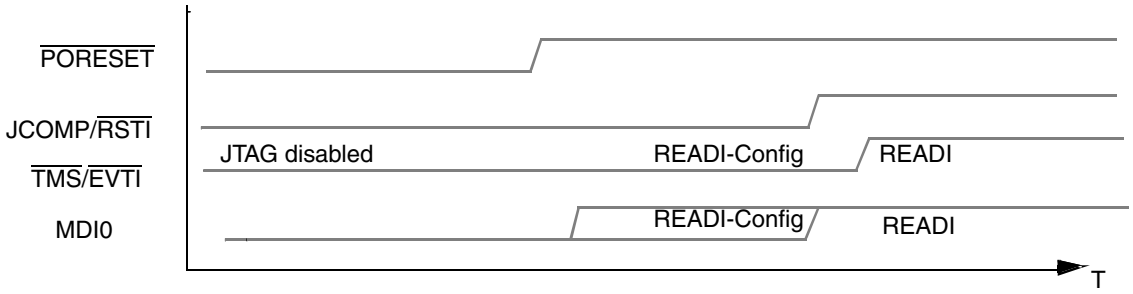


Figure 24-17. READI Mode Selection

24.7.7.1 Reset Configuration for Debug Mode

To enable RCPU development access via the READI signals, the reset sequence outlined below should be used:

- Assert READI reset ($\overline{\text{RSTI}}$), event-in ($\overline{\text{EVTI}}$) and system reset ($\overline{\text{HRESET}}$)
- Negate $\overline{\text{RSTI}}$
- Upon negation of $\overline{\text{RSTI}}$, tool should configure the DOR, DME, and DPA fields in the DC register to desired setting.
- Tool negates $\overline{\text{HRESET}}$ at least 16 system clocks after receiving the device ready message

Refer to Figure 24-84 for further details.

Table B-9. Time Processor Unit 3 A and B (TPU3 A and B) (continued)

Address	Access	Symbol	Register	Size	Reset
0x30 4150 – 0x30 415F	S/U[3]	—	TPU3_A Channel 5 Parameter Registers. See Section 19.4.15 for more information.	16, 32[2]	—
0x30 4160 – 0x30 416F	S/U[3]	—	TPU3_A Channel 6 Parameter Registers. See Section 19.4.15 for more information.	16, 32[2]	—
0x30 4170 – 0x30 417F	S/U[3]	—	TPU3_A Channel 7 Parameter Registers. See Section 19.4.15 for more information.	16, 32[2]	—
0x30 4180 – 0x30 418F	S/U[3]	—	TPU3_A Channel 8 Parameter Registers. See Section 19.4.15 for more information.	16, 32[2]	—
0x30 4190 – 0x30 419F	S/U[3]	—	TPU3_A Channel 9 Parameter Registers. See Section 19.4.15 for more information.	16, 32[2]	—
0x30 41A0 – 0x30 41AF	S/U[3]	—	TPU3_A Channel 10 Parameter Registers. See Section 19.4.15 for more information.	16, 32[2]	—
0x30 41B0 – 0x30 41BF	S/U[3]	—	TPU3_A Channel 11 Parameter Registers. See Section 19.4.15 for more information.	16, 32[2]	—
0x30 41C0 – 0x30 41CF	S/U[3]	—	TPU3_A Channel 11 Parameter Registers. See Section 19.4.15 for more information.	16, 32[2]	—
0x30 41D0 – 0x30 41DF	S/U[3]	—	TPU3_A Channel 11 Parameter Registers. See Section 19.4.15 for more information.	16, 32[2]	—
0x30 41E0 – 0x30 41EF	S/U[3]	—	TPU3_A Channel 14 Parameter Registers. See Section 19.4.15 for more information.	16, 32[2]	—
0x30 41F0 – 0x30 41FF	S/U[3]	—	TPU3_A Channel 15 Parameter Registers. See Section 19.4.15 for more information.	16, 32[2]	—
TPU3_B					
0x30 4400[1]	S[1]	TPUMCR_B	TPU3_B Module Configuration Register	16 only	S, M
0x30 4402	T	TCR_B	TPU3_B Test Configuration Register	16	S, M
0x30 4404	T	DSCR_B	TPU3_B Development Support Control Register	16[2]	S, M
0x30 4406	T	DSSR_B	TPU3_B Development Support Status Register	16[2]	S, M
0x30 4408	S	TICR_B	TPU3_B Interrupt Configuration Register	16[2]	S, M
0x30 440A	S	CIER_B	TPU3_B Channel Interrupt Enable Register	16[2]	S, M
0x30 440C	S	CFSR0_B	TPU3_B Channel Function Selection Register 0	16[2]	S, M
0x30 440E	S	CFSR1_B	TPU3_B Channel Function Selection Register 1	16[2]	S, M
0x30 4410	S	CFSR2_B	TPU3_B Channel Function Selection Register 2	16[2]	S, M
0x30 4412	S	CFSR3_B	TPU3_B Channel Function Selection Register 3	16[2]	S, M
0x30 4414	S/U[3]	HSQR0_B	TPU3_B Host Sequence Register 0	16[2]	S, M
0x30 4416	S/U[3]	HSQR1_B	TPU3_B Host Sequence Register 1	16[2]	S, M
0x30 4418	S/U[3]	HSRR0_B	TPU3_B Host Service Request Register 0	16[2]	S, M
0x30 441A	S/U[3]	HSRR1_B	TPU3_B Host Service Request Register 1	16[2]	S, M

D.20 Serial Input/Output Port (SIOP)

The serial input/output port (SIOP) TPU3 function uses two or three TPU3 channels to form a uni- or bidirectional synchronous serial port that can be used to communicate with a wide variety of devices. It can be used to add serial capabilities to a device without a serial port, or to extend the capabilities of one with a hardware-synchronous port. The SIOP TPU3 function has been designed to closely resemble the SIOP hardware port found on some Freescale MCUs.

SIOP operates in master mode (the TPU3 always generates the clock) and has the following programmable features:

1. Choice of one-channel clock-only, two-channel clock + transmit, two-channel clock + receive, or three-channel clock + transmit + receive operating modes
2. Freely programmable baud-rate period over a 15-bit range of TCR1 counts
3. Selection of MSB or LSB first shift direction
4. Variable transfer size from 1 to 16 bits
5. Programmable clock polarity

When a transfer of data is complete, the SIOP function notifies the host RCPU by issuing an interrupt request. The arrangement of the multiple SIOP channels is fixed: the data-out channel is the channel above the clock channel and the data-in channel is the channel below the clock channel. In clock-only or uni-directional mode, the unused TPU3 channels are free to run other TPU3 functions. Two possible SIOP configurations are shown in Figure D-31

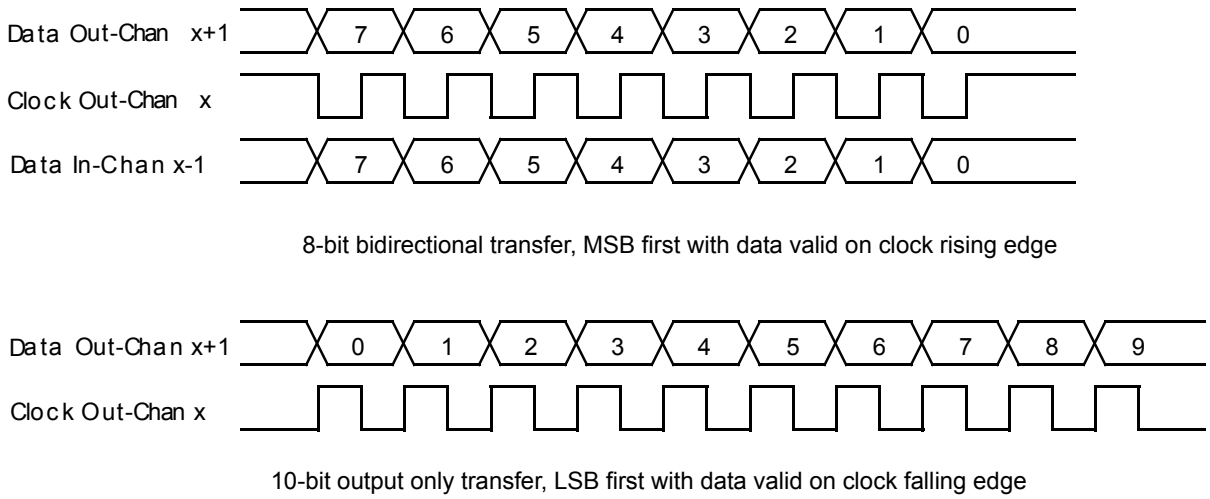


Figure D-31. Two Possible SIOP Configurations

D.20.1 Parameters

Figure D-32 shows the host interface areas and parameter RAM for the SIOP function. The following sections describe these parameters.

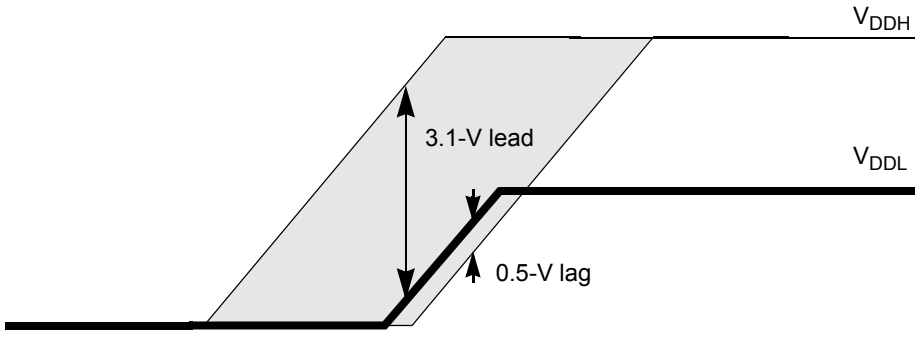
Table E-2. Instruction Timing Examples for Different Buses

Note: L = L-bus, U = U-bus, E = E-bus, C = CMF (Flash), IMB = intermodule bus, DC = DECRAM

Access	Number of Clocks													Total
	1	2	3	4	5	6	7	8	9	10	11	12	13	
Load/Store -> Ebus	L	U	E											6[1]
				E	U	L								
Load/Store -> IMB 16 bits	L	U	IMB											6
				IMB	U	L								
Instruction Fetch-> cmf new page 3 consecutive accesses	C,U													2
		U[2]												
		C,U												1
		U												
			C,U											1
			U											
Instruction Fetch-> DECRAM (Decompression off)	U	ICD U												
		ICD U	U											
Instruction Fetch-> cmf new page Load/Store -> IMB	C,U													2
		U												
	L	U	IMB											6
				IMB	U	L								
Instruction Fetch-> cmf new page Load/Store -> IMB		C	U											6
						U								
	L	U	IMB											6
				IMB	U	L								
External Bus-> cmf new page	E		U											5
				U	E									
External Bus-> IMB	E		U	IMB										7
					IMB	U	E							
Load/Store-> DECRAM	L	U												
			U	L										

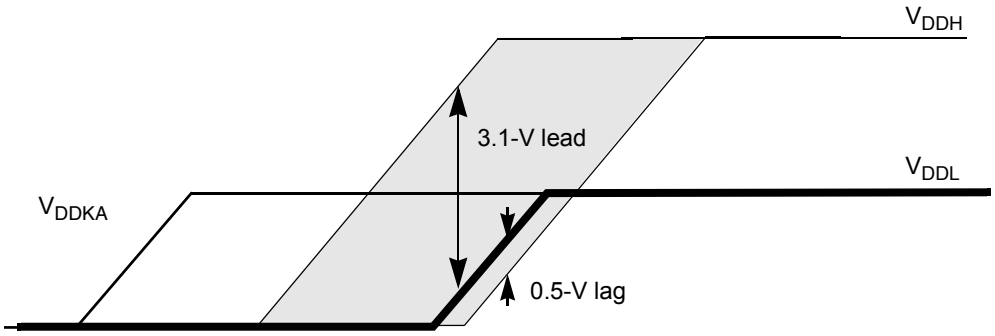
is required is due to ESD diodes in the pad logic for dual 2.6-V/5-V compliant pins and 2.6-V pins. The diodes are forward biased when V_{DDL} is greater than V_{DDH} and will start to conduct current.

Figure F-1 illustrates the power-up sequence if no keep-alive supply is required. Figure F-2 illustrates the power-up sequence if a keep-alive supply is required. The keep-alive supply should be powered-up at the same instant or before both the high voltage and low voltage supplies are powered-up.



V_{DDH} cannot lead V_{DDL} by more than 3.1 V
V_{DDH} cannot lag V_{DDL} by more than 0.5 V

Figure F-1. Option A Power-Up Sequence Without Keep-Alive Supply



V_{DDH} cannot lead V_{DDL} by more than 3.1 V
V_{DDH} cannot lag V_{DDL} by more than 0.5 V

Figure F-2. Option A Power-Up Sequence With Keep-Alive Supply

The option A power-down sequence (excluding V_{DDKA}) is

1. $V_{DDH} \leq V_{DDL} + 3.1$ V (V_{DDH} cannot lag V_{DDL} by more than 3.1 V)
2. $V_{DDH} \geq V_{DDL} - 0.5$ V (V_{DDH} cannot lead V_{DDL} by more than 0.5 V)

Figure F-3 illustrates the power-down sequence if no keep-alive supply is required.

Table F-10. Bus Operation Timing (continued)

Note: (V_{DD} = 2.6 V ± 0.1 V, V_{DDH} = 5.0 V ± 0.25 V, T_A = T_L to T_H, 50 pF load unless noted otherwise)

	Characteristic	40 MHz		56 MHz[1]		Unit
		Min	Max	Min	Max	
10b	CLKOUT to $\overline{\text{RETRY}}$ assertion (when driven by the Memory Controller)		10		10	ns
11	CLKOUT to $\overline{\text{TS}}$, $\overline{\text{BB}}$ negation	7.25	14	5.5	10.5	ns
11a	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{BI}}$ negation (when driven by the Memory Controller)	2	11	2	11	ns
11b	CLKOUT to $\overline{\text{RETRY}}$ negation (when driven by the Memory Controller)	2	11	2	11	ns
12	CLKOUT to $\overline{\text{TS}}$, $\overline{\text{BB}}$ High Z	6.25	20	4.5	16	ns
12a	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{BI}}$ High Z (when driven by the Memory Controller)		15		15	ns
13	CLKOUT to $\overline{\text{TEA}}$ assertion		8.5		8.5	ns
14	CLKOUT to $\overline{\text{TEA}}$ High Z		15		15	ns
15	Input Valid to CLKOUT (Setup Time) $\overline{\text{TA}}$ $\overline{\text{TEA}}$ $\overline{\text{BI}}$[3]	12		8.5		ns
15a	Input Valid to CLKOUT (Setup Time) $\overline{\text{KR}}$ $\overline{\text{CR}}$ $\overline{\text{RETRY}}$	10		7.25		ns
15b	Input Valid to CLKOUT (Setup Time) $\overline{\text{BB}}$ $\overline{\text{BG}}$ $\overline{\text{BR}}$[2]	8		6.5		ns
16	CLKOUT to Signal Invalid (Hold Time) $\overline{\text{TA}}$ $\overline{\text{TEA}}$ $\overline{\text{BI}}$ $\overline{\text{BB}}$ $\overline{\text{BG}}$ $\overline{\text{BR}}$[2, 3]	2		2		ns

Table F-10. Bus Operation Timing (continued)

Note: (V_{DD} = 2.6 V ± 0.1 V, V_{DDH} = 5.0 V ± 0.25 V, $T_A = T_L$ to T_H, 50 pF load unless noted otherwise)

	Characteristic	40 MHz		56 MHz[1]		Unit
		Min	Max	Min	Max	
16a	CLKOUT to Signal Invalid (Hold Time) $\overline{RETRY}$ $\overline{KR}$ $\overline{CR}$	2		2		ns
17	Signal Valid to CLKOUT Rising Edge (Setup Time) D[0:31][4]	6		6		ns
17b	Signal Valid to CLKOUT Rising Edge (Short Setup Time, SST = 1) D[0:31][4]	3		3		
18	CLKOUT Rising Edge to Signal Invalid (Hold Time) D[0:31][4]	2		2		ns
19	CLKOUT Rising Edge to $\overline{CS}$ asserted -GPCM- ACS = 00	7.25	15	6.5	11.5	ns
19a	CLKOUT Falling Edge to $\overline{CS}$ asserted -GPCM- ACS = 10, TRLX = 0 or 1		8		6	ns
19b	CLKOUT Falling Edge to $\overline{CS}$ asserted -GPCM- ACS = 11, TRLX = 0 or 1	6.25	14	5.5	10.5	ns
19c	CLKOUT Falling Edge to $\overline{CS}$ asserted -GPCM- ACS = 11, TRLX = 0, EBDF = 1	6.25	17	6.69	12.69	ns
20	CLKOUT Rising Edge to $\overline{CS}$ negated -GPCM- Read Access or Write access when CSNT = 0 or write access when CSNT = 1 and ACS = 00	1	8	1	7	ns
21	ADDR[8:31] to $\overline{CS}$ asserted -GPCM- ACS = 10, TRLX = 0	0.75		1		ns
21a	ADDR[8:31] to $\overline{CS}$ asserted -GPCM- ACS = 11, TRLX = 0	8		6		ns
22	CLKOUT Rising Edge to $\overline{OE}$, $\overline{WE}$[0:3]/$\overline{BE}$[0:3] asserted	1	8	1	6	ns

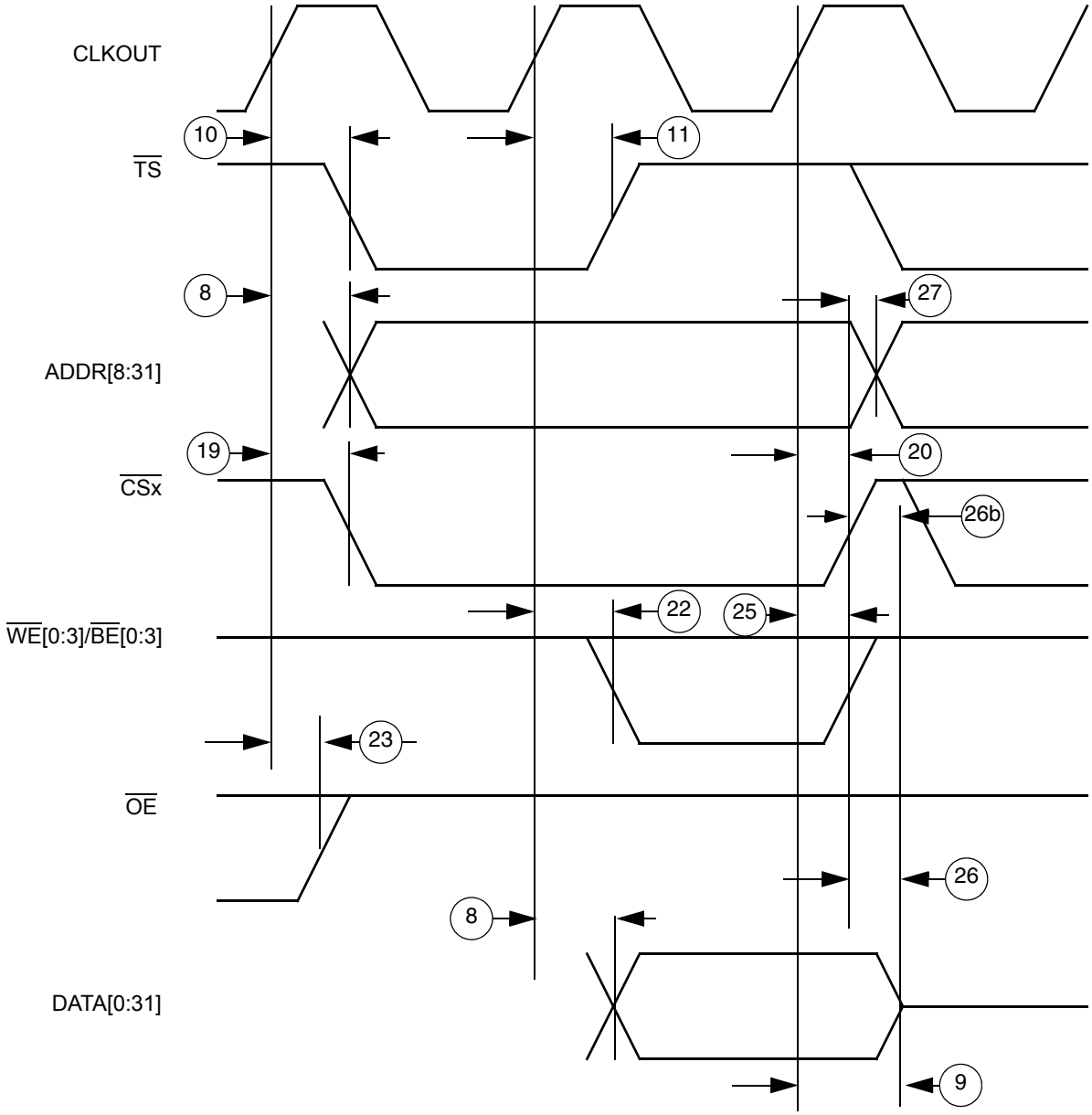


Figure F-22. External Bus Write Timing (GPCM Controlled – TRLX = '0', CSNT = '0')

Table G-28. MPC561/MPC563 Signal Names and Pin Names (continued)

Signal Name	Pin Name	Ball Assignment
VSS	vss	A19, A2, A23, A24, A26, A3, A4, AA1, AA2, AA23, AA24, AA25, AA3, AB1, AB2, AB24, AB25, AB4, AC1, AC21, AC23, AC25, AC3, AC5, AD2, AD22, AD24, AD4, AD5, AE1, AE22, AE23, AE25, AE3, AE4, AE5, AF2, AF22, AF23, AF24, AF26, AF3, AF4, AF6, B1, B19, B23, B25, B3, B4, C1, C2, C24, C26, C4, D1, D2, D23, D25, D26, D3, D5, E2, E24, E25, E26, E3, E4, L11, L12, L13, L14, L15, L16, M11, M12, M13, M14, M15, M16, N11, N12, N13, N14, N15, N16, P11, P12, P13, P14, P15, P16, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16, V25
KAPWR	kapwr	W26
IRAMSTBY	IRAMSTBY	M3
QVDDL	qvddl	AA4
		AB23
		AB3
		AC2
		AC24
		AD1
		AD25
		AD6
		AE26
		AE6
		B26
		C25
		D24
		E23
		F4
USIU Power Supplies		
VDDSYN	vddsyn	Y26
VSSSYN	vsssyn	AB26
QADC64E Power Supplies		
VRH	vrh	C10
VRL	vrl	A10