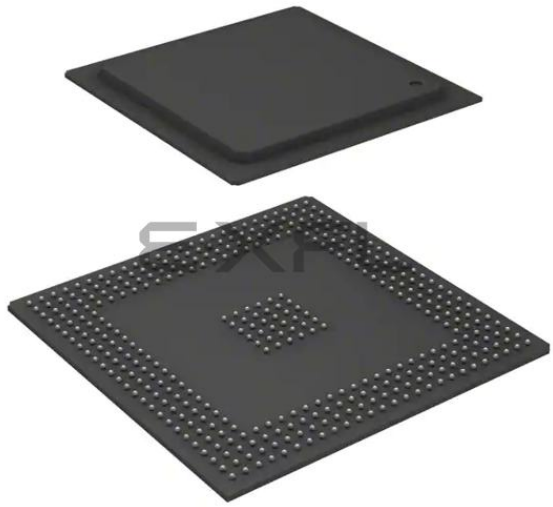

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	PowerPC
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	56
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 2.7V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	388-BBGA
Supplier Device Package	388-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc563cvr40

Contents

1.3.3.5 Queued Serial Multi-Channel Module (QSMCM)

- One queued serial module with one queued SPI and two SCIs (QSMCM)
- QSMCM matches full MPC555 QSMCM functionality
- Queued SPI
  - Provides full-duplex communication port for peripheral expansion or inter-processor communication
  - Up to 32 preprogrammed transfers, reducing overhead
  - Synchronous serial interface with baud rate of up to system clock / 4
  - Four programmable peripheral-selects signals:
  - Supports up to 16 devices with external decoding
  - Supports up to eight devices with internal decoding
  - Special wrap-around mode allows continuous sampling of a serial peripheral for efficient interfacing to serial analog-to-digital (A/D) converters
- SCI
  - UART mode provides NRZ format and half- or full-duplex interface
  - 16 register receive buffers and 16 register transmit buffers on one SCI
  - Advanced error detection and optional parity generation and detection
  - Word-length programmable as eight or nine bits
  - Separate transmitter and receiver enable bits, and double buffering of data
  - Wake-up functions allow the CPU to run uninterrupted until either a true idle line is detected, or a new address byte is received

1.3.3.6 Peripheral Pin Multiplexing (PPM)

- Synchronous serial interface between the microprocessor and an external device
- Four internal parallel data sources can be multiplexed through the PPM
  - TPU3_A: 16 channels
  - TPU3_B: 16 channels
  - MIOS14: 12 PWM channels, four MDA channels
  - Internal GPIO: 16 general-purpose inputs, 16 general-purpose outputs
- Software configurable stream size
- Software configurable clock (TCLK) based on system clock
- Software selectable clock modes (SPI mode and TDM mode)
- Software selectable operation modes
  - Continuous mode
  - Start-transmit-receive (STR) mode
- Software configurable internal modules interconnect (shorting)

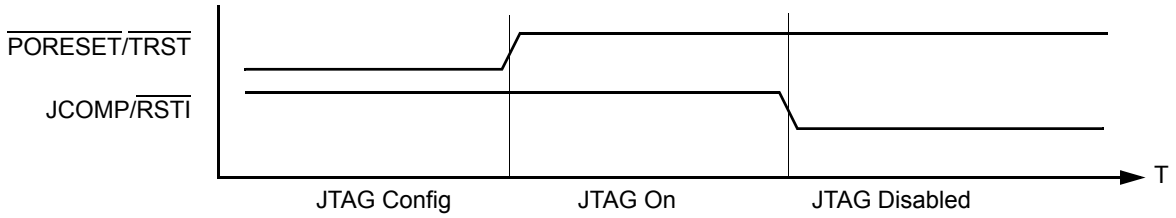

Figure 2-4. Debug Mode Selection (JTAG)

2.5.2 BDM Mode Selection

The MPC561/MPC563 has a 10 pin BDM port. See Figure 2-5 for BDM mode selection.

The BDM mode is entered by the following sequence of events:

- Hold DSCK high at reset negation (SRESET)
- Configure DSDI to select BDM clock mode, within 8 clocks of reset negation

BDM mode is exited by:

- Reset the device by asserting PORESET/TRST or HRESET

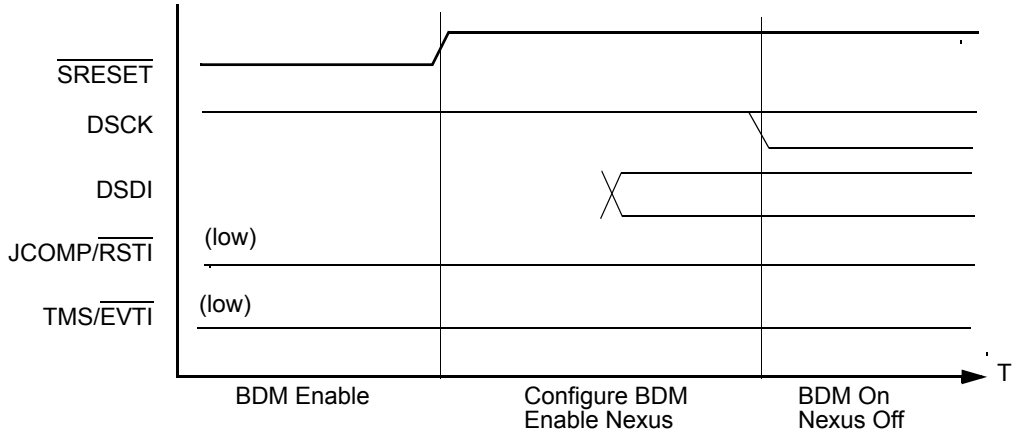

Figure 2-5. Debug Mode Selection (BDM)

2.5.3 Nexus Mode Selection

The READI module signals support the Nexus (IEEE-ISTO 5001-1999) auxiliary port interface for debug. There are two modes available: full port mode and reduced port mode. Reduced port mode allows for a 1 bit input stream and a 2 bit output stream. Full port mode allows for a 2-bit input stream and an 8-bit output stream. If MDI0 is held high when Nexus mode is enabled, full port mode will be used during Nexus debug. If MDI0 is held low when Nexus mode is enabled, reduced port mode will be used. See Figure 2-6 for Nexus mode selection.

The Nexus interface is entered by the following sequence of events:

- Hold JCOMP/RSTI low while negating PORESET/TRST
- Hold TMS/EVTI low to enable Nexus mode and configure TDI/DSDI/MDI0 for full or reduced port mode. Both of these should be done at least 4 clocks before driving JCOMP/RSTI high

Table 4-1. Exception Addresses Mapping (continued)

Name of Exception	Original Address Issues by Core	Mapped Address by Exception Table Relocation Logic
Implementation Dependent Instruction Storage Protection Error	0xFFF0 1300	Page_Offset+0x098
Implementation Dependent Data Storage Protection Error	0xFFF0 1400	Page_Offset+0x0A0
Implementation Dependent Data Breakpoint	0xFFF0 1C00	Page_Offset+0x0E0
Implementation Dependent Instruction Breakpoint	0x0FFF 1D00	Page_Offset+0x0E8
Implementation Dependent Maskable External Breakpoint	0xFFF0 1E00	Page_Offset+0x0F0
Non-Maskable External Breakpoint	0xFFF0 1F00	Page_Offset+0x0F8

1 Refer to Table 4-2.

2 0x500 is remapped if the EEIR feature is enabled. See Section 4.3.2, “Enhanced External Interrupt Relocation (EEIR).”

Table 4-2. Exception Relocation Page Offset

BBCMCR(OERC[0:1])		Page Offset	Comments
0	0	0x0 + ISB offset[1]	0
0	1	0x1 0000 + ISB offset	64 Kbytes[2]
1	0	0x8 0000 + ISB offset	512 Kbytes
1	1	0x3F E000 + ISB offset	L-bus (CALRAM) Address

1 ISB offset is equal 4M * ISB (0x400000 * ISB), where ISB is value of bit field in USIU IMMR register.

2 This offset is different from the MPC555.

4.3.2 Enhanced External Interrupt Relocation (EEIR)

The BBC also supports the enhanced external interrupt model of the MPC561/MPC563 which allows the removal of the interrupt requesting a source detection stage from the interrupt routine. The interrupt controller provides the interrupt vector to the BBC together with an interrupt request to the RCPU. When the RCPU acknowledges an interrupt request, it issues an external interrupt vector to the BBC. The BBC logic detects this address and replaces it with another address corresponding to the interrupt controller vector, which is defined by the highest priority interrupt request from a peripherial module or external interrupt request pin. See Figure 4-3.

The external interrupt relocation table should be placed at the physical address defined in the external interrupt relocation table base address register. See Section 4.6.2.5, “External Interrupt Relocation Table

Table 5-1. USIU Address Map (continued)

Address	Register
0x2F C0FC–0x2F C0FF	Reserved
Memory Controller Registers	
0x2F C100	Base Register 0 (BR0) See Table 10-8 for bit descriptions.
0x2F C104	Option Register 0 (OR0) See Table 10-10 for bit descriptions.
0x2F C108	Base Register 1 (BR1) See Table 10-8 for bit descriptions.
0x2F C10C	Option Register 1 (OR1) See Table 10-10 for bit descriptions.
0x2F C110	Base Register 2 (BR2) See Table 10-8 for bit descriptions.
0x2F C114	Option Register 2 (OR2) See Table 10-10 for bit descriptions.
0x2F C118	Base Register 3 (BR3) See Table 10-8 for bit descriptions.
0x2F C11C	Option Register 3 (OR3) See Table 10-10 for bit descriptions.
0x2F C120–0x2F C13C	Reserved
0x2F C140	Dual-Mapping Base Register (DMBR) See Table 10-11 for bit descriptions.
0x2F C144	Dual-Mapping Option Register (DMOR) See Table 10-12 for bit descriptions.
0x2F C148–0x2F C174	Reserved
0x2F C178[1]	Memory Status (MSTAT) See Table 10-7 for bit descriptions.
0x2F C17A–0x2F C1FC	Reserved
System Integration Timers	
0x2F C200	Time Base Status and Control (TBSCR) See Table 6-18 for bit descriptions.
0x2F C204	Time Base Reference 0 (TBREF0) See Section 6.2.2.4.3, “Time Base Reference Registers (TBREF0 and TBREF1),” for bit descriptions.
0x2F C208	Time Base Reference 1 (TBREF1) See Section 6.2.2.4.3, “Time Base Reference Registers (TBREF0 and TBREF1),” for bit descriptions.
0x2F C20C–0x2F C21C	Reserved

Table 6-17. TESR Bit Descriptions (continued)

Bits	Name	Description
20:25	—	Reserved
26	DEXT	Data external transfer error acknowledge. This bit is set if the cycle was terminated by an externally generated $\overline{\text{TEA}}$ signal when a data load or store is requested by an internal master.
27	DBM	Data transfer monitor time out. This bit is set if the cycle was terminated by a bus monitor time-out when a data load or store is requested by an internal master.
28:31	—	Reserved

6.2.2.4 System Timer Registers

The following sections describe registers associated with the system timers. These facilities are powered by the KAPWR and can preserve their value when the main power supply is off. Refer to Section 8.2.3, "Pre-Divider," for details on the required actions needed in order to guarantee this data retention.

A list of KAPWR registers affected by the key/lock mechanism is found in Table 8-8.

6.2.2.4.1 Decrementer Register (DEC)

The 32-bit decrementer register is defined by the PowerPC architecture. The values stored in this register are used by a down counter to cause decrementer exceptions. The decrementer causes an exception whenever bit zero changes from a logic zero to a logic one. A read of this register always returns the current count value from the down counter.

Contents of this register can be read or written to by the mfspr or the mtspr instruction. The decrementer register is reset by $\overline{\text{PORESET}}$. $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ do not affect this register. The decrementer is powered by standby power and can continue to count when standby power is applied.

Decrementer counts down the time base clock and the counting is enabled by TBE bit in TBCSR register Section 6.2.2.4.4, "Time Base Control and Status Register (TBSCR)."

	MSB 0	LSB 31
Field	DECREMENTING COUNTER	
PORESET	0000_0000_0000_0000_0000_0000_0000_0000	
$\overline{\text{HRESET}}$ $\overline{\text{SRESET}}$	Unaffected	
Addr	SPR 22	

Figure 6-29. Decrementer Register (DEC)

Refer to Section 3.9.5, "Decrementer Register (DEC)" for more information on this register.

6.2.2.4.2 Time Base SPRs (TB)

The TB is a 64-bit register containing a 64-bit integer that is incremented periodically. There is no automatic initialization of the TB; the system software must perform this initialization. The contents of the

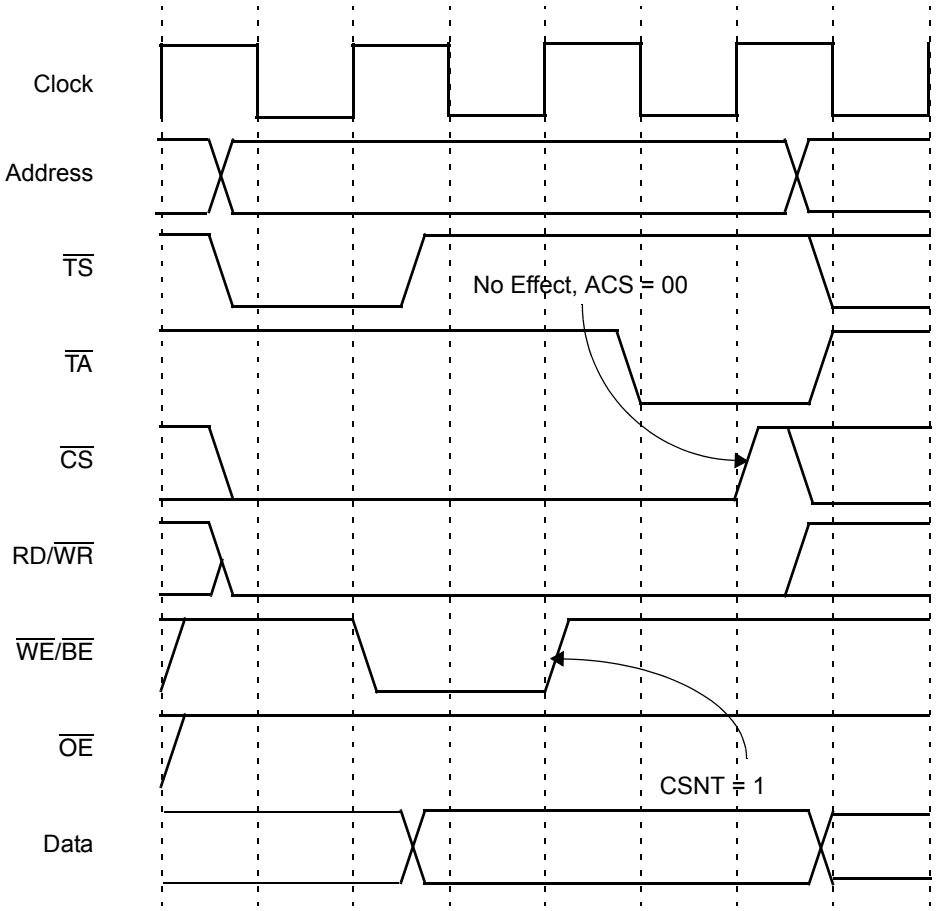

Figure 10-14. Relaxed Timing — Write Access (ACS = 00, SCY = 0, CSNT = 1, TRLX = 1

10.3.4 Extended Hold Time on Read Accesses

For devices that require a long disconnection time from the data bus on read accesses, the bit EHTR in the corresponding OR register can be set. In this case any MPC561/MPC563 access to the external bus following a read access to the referred memory bank is delayed by one clock cycle unless it is a read access to the same bank. Figure 10-15 through Figure 10-18 show the effect of the EHTR bit on memory controller timing.

Figure 10-15 shows a write access following a read access. Because EHTR = 0, no extra clock cycle is inserted between memory cycles.

Table 11-10. L2U_GRA Bit Descriptions (continued)

Bits	Name	Description
3	ENR3	Enable attribute for region 3 0 Region attribute is off 1 Region attribute is on
4:19	—	Reserved
20:21	PP	Protection bits 00 No supervisor access, no user access 01 Supervisor read/write access, no user access 10 Supervisor read/write access, user read-only access 11 Supervisor read/write access, user read/write access
22:24	—	Reserved
25	G	Guarded attribute 0 Not guarded from speculative accesses 1 Guarded from speculative accesses
26:31	—	Reserved

The AltRef signal may be selected through the CCW as the high reference for a conversion. This allows for the ability to “zoom” in on a portion of the convertible range with the full 10 bits. Refer to Table 14-19.

No A/D converter can be more accurate than its analog reference. Any noise in the reference can result in at least that much error in a conversion. The reference for the QADC64E, supplied by signals V_{RH}, AltRef, and V_{RL}, should be low-pass filtered from its source to obtain a noise-free, clean signal. In many cases, simple capacitive bypassing may sufficed. In extreme cases, inductors or ferrite beads may be necessary if noise or RF energy is present. Series resistance is not advisable since there is an effective DC current requirement from the reference voltage by the internal resistor string in the RC DAC array. External resistance may introduce error in this architecture under certain conditions. Any series devices in the filter network should contain a minimum amount of DC resistance.

14.6.5 Analog Input Signals

Analog inputs should have low AC impedance at the signals. Low AC impedance can be realized by placing a capacitor with good high frequency characteristics at the input signal of the part. Ideally, that capacitor should be as large as possible (within the practical range of capacitors that still have good high frequency characteristics). This capacitor has two effects:

- It helps attenuate any noise that may exist on the input.
- It sources charge during the sample period when the analog signal source is a high-impedance source.

Series resistance can be used with the capacitor on an input signal to implement a simple RC filter. The maximum level of filtering at the input signals is application dependent and is based on the bandpass characteristics required to accurately track the dynamic characteristics of an input. Simple RC filtering at the signal may be limited by the source impedance of the transducer or circuit supplying the analog signal to be measured. Refer to Section 14.6.5.3, “Error Resulting from Leakage” for more information. In some cases, the size of the capacitor at the signal may be very small.

Figure 14-50 is a simplified model of an input channel. Refer to this model in the following discussion of the interaction between the external circuitry and the circuitry inside the QADC64E.

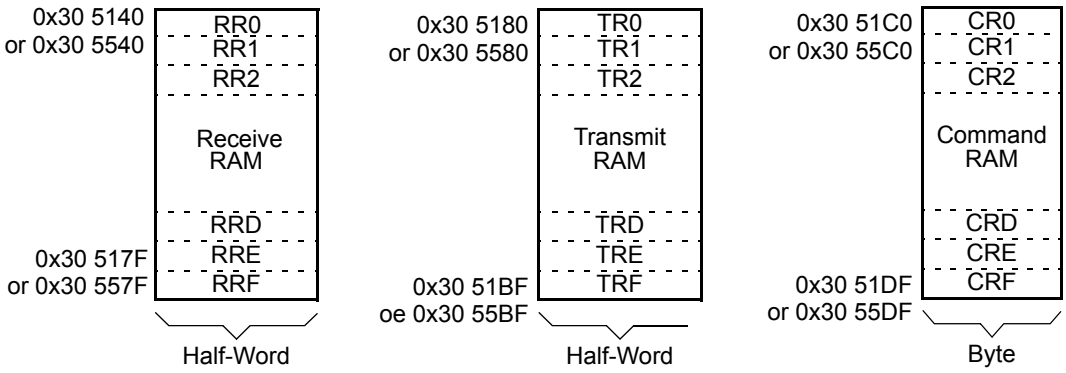

Figure 15-16. QSPI RAM

15.6.2.1 Receive RAM

Data received by the QSPI is stored in this segment, to be read by the CPU. Data stored in the receive RAM is right-justified, (i.e., the least significant bit is always in the right-most bit position within the word regardless of the serial transfer length). Unused bits in a receive queue entry are set to zero by the QSPI upon completion of the individual queue entry. The CPU can access the data using byte, half-word, or word addressing.

The CPTQP value in SPSR shows which queue entries have been executed. The CPU uses this information to determine which locations in receive RAM contain valid data before reading them.

15.6.2.2 Transmit RAM

Data that is to be transmitted by the QSPI is stored in this segment. The CPU normally writes one word of data into this segment for each queue command to be executed. If the corresponding peripheral, such as a serial input port, is used solely to input data, then this segment does not need to be initialized.

Data must be written to transmit RAM in a right-justified format. The QSPI cannot modify information in the transmit RAM. The QSPI copies the information to its data serializer for transmission. Information remains in transmit RAM until overwritten.

15.6.2.3 Command RAM

Command RAM is used by the QSPI in master mode. The CPU writes one byte of control information to this segment for each QSPI command to be executed. The QSPI cannot modify information in command RAM.

Command RAM consists of 32 bytes. Each byte is divided into two fields. The peripheral chip-select field, enables peripherals for transfer. The command control field provides transfer options.

A maximum of 32 commands can be in the queue. These bytes are assigned an address from 0x00 to 0x1F. Queue execution by the QSPI proceeds from the address in NEWQP through the address in ENDQP. (Both of these fields are in SPCR2.)

Table 16-13. CANCTRL0 Bit Descriptions

Bits	Name	Description
0	BOFFMSK	Bus off interrupt mask. The BOFF MASK bit provides a mask for the bus off interrupt. 0 Bus off interrupt disabled 1 Bus off interrupt enabled
1	ERRMSK	Error interrupt mask. The ERRMSK bit provides a mask for the error interrupt. 0 Error interrupt disabled 1 Error interrupt enabled
2:3	—	Reserved
4:5	RXMODE	Receive signal configuration control. These bits control the configuration of the CNRX0 signals. Refer to Table 16-14.
6:7	TXMODE	Transmit signal configuration control. This bit field controls the configuration of the CNTX0 signals. Refer to Table 16-15.
8:15	CANCTRL1	See Table 16-16 and Section 16.7.5, “Control Register 1 (CANCTRL1).”

Table 16-14. Rx MODE[1:0] Configuration

Signal	RX1	RX0	Receive Signal Configuration
CNRX0	X	0	0 CNRX0 signal is interpreted as a dominant bit 1 CNRX0 signal is interpreted as a recessive bit
	X	1	0 CNRX0 signal is interpreted as a recessive bit 1 CNRX0 signal is interpreted as a dominant bit

Table 16-15. Transmit Signal Configuration

TXMODE[1:0]	TransmitSignal Configuration
00	Full CMOS[1]; positive polarity (CNTX0 = 0 is a dominant level)
01	Full CMOS[1]; negative polarity (CNTX0 = 1 is a dominant level)
1X	Open drain[2]; positive polarity

1 Full CMOS drive indicates that both dominant and recessive levels are driven by the chip.

2 Open drain drive indicates that only a dominant level is driven by the chip. During a recessive level, the CNTX0 signal is disabled (three stated), and the electrical level is achieved by external pull-up/pull-down devices. The assertion of both Tx mode bits causes the polarity inversion to be cancelled (open drain mode forces the polarity to be positive).

16.7.5 Control Register 1 (CANCTRL1)

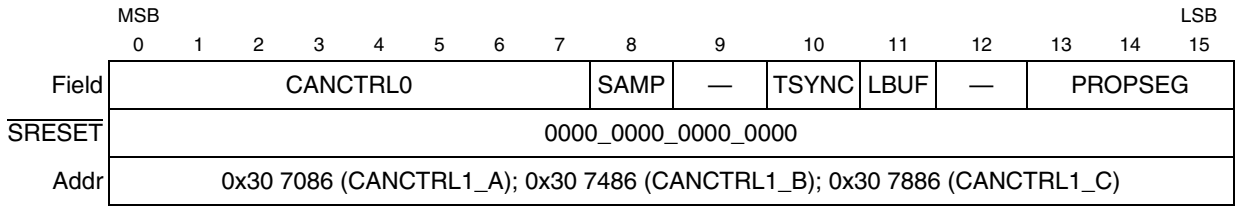

Figure 16-12. Control Register 1 (CANCTRL1)

Table 17-1. MIOS14 Configuration Description (continued)

Sub-Module Type	Block No.	Connected to:				MIRSM No.	MIRSM Bit Position	Base Address Offset	Signal Function	Input Signal Name	Output Signal Name	Alternate Signal Name
		CBA	CBB	CBC	CBD							
		BSL0=0 BSL1=0	BSL0=1 BSL1=0	BSL0=0 BSL1=1	BSL0=1 BSL1=1							
									Load In	MPWM 19		MDO7
Reserved	25-26											
MDASM	27	CB6	CB22	CB23	CB24	1	11	0x30 60D8	Channel I/O	MDA27	MDA27	
MDASM	28	CB6	CB22	CB23	CB24	1	12	0x30 60E0	Channel I/O	MDA28	MDA28	
MDASM	29	CB6	CB22	CB7	CB8	1	13	0x30 60E8	Channel I/O	MDA29	MDA29	
MDASM	30	CB6	CB22	CB7	CB8	1	14	0x30 60F0	Channel I/O	MDA30	MDA30	
MDASM	31	CB6	CB22	CB7	CB8	1	15	0x30 60F8	Channel I/O	MDA31	MDA31	
MPIOSM	32							0x30 6100	GPIO	MPIO32B0	MPIO32B0	VF0 /MDO1
									GPIO	MPIO32B1	MPIO32B1	VF1 /MCKO
									GPIO	MPIO32B2	MPIO32B2	$\overline{\text{VF2}}$ /MSEI
									GPIO	MPIO32B3	MPIO32B3	VFLS0 /$\overline{\text{MSEO}}$
									GPIO	MPIO32B4	MPIO32B4	VFLS1
									GPIO	MPIO32B5	MPIO32B5	MDO5
									GPIO	MPIO32B6	MPIO32B6	MPWM4/ MDO6
									GPIO	MPIO32B7	MPIO32B7	MPWM5
									GPIO	MPIO32B8	MPIO32B8	MPWM20
									GPIO	MPIO32B9	MPIO32B9	MPWM21
									GPIO	MPIO32B10	MPIO32B10	PPM_ TSYNC
									GPIO	MPIO32B11	MPIO32B11	C_CNRX0

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	PIN	WOR	FREN	—	EDPOL	FORCA	FORCB	—		BSL		—	MODE			
$\overline{\text{SRESET}}$	—	000_0000_0000_0000														
Addr	0x30 605E, 0x30 6066, 0x30 606E, 0x30 6076, 0x30 607E, 0x30 60DE, 0x30 60E6, 0x30 60EE, 0x30 60F6, 0x30 60FE															

Figure 17-24. MDASM Status/Control Register (MDASMSCR)

Table 17-21. MDASMSCR Bit Descriptions

Bits	Name	Description
0	PIN	Pin Input Status — The pin input status bit reflects the status of the corresponding bit.
1	WOR	Wired-OR bit — In the DIS, IPWM, IPM and IC modes, the WOR bit is not used; reading this bit returns the value that was previously written. In the OCB, OCAB and OPWM modes, the WOR bit selects whether the output buffer is configured for open-drain or totem pole operation. When open-drain mode is selected, the EDPOL bit is not used; writing to EDPOL will have no effect on the output voltage. 1 Output buffer is open-drain. 0 Output buffer is totem pole. The WOR bit is cleared by reset.
2	FREN	Freeze enable bit — This active high read/write control bit enables the MDASM to recognize the MIOB freeze signal. 1 = The MDASM is frozen if the MIOB freeze line is active. 0 = The MDASM is not frozen even if the MIOB freeze line is active. The FREN is cleared by reset.
3	—	Reserved
4	EDPOL	Polarity bit — In the DIS mode, this bit is not used; reading it returns the last value written. In the IPWM mode, this bit is used to select the capture edge sensitivity of channels A and B. 1 Channel A captures on a falling edge. Channel B captures on a rising edge. 0 Channel A captures on a rising edge. Channel B captures on a falling edge. In the IPM and IC modes, the EDPOL bit is used to select the input capture edge sensitivity of channel A. 1 Channel A captures on a falling edge. 0 Channel A captures on a rising edge. In the OCB, OCAB and OPWM modes, the EDPOL bit is used to select the voltage level on the output signal. If open-drain mode is selected via the WOR bit, the EDPOL bit is disabled and writing to it will have no effect on the output voltage. 1 The complement of the output flip-flop logic level appears on the output signal: a match on channel A resets the output signal; a match on channel B sets the output signal. 0 The output flip-flop logic level appears on the output signal: a match on channel A sets the output signal, a match on channel B resets the output signal. The EDPOL bit is cleared by reset.
5	FORCA	Force A bit — In the OCB, OCAB and OPWM modes, the FORCA bit allows the software to force the output flip-flop to behave as if a successful comparison had occurred on channel A (except that the FLAG line is not activated). Writing a one to FORCA sets the output flip-flop; writing a zero to it has no effect. In the DIS, IPWM, IPM and IC modes, the FORCA bit is not used and writing to it has no effect. FORCA is cleared by reset and is always read as zero. Writing a one to both FORCA and FORCB simultaneously resets the output flip-flop.

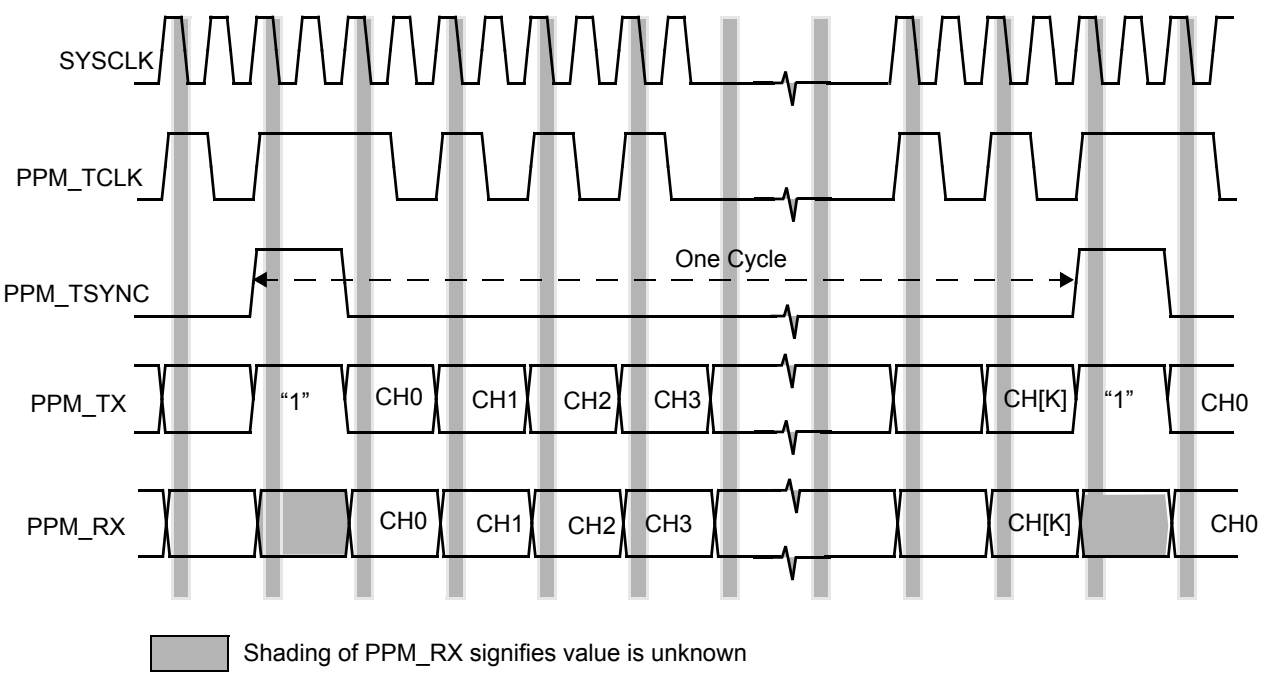

Figure 18-6. One Transmit and Receive Cycle in SPI Mode

18.3.1.3 PPM Control Settings

As data is transferred through the PPM module it must be sampled at a rate which guarantees its validity. This sample rate is a multiple of PPM_TCLK and is defined by the SAMP[0:2] field of the PPMPCR register. For transmit operations, the sample rate is the rate at which TX_DATA receives data from the internal modules. For receive operations, it is the rate at which the internal modules read RX_SHIFTER. The register RX_DATA is updated from RX_SHIFTER on completed receive (PPM_TSYNC) cycles.

19.4.10 Channel Interrupt Status Register (CISR)

The channel interrupt status register (CISR) contains one interrupt status flag per channel. Time functions specify via microcode when an interrupt flag is set. Setting a flag causes the TPU3 to make an interrupt service request if the corresponding CIER bit is set. To clear a status flag, read CISR, then write a zero to the appropriate bit.

NOTE

CISR is the only TPU3 register that can be accessed on a byte basis.

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 9	CH 8	CH 7	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0
$\overline{\text{SRESET}}$	0000_0000_0000_0000															
Addr	0x30 4020 (TPU_A), 0x30 4420 (TPU_B)															

Figure 19-20. CISR — Channel Interrupt Status Register

Table 19-17. CISR Bit Descriptions

Bits	Name	Description
0:15	CH[15:0]	Channel interrupt status 0 Channel interrupt not asserted 1 Channel interrupt asserted

19.4.11 TPU3 Module Configuration Register 2 (TPUMCR2)

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	—							DIV2	SOFTRST	ETBANK		FPSCK			T2CF	DTPU
$\overline{\text{SRESET}}$	0000_0000_0000_0000															
Addr	0x30 4028 (TPU_A), 0x30 4428 (TPU_B)															

Figure 19-21. TPUMCR2 — TPU Module Configuration Register 2

Table 19-18. TPUMCR2 Bit Descriptions

Bits	Name	Description
0:6	—	Reserved
7	DIV2	Divide by 2 control. When asserted, the DIV2 bit, along with the TCR1P bit and the PSCK bit in the TPUMCR, determines the rate of the TCR1 counter in the TPU3. If set, the TCR1 counter increments at a rate of two system clocks. If negated, TCR1 increments at the rate determined by control bits in the TCR1P and PSCK fields. 0 TCR1 increments at rate determined by control bits in the TCR1P and PSCK fields of the TPUMCR register 1 Causes TCR1 counter to increment at a rate of the system clock divided by two

— The DPTRAM array acts as a microcode storage for the TPU3 module. This provides a means of executing TPU3 code out of DPTRAM instead of TPU3 ROM.

- Includes built in check logic which scans the array contents and calculates the DPTRAM signature
- IMB3 bus interface
- Two TPU3 interface units
- Byte, half-word, or word accessible

20.2 DPTRAM Configuration Block Diagram

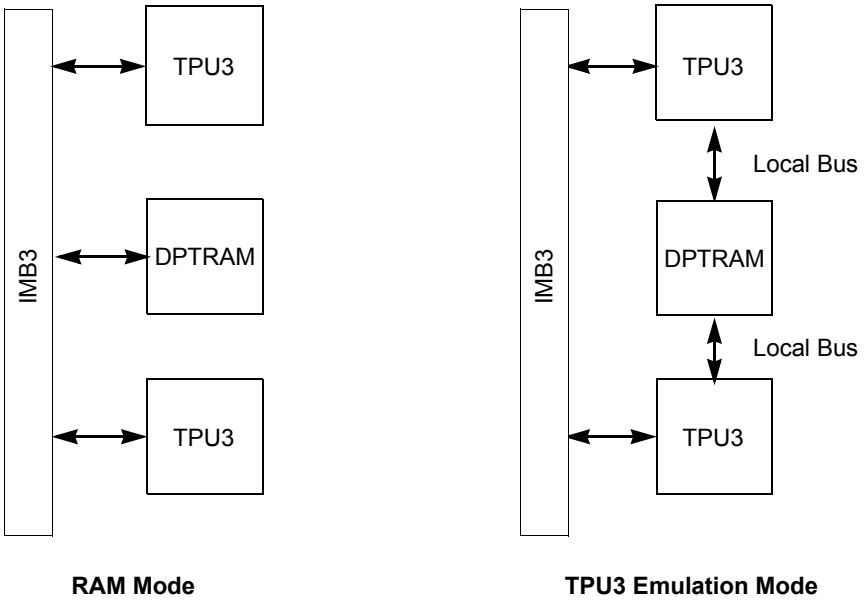

Figure 20-1. DPTRAM Configuration

20.3 Programming Model

The DPTRAM module consists of two separately addressable sections. The first is a set of memory-mapped control and status registers used for configuration (DPTMCR, RAMBAR, MISRH, MISRL, MISCNT) and testing (DPTTCR) of the DPTRAM array. The second section is the array itself.

All DPTRAM module control and status registers are located in supervisor data space. User read or write attempts will result in a bus error.

When the TPU3 is using the RAM array for microcode control storage, none of these control registers has any effect on the operation of the RAM array.

All addresses within the 64-byte control block will respond when accessed properly. Unimplemented addresses will return zeros for read accesses. Likewise, unimplemented bits within registers will return zero when read and will not be affected by write operations.

Table 20-1 shows the DPTRAM control and status registers. The addresses shown are offsets from the internal system base address (see Section 6.2.2.1.2, “Internal Memory Map Register (IMMR)”). Refer to Figure 1-3 to locate the DPTRAM control block in the MPC561/MPC563 address map.

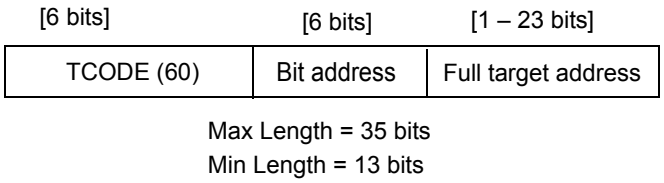

Figure 24-28. Direct Branch Synchronization Message Format with Compressed Code (PTSM = 0)

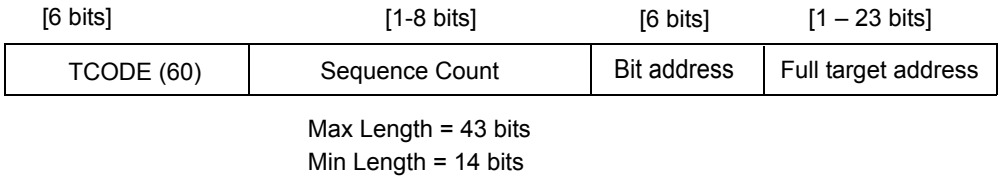

Figure 24-29. Direct Branch Synchronization Message Format with Compressed Code (PTSM = 1)

24.8.2.4.4 Indirect Branch Synchronization Message with Compressed Code

For compressed code support, six additional bits indicate the starting bit address within the word of the compressed instruction. The program trace indirect branch synchronization with compressed code message has the following formats depending on the setting of MC[PTSM]:

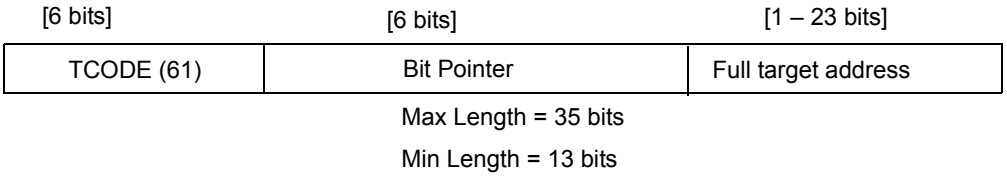

Figure 24-30. Indirect Branch Synchronization Message Format with Compressed Code (PTSM - 0)

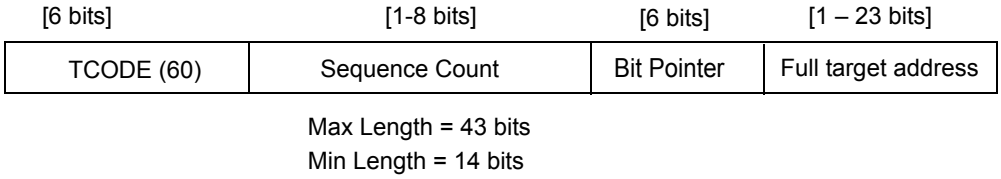

Figure 24-31. Indirect Branch Synchronization Message Format with Compressed Code (PTSM = 1)

Bit pointer format is shown in Figure 24-22 and bit address format is described in Table 24-26.

24.8.2.4.5 Resource Full Message

When more than 256 instructions have run without a branch being taken a program trace resource full message will be generated that indicates the maximum I-CNT value has been reached. The I-CNT field has a maximum width of 8 bits.

If the $\overline{\text{PORESET}}$ or $\overline{\text{HRESET}}$ signal is not asserted before this condition, there is a possibility of disturbing the programmed state of the flash. In addition, the state of the pads are indeterminant until $\overline{\text{PORESET}}$ or $\overline{\text{HRESET}}$ propagates through the device to initialize all circuitry.

F.9.2 Keep-Alive RAM

$\overline{\text{PORESET}}$ or $\overline{\text{HRESET}}$ must be asserted during power-down prior to any supply dropping out of specified operating conditions.

An additional constraint is placed on $\overline{\text{PORESET}}$ assertion since it is an asynchronous input. To assure that the assertion of $\overline{\text{PORESET}}$ does not potentially cause stores to keep-alive RAM to be corrupted (store single or store multiple) or non-coherent (store multiple), either of the following solutions is recommended:

- Assert $\overline{\text{HRESET}}$ at least 0.5 µs prior to when $\overline{\text{PORESET}}$ is asserted.
- Assert $\overline{\text{IRQ}}$0 (non-maskable interrupt) at least 0.5 µs prior to when $\overline{\text{PORESET}}$ is asserted. The service routine for $\overline{\text{IRQ}}$0 should not perform any writes to keep-alive RAM.

The amount of delay that should be added to $\overline{\text{PORESET}}$ assertion is dependent upon the frequency of operation and the maximum number of store multiples executed that are required to be coherent. If store multiples of more than 28 registers are needed and if the frequency of operation is lower that 56 MHz, the delay added to $\overline{\text{PORESET}}$ assertion will need to be greater than 0.5 µs. In addition, if KAPWR features are being used, $\overline{\text{PORESET}}$ should not be driven low while the V_{DDH} and V_{DDL} supplies are off.

F.10 AC Timing

Figure F-9 displays generic examples of MPC561/MPC563 timing. Specific timing diagrams are shown in Figure F-10 through Figure F-36.

Table F-28. MPC561/MPC563 Signal Names and Pin Names (continued)

Signal Name	Pin Name	Ball Assignment
IRQ1/RSV/SGPIOC1	irq1_b_rsv_b_sgpioc1	P4
IRQ2/CR/SGPIOC2/MTS[1]	irq2_b_cr_b_sgpioc2_mts_b	P2
IRQ3/KR/RETRY/SGPIOC	irq3_b_kr_b_retry_b_sgpioc3	N1
IRQ4/AT2/SGPIOC4	irq4_b_at2_sgpioc4	P1
IRQ5/SGPIOC5/MODCK1	irq5_b_sgpioc5_modck1	AD21
IRQ[6:7]/MODCK[2:3]	irq6_b_modck2	AE21
	irq7_b_modck3	Y24
PULL_SEL (input only)	pull_sel	R26
TSIZ[0:1]	tsiz0	V4
	tsiz1	W1
RD/WR	rd_wr _b	V1
BURST	burst	Y1
BDIP	bdip_b	W4
TS	ts_b	W2
TA	ta_b	W3
TEA	tea_b	V3
RSTCONF/TEXP	rstconf_b_texp	Y25
OE	oe_b	V2
BI/STS	bi_b_sts_b	Y2
CS[0:3]	cs0_b	U1
	cs1_b	U2
	cs2_b	U3
	cs3_b	U4
WE[0:3]/BE[0:3]/AT[0:3]	we0_b_we0_b_a0	T1
	we0_b_be1_b_at1	T2
	we0_b_be2_b_at2	T3
	we0_b_be3_b_at3	T4
PORESET/TRST	poreset_b_trst_b	W25
HRESET	hreset_b	W23
SRESET	sreset_b	W24
SGPIOC6/FRZ/PTR	sgpioc6_frz_ptr_b	N4
SGPIOC7/IRQOUT/LWP0	sgpioc7_irqout_b_lwp0	R1
BG/VF0/LWP1	bg_b_vf0_lwp1	R3

Table G-28. MPC561/MPC563 Signal Names and Pin Names (continued)

Signal Name	Pin Name	Ball Assignment
VSS	vss	A19, A2, A23, A24, A26, A3, A4, AA1, AA2, AA23, AA24, AA25, AA3, AB1, AB2, AB24, AB25, AB4, AC1, AC21, AC23, AC25, AC3, AC5, AD2, AD22, AD24, AD4, AD5, AE1, AE22, AE23, AE25, AE3, AE4, AE5, AF2, AF22, AF23, AF24, AF26, AF3, AF4, AF6, B1, B19, B23, B25, B3, B4, C1, C2, C24, C26, C4, D1, D2, D23, D25, D26, D3, D5, E2, E24, E25, E26, E3, E4, L11, L12, L13, L14, L15, L16, M11, M12, M13, M14, M15, M16, N11, N12, N13, N14, N15, N16, P11, P12, P13, P14, P15, P16, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16, V25
KAPWR	kapwr	W26
IRAMSTBY	IRAMSTBY	M3
QVDDL	qvddl	AA4
		AB23
		AB3
		AC2
		AC24
		AD1
		AD25
		AD6
		AE26
		AE6
		B26
		C25
		D24
		E23
		F4
USIU Power Supplies		
VDDSYN	vddsyn	Y26
VSSSYN	vsssyn	AB26
QADC64E Power Supplies		
VRH	vrh	C10
VRL	vrl	A10