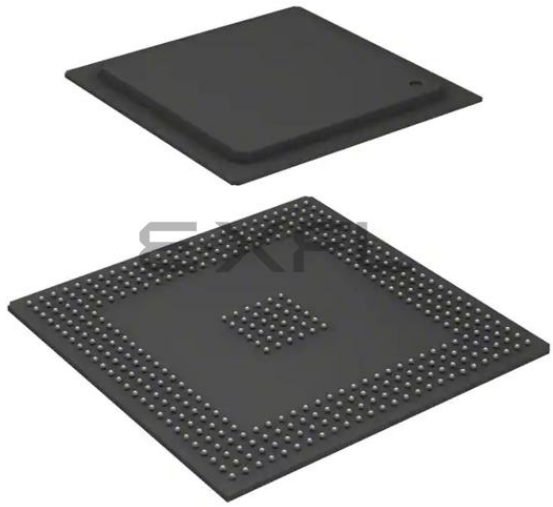

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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
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Package / Case	388-BBGA
Supplier Device Package	388-PBGA (27x27)
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Figures

Tables

Table 2-14. MPC561/MPC563 Signal Reset State (continued)

Signal List[1]	Voltage	Slew Rate Controlled Option?	Drive Load (pF)[2]	Reset State	Hysteresis Enabled?	Function After HRESET, PORESET/TRST
A_AN1 /	5 V	Yes	NA	PU5 when driver not enabled or until PULL_DIS2 is set	No	A_AN1
A_ANx /	5 V	Yes	NA		No	
A_PQB1	5 V	Yes	50 ; 50 [5]		Yes	
A_AN2 /	5 V	Yes	NA	PU5 when driver not enabled or until PULL_DIS2 is set	No	A_AN2
A_ANy /	5 V	Yes	NA		No	
A_PQB2	5 V	Yes	50 ; 50 [5]		Yes	
A_AN3 /	5 V	Yes	NA	PU5 when driver not enabled or until PULL_DIS2 is set	No	A_AN3
A_ANz /	5 V	Yes	NA		No	
A_PQB3	5 V	Yes	50 ; 50 [5]		Yes	
A_AN[48:51]/	5 V	Yes	NA	PU5 when driver not enabled or until PULL_DIS2 is set	No	A_AN[48:51]
A_PQB[4:7]	5 V	Yes	50 ; 50 [5]		Yes	
A_AN[52:54] /	5 V	Yes	NA	PU5 when driver not enabled or until PULL_DIS2 is set	No	A_AN[52:54]
A_MA[0:2] /	5 V	Yes	NA		Yes	
A_PQA[0:2]	5 V	Yes	50 ; 50 [5]		Yes	
A_AN[55:59]/	5 V	Yes	NA	PU5 when driver not enabled or until PULL_DIS2 is set	No	A_AN[55:59]
A_PQA[3:7]	5 V	Yes	50 ; 50 [5]		Yes	
B_AN0 /	5 V	Yes	NA	PU5 when driver not enabled or until PULL_DIS2 is set	No	B_AN0
B_ANw /	5 V	Yes	NA		No	
B_PQB0	5 V	Yes	50 ; 50 [5]		Yes	
B_AN1 /	5 V	Yes	NA	PU5 when driver not enabled or until PULL_DIS2 is set	No	B_AN1
B_ANx /	5 V	Yes	NA		No	
B_PQB1	5 V	Yes	50 ; 50 [5]		Yes	
B_AN2 /	5 V	Yes	NA	PU5 when driver not enabled or until PULL_DIS2 is set	No	B_AN2
B_ANy /	5 V	Yes	NA		No	
B_PQB2	5 V	Yes	50 ; 50 [5]		Yes	

4.6.2.5 External Interrupt Relocation Table Base Address Register (EIBADR)

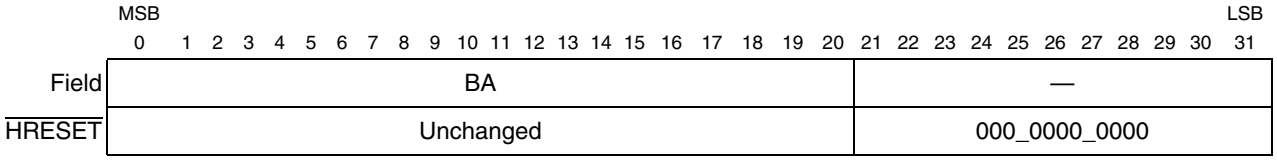


Figure 4-11. External Interrupt Relocation Table Base Address Register (EIBADR)

Table 4-9. EIBADR External Interrupt Relocation Table Base Address Register Bit Descriptions

Bits	Name	Description
0:20	BA	External Interrupt Relocation Table Base Address bits [0:20]
21:31	—	Reserved. EIBADR must be set on a 4K page boundary.

4.6.3 Decompressor Class Configuration Registers

See Section A.4, “Decompressor Class Configuration Registers (DCCR0-15)” for the registers of the ICDU.

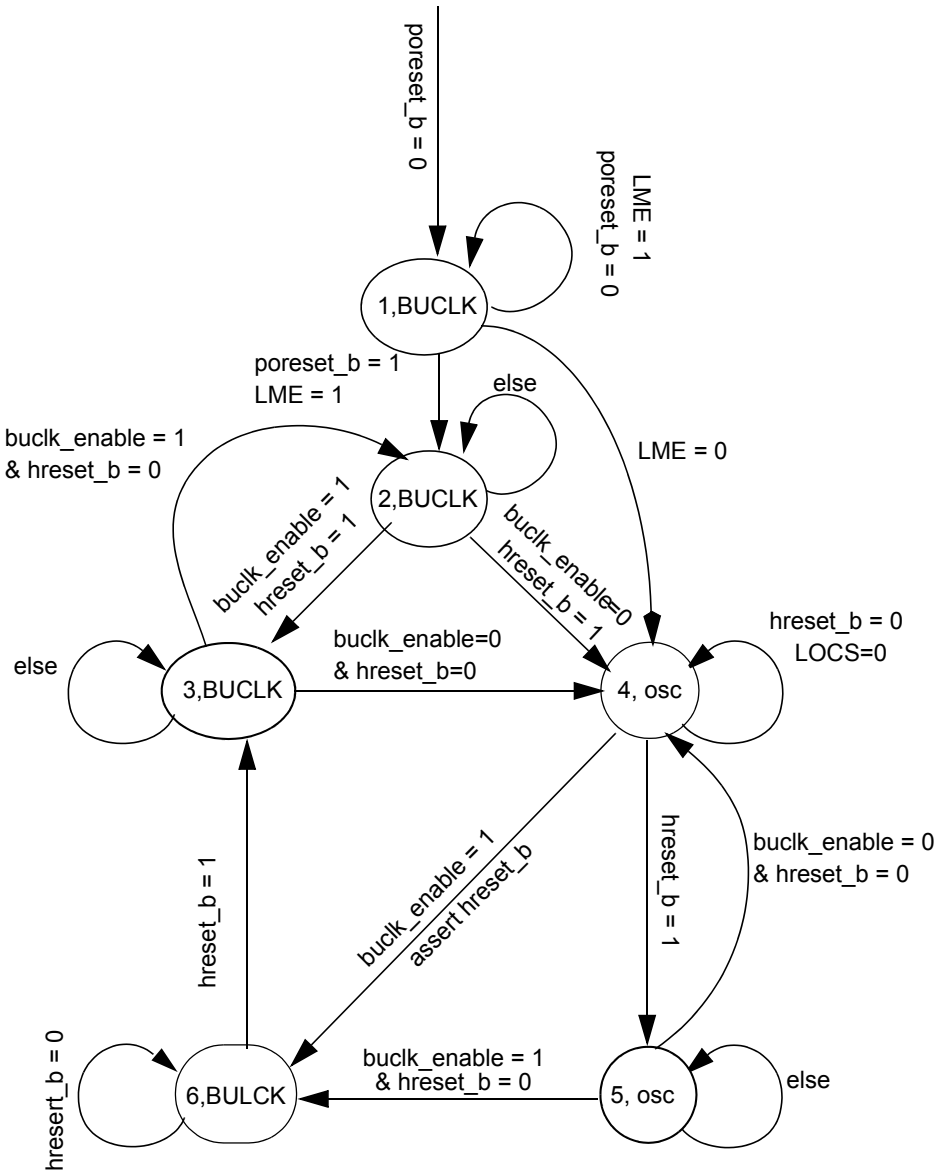


Figure 8-8. Clock Source Switching Flow Chart

NOTE

buclk_enable = (STBUC | LOC) and LME lock indicates loss of lock status bit (LOCS) for all cases and loss of clock sticky bit (LOCSS) when state 3 is active. When buclk_enable is changed, the chip asserts $\overline{\text{HRESET}}$ to switch the system clock to BUCLK or PLL.

At $\overline{\text{PORESET}}$ negation, if the PLL is not locked, the loss-of-clock sticky bit (LOCSS) is asserted, and the chip should operate with BUCLK.

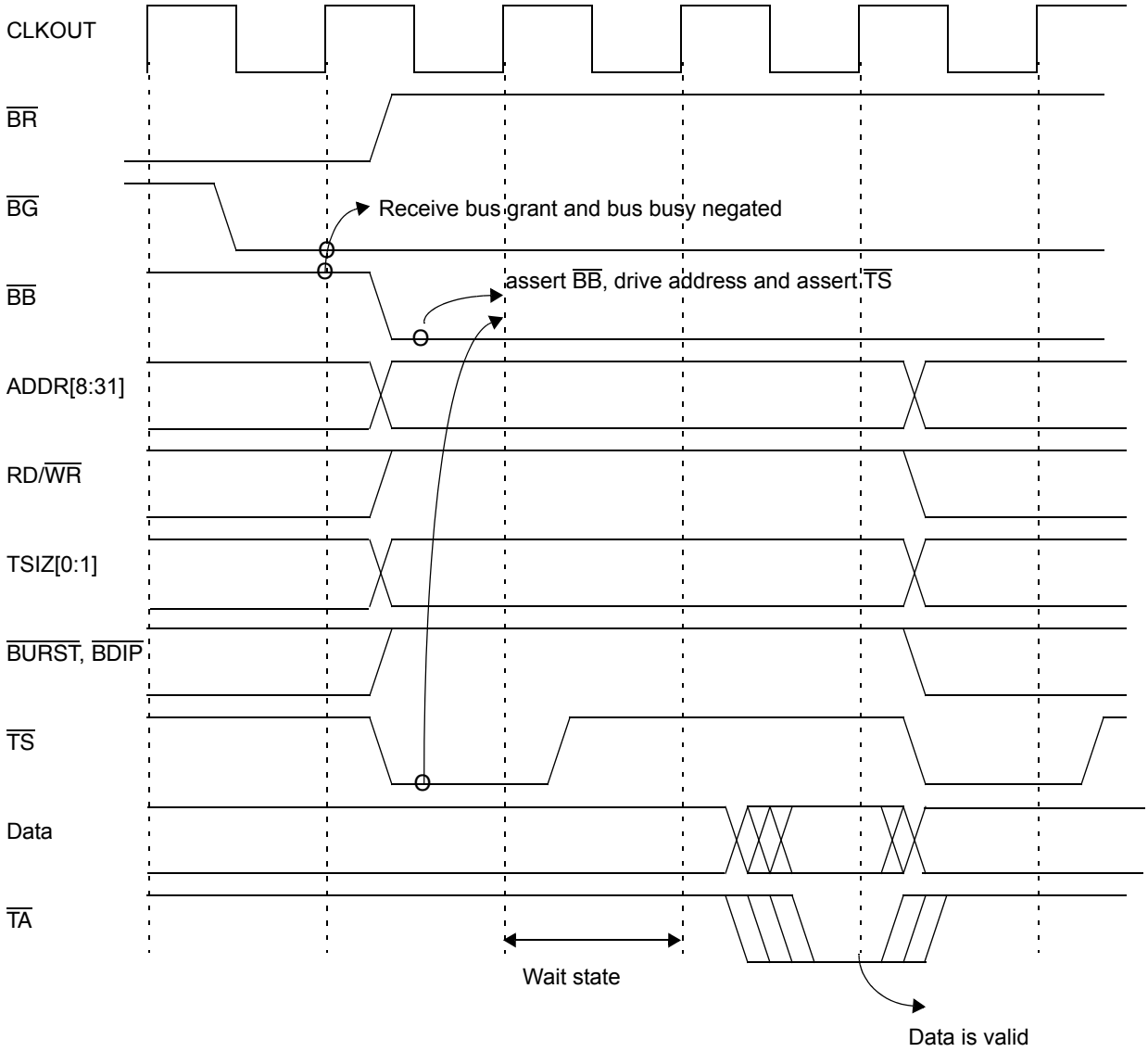


Figure 9-6. Single Beat Read Cycle – Basic Timing – One Wait State

9.5.2.2 Single Beat Write Flow

The basic write cycle begins with a bus arbitration, followed by the address transfer, then the data transfer. The handshakes are illustrated in the following flow and timing diagrams as applicable to the fixed transaction protocol.

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	CIE2	PIE2	SSE2	MQ2					RESUME	BQ2						
SRESET	0	0	0	0_0000					0	111_1111						
Addr	0x30 480E (QACR2_A), 0x30 4C0E (QACR2_B)															

Figure 13-11. Control Register 2 (QACR2)

Table 13-12. QACR2 Bit Descriptions

Bits	Name	Description
0	CIE2	Queue 2 Completion Software Interrupt Enable. CIE2 enables an interrupt upon completion of queue 2. The interrupt request is initiated when the conversion is complete for the CCW in queue 2. 0 Disable the queue completion interrupt associated with queue 2 1 Enable an interrupt after the conversion of the sample requested by the last CCW in queue 2
1	PIE2	Queue 2 Pause Software Interrupt Enable. PIE2 enables an interrupt when queue 2 enters the pause state. The interrupt request is initiated when conversion is complete for a CCW that has the pause bit set. 0 Disable the pause interrupt associated with queue 2 1 Enable an interrupt after the conversion of the sample requested by a CCW in queue 2 which has the pause bit set
2	SSE2	Queue 2 Single-Scan Enable Bit. SSE2 enables a single-scan of queue 2 to start after a trigger event occurs. The SSE2 bit may be set to a one during the same write cycle when the MQ2 bits are set for one of the single-scan queue operating modes. The single-scan enable bit can be written as a one or a zero, but is always read as a zero. The SSE2 bit enables a trigger event to initiate queue execution for any single-scan operation on queue 2. The QADC64E clears the SSE2 bit when the single-scan is complete. Refer to Table 13-13 for more information. 0 Trigger events are not accepted for single-scan modes 1 Accept a trigger event to start queue 2 in a single-scan mode
3:7	MQ2	Queue 2 Operating Mode. The MQ2 field selects the queue operating mode for queue 2. Refer to Table 13-13 for more information.
8	RESUME	0 After suspension, begin executing with the first CCW in queue 2 or the current sub-queue 1 After suspension, begin executing with the aborted CCW in queue 2

QADC64E to begin executing the CCWs in a queue or sub-queue. An “external trigger” is only one of the possible “trigger events.”

A scan sequence may be initiated by the following:

- A software command
- Expiration of the periodic/interval timer
- External trigger signal
- External gated signal (queue 1 only)

The software also specifies whether the QADC64E is to perform a single pass through the queue or is to scan continuously. When a single-scan mode is selected, the software selects the queue operating mode and sets the single-scan enable bit. When a continuous-scan mode is selected, the queue remains active in the selected queue operating mode after the QADC64E completes each queue scan sequence.

During queue execution, the QADC64E reads each CCW from the active queue and executes conversions in three stages:

- Initial sample
- Final sample
- Resolution

During initial sample, a buffered version of the selected input channel is connected to the sample capacitor at the input of the sample buffer amplifier.

During the final sample period, the sample buffer amplifier is bypassed, and the multiplexer input charges the sample capacitor directly. Each CCW specifies a final input sample time of two or 16 QCLK cycles. When an analog-to-digital conversion is complete, the result is written to the corresponding location in the result word table. The QADC64E continues to sequentially execute each CCW in the queue until the end of the queue is detected or a pause bit is found in a CCW.

When the pause bit is set in the current CCW, the QADC64E stops execution of the queue until a new trigger event occurs. The pause status flag bit is set, which may cause an interrupt to notify the software that the queue has reached the pause state. After the trigger event occurs, the paused state ends and the QADC64E continues to execute each CCW in the queue until another pause is encountered or the end of the queue is detected.

The following indicate the end-of-queue condition:

- The CCW channel field is programmed with 63 (0x3F) to specify the end of the queue
- The end-of-queue 1 is implied by the beginning of queue 2, which is specified in the BQ2 field in QACR2
- The physical end of the queue RAM space defines the end of either queue

When any of the end-of-queue conditions is recognized, a queue completion flag is set, and if enabled, an interrupt is issued to the software. The following situations prematurely terminate queue execution:

- Since queue 1 is higher in priority than queue 2, when a trigger event occurs on queue 1 during queue 2 execution, the execution of queue 2 is suspended by aborting the execution of the CCW in progress, and the queue 1 execution begins. When queue 1 execution is completed, queue 2

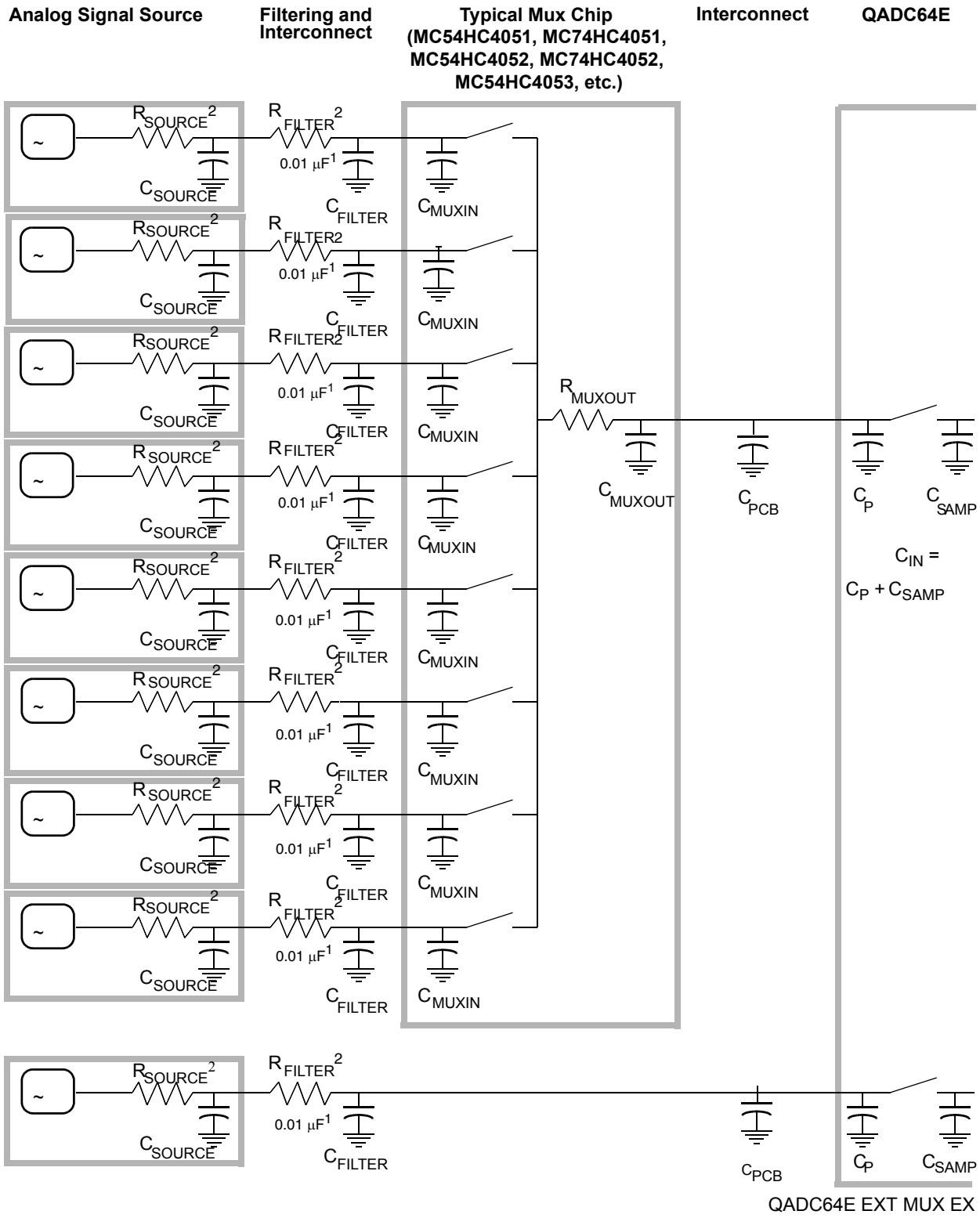


Figure 14-51. External Multiplexing of Analog Signal Sources

MSB 0	1	2	3	4	5	6	LSB 7
CONT	BITSE	DT	DSCK	PCS3	PCS2	PCS1	PCS0[1]
—	—	—	—	—	—	—	—
CONT	BITSE	DT	DSCK	PCS3	PCS2	PCS1	PCS0[1]
Command Control				Peripheral Chip Select			

The PCS0 bit represents the dual-function PCS0/$\overline{SS}$.

Figure 15-17. CR[0:F] — Command RAM 0x30 51C0, 0x30 51DF

Table 15-19. Command RAM Bit Descriptions

Bits	Name	Description
0	CONT	Continue 0 Control of chip selects returned to PORTQS after transfer is complete. 1 Peripheral chip selects remain asserted after transfer is complete.
1	BITSE	Bits per transfer enable 0 Eight bits 1 Number of bits set in BITS field of SPCR0.
2	DT	Delay after transfer 0 Delay after transfer is 17 ÷ f_{SYS}. 1 SPCR1 DTL[7:0] specifies delay after transfer PCS valid to SCK.
3	DSCK	PCS to SCK Delay 0 PCS valid to SCK delay is one-half SCK. 1 SPCR1 DSCKL[6:0] specifies delay from PCS valid to SCK.
4:7	PCS[3:0]	Peripheral chip selects. Use peripheral chip-select bits to select an external device for serial data transfer. More than one peripheral chip select may be activated at a time, and more than one peripheral chip can be connected to each PCS pin, provided proper fanout is observed. PCS0 shares a pin with the slave select ($\overline{SS}$) signal, which initiates slave mode serial transfer. If $\overline{SS}$ is taken low when the QSPI is in master mode, a mode fault occurs.

Refer to Section 15.6.5, “Master Mode Operation” for more information on the command RAM.

15.6.3 QSPI Pins

Seven pins are associated with the QSPI. When not needed by the QSPI, they can be configured for general-purpose I/O. Table 15-20 identifies the QSPI pins and their functions. Register DDRQS determines whether the pins are designated as input or output. The user must initialize DDRQS for the QSPI to function correctly.

but the data register (SC1DR) is still full. The data in the shifter that generated the OR assertion is overwritten by the next received data frame, but the data in the SC1DR is not lost.

If a 32-bit coherent operation is in progress when an edge (except for the first edge) is detected, the transfer of data from B1 to B2 is deferred until the coherent operation is completed. At any time, the input level present on the input signal can be read on the PIN bit.

The input pulse period is calculated by subtracting the value in data register B from the value in data register A.

Figure 17-17 provides an example of how the MDASM can be used for input period measurement.

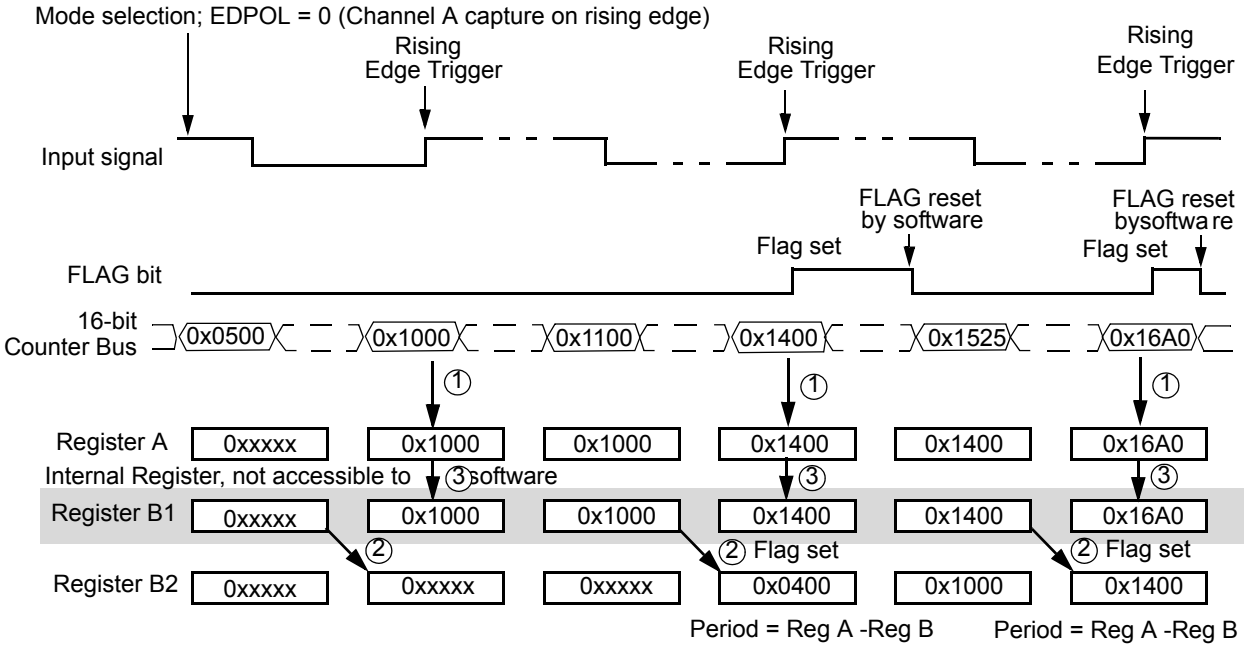


Figure 17-17. Input Period Measurement Example

17.9.3.4 Input Capture (IC) Mode

IC mode is selected by setting MODE[0:3] to 0b0011.

This mode is identical to the input period measurement mode (IPM) described above, with the exception that the FLAG line is also activated at the occurrence of the first detected edge of the selected polarity. In this mode the MDASM functions as a standard input capture function. In this case the value latched in channel B can be ignored. Figure 17-18 provides an example of how the MDASM can be used for input capture.

18.3.2 PPM Signal Short Functionality

The MPC561/MPC563 devices have many modules that multiplex their functions onto shared signals. In order to access those functions, the signals must be configured appropriately. However, choosing one function can be at the cost of another function. The PPM makes more functions available simultaneously by creating internal shorts that can activate functions that would otherwise require an external signal. Internal signal shorts are enabled using the PPM short register, SHORT_REG.

18.3.2.1 TouCAN Shorting

There are three TouCAN modules on the MPC561/MPC563 devices. Using the PPM it is possible to internally short the CNRX0 and CNTX0 signals of these three modules to increase message buffer capacity. Three bits of the SHORT_REG register (SH_TCAN[0:2]), are allocated to enable four combinations of shorting between the TouCAN modules. See Table 18-8 for information on these bit descriptions.

When one TouCAN module is shorted to another, the CANRX signals and the CANTX signals of both modules are shorted internally. Both modules continue to operate as normal but all transmit and receive operations are done using only one pair of CANRX and CANTX signals. The CANRX and CANTX signals of the other module are no longer under the control of the TouCAN module.

The C_TouCAN signals C_CNTX0 and C_CNRX0 are multiplexed signals. When C_TouCAN is shorted with one or two other TouCAN modules, C_TouCAN no longer has control of these signals and so they can be configured for another of the available functions. Refer to Chapter 2, “Signal Descriptions,” for more information. Also see Figure 18-24.

18.3.2.2 TPU Shorting

There are two TPU3 modules on the MPC561/MPC563 devices. Using the PPM, it is possible to internally short channel A_TPUCH0 with B_TPUCH0 and channel A_TPUCH1 with B_TPUCH1. Two bits of the SHORT_CH register (SH_TPU[1:0]) control the internal shorting. The input/output enable states of the TPU channels themselves determine the effect that the short bits have on the TPU modules’ operation. See Table 18-9 for information on SHORT_CH[SH_TPU] bit descriptions.

The PPM only controls the internal shorting of TPU3 channels TPUCH0 and TPUCH1. TPU channels are configured for input and output by the TPU ROM functions defined for them. Refer to Appendix D, “TPU3 ROM Functions” for further information, and see Figure 18-25. If TPU_A and TPU_B channel 0 are shorted via SHORT_CH[SH_TPU] and one is set to ouput while the other is set to input, then the data from the output channel will not appear on the pin of the input channel. This holds true if TPU_A and TPU_B channel 1 are shorted via SHORT_CH[SH_TPU]. Connect an external device to the pin of the module that has the channel function set to output.

18.3.2.3 ETRIG1 and ETRIG2

Each of the two QADC64E modules on the MPC561/MPC563 has an external trigger input signal that can be used to trigger analog to digital conversions. Using the PPM, these external trigger inputs can be sourced internally. Control for these short functions is found in SHORT_REG[SH_ET1] and

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	RX_DATA															
$\overline{\text{SRESET}}$	0000_0000_0000_0000															
Addr	0x30 5C16															

Figure 18-18. Receive Data Register (RX_DATA)

18.4.6 Receive Shift Register (RX_SHIFTER)

RX_SHIFTER receives data serially from the PPM input signals PPM_RX[0:1] (depending on the value of PPMPCR[OP_16_8]). Data bits are shifted in on every PPM_TCLK cycle. Data in the RX_SHIFTER register is delivered directly to the MPC561/MPC563 internal modules with no wait time.

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	RX_SHIFTER															
$\overline{\text{SRESET}}$	0000_0000_0000_0000															
Addr	0x30 5C1A															

Figure 18-19. Receive Shifter Register (RX_SHIFTER)

18.4.7 Transmit Data Register (TX_DATA)

TX_DATA contains data from the internally multiplexed modules that is to be transmitted from the PPM module on the PPM_TX[1:0] signals (depending on the value in PPMPCR[OP_16_8]). Data bits are transmitted serially (shifted out) on each PPM_TCLK cycle. The data is shifted out least significant bit (LSB) first, therefore TX_DATA15 first, TX_DATA0 last.

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	TX_DATA															
$\overline{\text{SRESET}}$	0000_0000_0000_0000															
Addr	0x30 5C1E															

Figure 18-20. Transmit Data Register (TX_DATA)

18.4.8 General-Purpose Data Out (GPDO)

GPDO is an internal register whose data can be transmitted serially through the PPM. By default, the transmit configuration registers are set to transmit from this register. The value in GPDO[0:15] is written into TX_DATA[0:15].

21.2.2 UC3F EEPROM Array Addressing

The UC3F array is divided into eight blocks, 64 Kbytes in size, which may be independently erased. Two blocks are host to a 16-Kbyte small block.

Seventeen bits of address are used to decode locations in the UC3F array. The read control logic in the UC3F EEPROM module decodes the upper 14 bits of that address to determine if the desired data is currently stored in one of the two read page buffers. If the data is already present in one of the two read page buffers, a read operation is not completed to the UC3F array core, and 64 bits of data are transferred from the appropriate read page buffer to the BIU. This type of array read access is an on-page read.

In the event that the read control logic determines that the desired data is not contained within one of the read page buffers, a read access to the UC3F array core is completed and 32 bytes of data are transferred from the array core. Only the addressed 64 bits of data will be transferred to the BIU. This type of array read access is an off-page read. The BIU contains logic to implement the read page buffer update and replacement scheme to transfer the 32 bytes of data into the appropriate read page buffer. If the read page update and replacement scheme contains a random access mode that does not update the read page buffers, the 32 bytes of data retrieved from the UC3F array core will not be transferred into either read page buffer. The BIU is expected to contain page update logic for controlling the updating of the read page buffers.

Write accesses to the UC3F array have no effect except during program and erase operation.

21.2.3 UC3F EEPROM Shadow Row

The UC3F EEPROM module contains a special shadow row that is used to hold reset configuration data and user data. See Figure 21-6.

The shadow row is accessed by setting UC3FMCR[SIE] = 1 and performing normal array accesses. Upon transitioning SIE (a 1-to-0 or 0-to-1 transition), the read page match decode circuit is reset so that the next array access is an off-page access.

The shadow row contains 512 bytes which are addressed for read accesses using the low order row and read page addresses.

The shadow row is implemented in the lowest numbered block of the array. In the case of a UC3F array configuration which also has a small block in the lowest numbered block of the array, the shadow row is contained in the small block. If SBEN[0] = 1 in this array configuration, the shadow row is treated as part of small block 0. SBPROTECT[0] and SBBLOCK[0] are used to control program and erase operation of the shadow row. If SBEN[0] = 0 in this array configuration, the shadow row is treated as part of the host block. The corresponding PROTECT and BLOCK bits are used to control program and erase operation of the shadow row.

NOTE

A module cannot read its own shadow row. On the MPC563 the program accessing the Flash shadow row must be executing from external memory or from internal SRAM.

Table 22-3. CRAMMCR Bit Descriptions (continued)

Bits	Name	Description
22	S0	Supervisor-only/supervisor-user privilege (Space assignment) — If the data relocate (DR) bit is set in Machine Status Register (MSR) and S0 is also set, then any access to the array block by a user program generates an error. If DR bit is 0, both user and supervisor program can access the array block, regardless of the value programmed in S0. The CALRAM array may be placed in supervisor or unrestricted space. This bit controls the highest 8-Kbyte block (lowest address) of CALRAM in the associated array. Likewise, S1, S2, and S3 control other three blocks in the same manner. See Table 22-4 for control bit address ranges. S0 = 0 and DR = 0 both user and supervisor access allowed (array 8-Kbyte block) S0 = 0 and DR = 1 both user and supervisor access allowed (array 8-Kbyte block) S0 = 1 and DR = 0 both user and supervisor access allowed (array 8-Kbyte block) S0 = 1 and DR = 1 only supervisor access allowed (array 8-Kbyte block)
23	R1	Same as R0 except for address ranges shown on Table 22-4.
24	D1	Same as D0 except for address ranges shown on Table 22-4.
25	S1	Same as S0 except for address ranges shown on Table 22-4.
26	R2	Same as R0 except for address ranges shown on Table 22-4.
27	D2	Same as D0 except for address ranges shown on Table 22-4.
28	S2	Same as S0 except for address ranges shown on Table 22-4.
29	R3	Same as R0 except for address ranges shown on Table 22-4.
30	D3	Same as D0 except for address ranges shown on Table 22-4.
31	S3	Same as S0 except for address ranges shown on Table 22-4.

Table 22-4. CRAMMCR Privilege Bit Assignment for 8-Kbyte Array Blocks

Bit Selection	Address Block (Relative)
R0, D0, and S0	0xXXXX 0000 – 0xXXXX 1FFF
R1, D1, and S1	0xXXXX 2000 – 0xXXXX 3FFF
R2, D2, and S2	0xXXXX 4000 – 0xXXXX 5FFF
R3, D3, and S3	0xXXXX 6000 – 0xXXXX 7FFF

22.5.2 CALRAM Region Base Address Registers (CRAM_RBAx)

The region base address register defines the base address of a region on the U-bus Flash memory space that will be overlaid by a portion of the CALRAM memory space and the region size. Because eight such regions in the Flash can be overlaid by the CALRAM, eight such registers (x = 0, 1, 2, 7) are provided.

The CRAM_RBAx[11:29] provides the base address (starting address) of the of the U-bus Flash region to be overlaid and the CRAM_RBAx[0:3] provides size corresponding to the region. See Table 22-6 for details. The RGN_SIZE[0] is reserved and should never be programmed to a one, because the MPC563 has only 512 Kbytes of Flash, and CRAM_RBAx[11] and CRAM_RBAx[12] should never be programmed to a one. Also, note that if CRAM_OVLCR[CLPS] is set, each of the eight sizes are forced

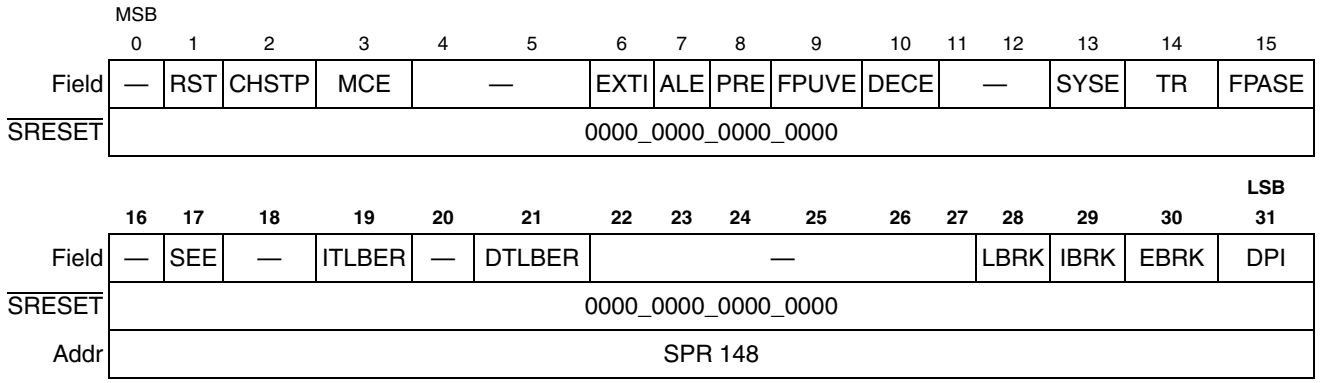


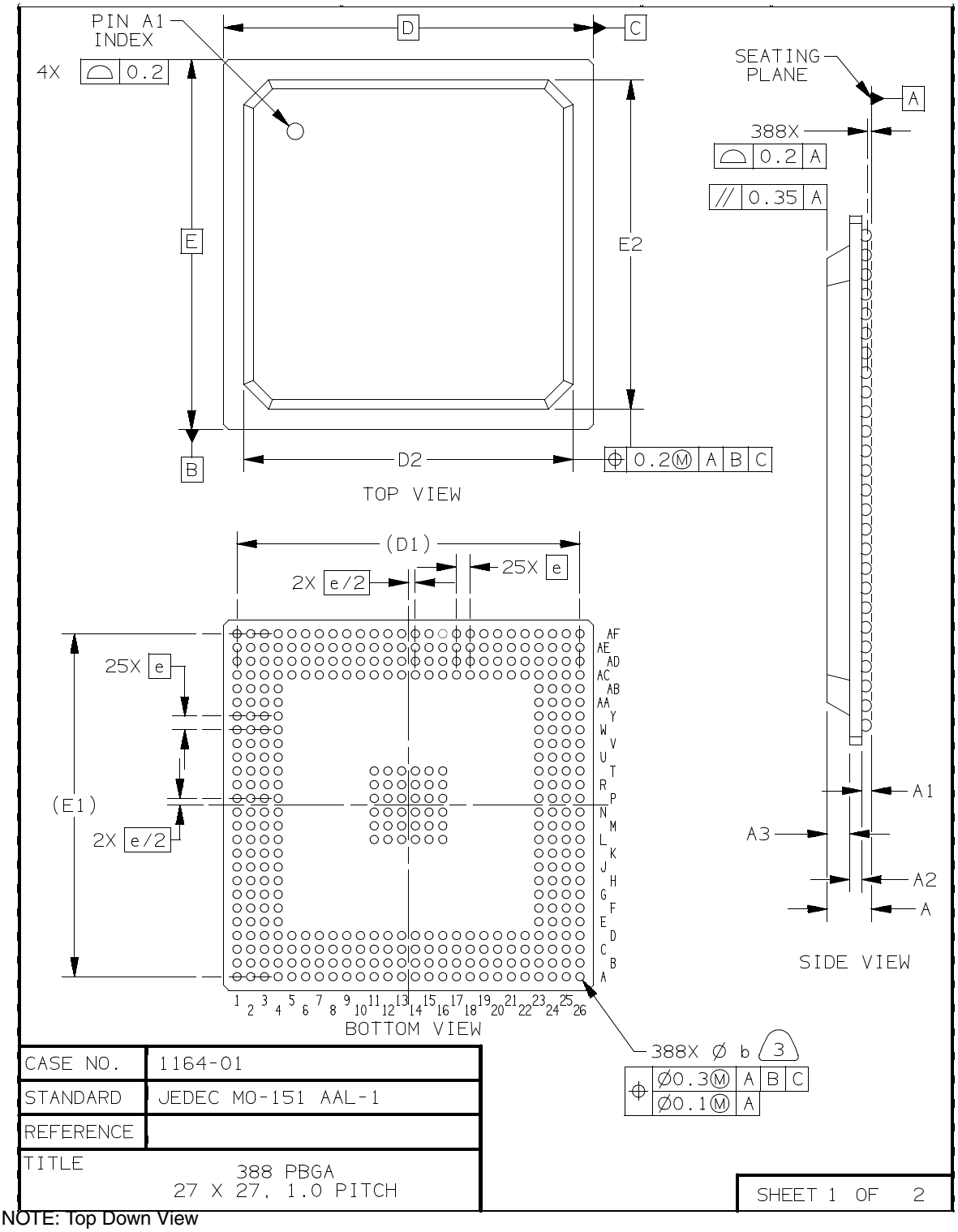
Figure 23-16. Exception Cause Register (ECR)

Table 23-18. ECR Bit Descriptions

Bits	Name	Description
0	—	Reserved
1	RST	Reset interrupt bit. This bit is set when the system reset pin is asserted.
2	CHSTP	Checkstop bit. Set when the processor enters checkstop state.
3	MCE	Machine check interrupt bit. Set when a machine check exception (other than one caused by a data storage or instruction storage error) is asserted.
4:5	—	Reserved
6	EXTI	External interrupt bit. Set when the external interrupt is asserted.
7	ALE	Alignment exception bit. Set when the alignment exception is asserted.
8	PRE	Program exception bit. Set when the program exception is asserted.
9	FPUVE	Floating point unavailable exception bit. Set when the program exception is asserted.
10	DECE	Decrementer exception bit. Set when the decrementer exception is asserted.
11:12	—	Reserved
13	SYSE	System call exception bit. Set when the system call exception is asserted.
14	TR	Trace exception bit. Set when in single-step mode or when in branch trace mode.
15	FPASE	Floating point assist exception bit. Set when the floating point assist exception occurs.
16	—	Reserved
17	SEE	Software emulation exception. Set when the software emulation exception is asserted.
18	—	Reserved
19	ITLBER	Implementation specific instruction protection error This bit is set as a result of an instruction protection error. Results in debug mode entry if debug mode is enabled and the corresponding enable bit is set.
20	—	Reserved
21	DTLBER	Implementation specific data protection error This bit is set as a result of an data protection error. Results in debug mode entry if debug mode is enabled and the corresponding enable bit is set.

Appendix C
Clock and Board Guidelines

The MPC561/MPC563 built-in PLL, oscillator, and other analog and sensitive circuits require that the board design follow special layout guidelines to ensure proper operation of the chip clocks. This appendix describes how the clock supplies and external components should be connected in a system. These guidelines must be fulfilled to reduce switching noise which is generated on internal and external buses during operation. Any noise injected into the sensitive clock and PLL logic reduces clock performance. The USIU maintains a PLL loss-of-lock warning indication that can be used to determine the clock stability in the MPC561/MPC563.



1 NOTE: Top Down View

Figure F-64. MPC561/MPC563 Package Footprint (1 of 2)

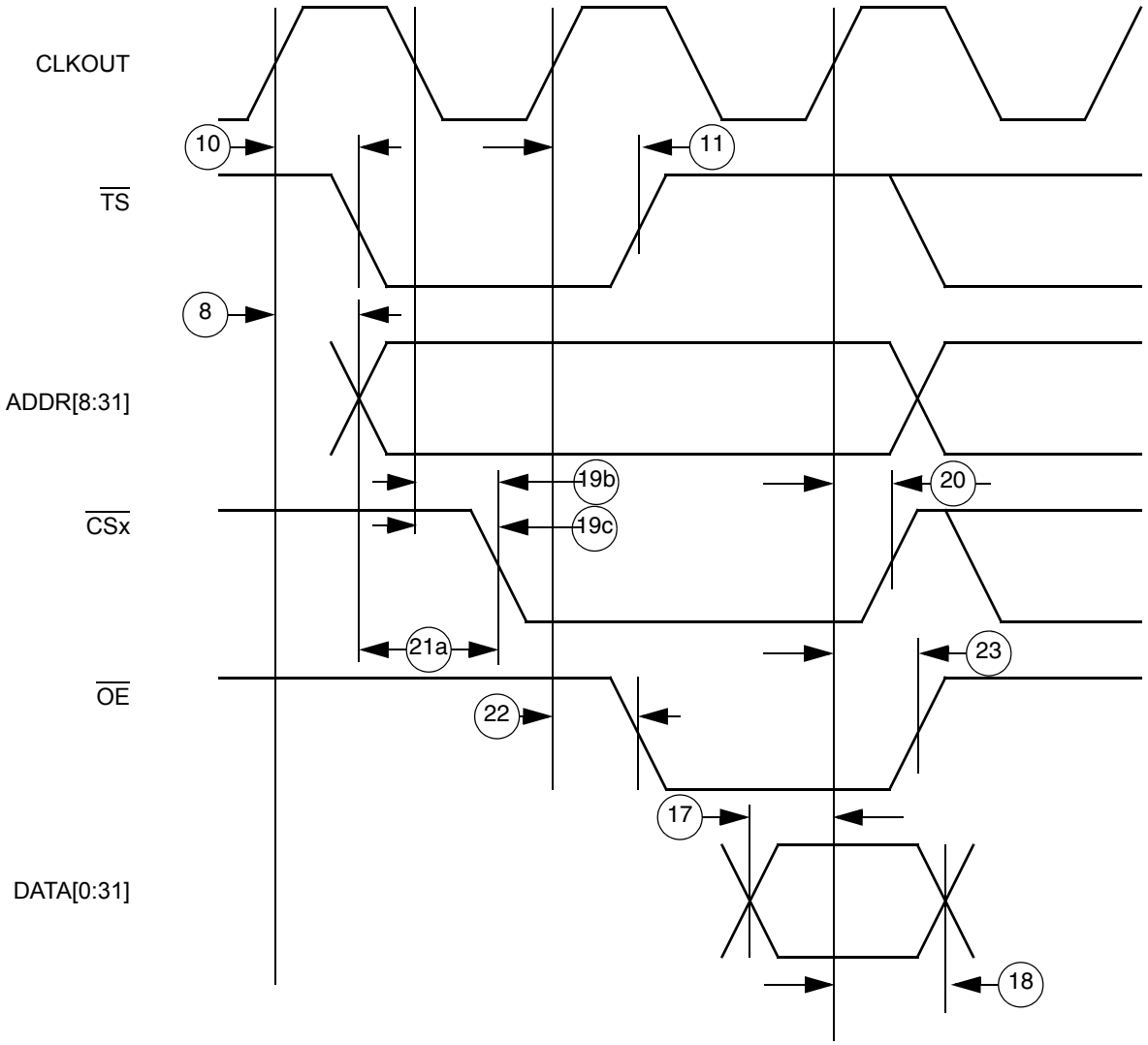


Figure G-17. External Bus Read Timing (GPCM Controlled – TRLX = '0' ACS = '11')