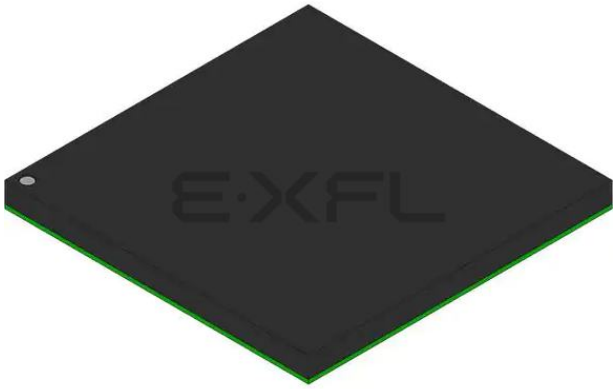

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PowerPC
Core Size	32-Bit Single-Core
Speed	56MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	56
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 2.7V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	388-BBGA
Supplier Device Package	388-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc564mzp56

Table 2-1. MPC561/MPC563 Signal Descriptions (continued)

Signal Name	No. of Signals	Type	Function after Reset[1]	Description
Interrupt Controller				
$\overline{\text{IRQ0}}$ / SGPIOC0 / MDO4	1	I	MDO4 if the Nexus (READI) port is enabled, $\overline{\text{IRQ0}}$ otherwise. See Section 2.5.	Interrupt Request 0. One of the eight external signals that can request, by means of the internal interrupt controller, a service routine from the RCPU. $\overline{\text{IRQ0}}$ is a non-maskable interrupt (NMI).
		I/O		Port SGPIOC0. Allows the signal to be used as a general-purpose input/output.
		O		READI Message Data Out. Message data out (MDO4) are output signals used for uploading OTM, BTM, DTM, and read/write accesses. External latching of MDO occurs on rising edge of MCKO. Eight signals are implemented.
$\overline{\text{IRQ1}}$ / $\overline{\text{RSV}}$ / SGPIOC1	1	I	$\overline{\text{IRQ1}}$	Interrupt Request 1. One of the eight external signals that can request, by means of the internal interrupt controller, a service routine from the RCPU.
		O		Reservation. This signal is used, together with the address bus, to indicate that the internal core initiated a transfer as a result of a STWCX or a LWARX instruction.
		I/O		Port SGPIOC1. Allows the signal to be used as a general-purpose input/output.
$\overline{\text{IRQ2}}$ / $\overline{\text{CR}}$ / SGPIOC2 / $\overline{\text{MTS}}$[2]	1	I	$\overline{\text{IRQ2}}$	Interrupt Request 2. One of the eight external signals that can request, by means of the internal interrupt controller, a service routine from the RCPU.
		I		Cancel Reservation. Instructs the MPC561/MPC563 to clear its reservation because some other master has touched its reserved space. An external bus snooper asserts this signal.
		I/O		Port SGPIOC2. Allows the signal to be used as a general-purpose input/output.
		O		Memory Transfer Start. This is the transfer start signal from the MPC561's memory controller that allows external memory access by an external bus master.
$\overline{\text{IRQ3}}$ / $\overline{\text{KR}}$ / $\overline{\text{RETRY}}$ / SGPIOC3	1	I	$\overline{\text{IRQ3}}$	Interrupt Request 3. One of the eight external signals that can request, by means of the internal interrupt controller, a service routine from the RCPU.
		I/O		Kill Reservation. In case of a bus cycle initiated by a STWCX instruction issued by the RCPU core to a non-local bus on which the storage reservation has been lost, this signal is used by the non-local bus interface to back-off the cycle.
		I/O		Retry. Indicates to a master that the cycle is terminated but should be repeated. As an input, it is driven by the external slave to retry a cycle.
		I/O		Port SGPIOC3. Allows the signal to be used as a general-purpose input/output.

Table 2-1. MPC561/MPC563 Signal Descriptions (continued)

Signal Name	No. of Signals	Type	Function after Reset[1]	Description
MPIO32B3 / VFLS0 / $\overline{\text{MSEO}}$	2	I/O	MPIO32B3 unless the Nexus (READI) port is enabled. See Section 2.5.	MIOS14 GPIO 3. Allows the signal to be used as a general-purpose input/output.
		O		Visible History Buffer Flush Status 0. This signal is output by the MPC561/MPC563 to allow program instruction flow tracking. It reports the number of instructions flushed from the history buffer in the RCPU. See Chapter 23, "Development Support," for details.
		O		$\overline{\text{MSEO}}$. Message start/end out ($\overline{\text{MSEO}}$) is an output signal which indicates when a message on the MDO signals has started, when a variable length packet has ended, and when the message has ended. External latching of $\overline{\text{MSEO}}$ occurs on rising edge of MCKO.
MPIO32B4 / VFLS1	1	I/O	MPIO32B4	MIOS14 GPIO 4. Allows the signal to be used as a general-purpose input/output.
		O		Visible History Buffer Flush Status 1. This signal is output by the MPC561/MPC563 to allow program instruction flow tracking. It reports the number of instructions flushed from the history buffer in the RCPU. See Chapter 23, "Development Support," for details.
MPIO32B5 / MDO5	1	I/O	MPIO32B5 unless the Nexus (READI) port is enabled, then MDO5. See Section 2.5.	MIOS14 GPIO 5. Allows the signal to be used as a general-purpose input/output.
		O		READI Message Data Out. Message data out (MDO5) is an output signal used for uploading OTM, BTM, DTM, and read/write accesses. External latching of MDO occurs on rising edge of MCKO. Eight MDO signals are implemented.
MPIO32B6 / MPWM4 / MDO6	1	I/O	MPIO32B6 unless the Nexus (READI) port is enabled, then MDO6. See Section 2.5.	MIOS14 GPIO 6. Allows the signal to be used as general-purpose input/output.
		I/O		Pulse Width Modulation 4. These signals provide variable pulse width outputs at a wide range of frequencies.
		O		READI Message Data Out. Message data out (MDO6) is an output signal used for uploading OTM, BTM, DTM, and read/write accesses. External latching of MDO occurs on rising edge of MCKO. Eight MDO signals are implemented.
MPIO32B[7:9] / MPWM[5, 20:21]	3	I/O	MPIO32B[7:9]	MIOS14 GPIO[7:9]. Allows these signals to be used as general-purpose input/outputs.
		I/O		Pulse Width Modulation [5, 20:21]. These signals provide variable pulse width outputs at a wide range of frequencies.
MPIO32B10 / PPM_TSYNC	1	I/O	MPIO32B10	MIOS14 GPIO 10. This function allows the signals to be used as general-purpose inputs/outputs.
		O		PPM_TSYNC. Synchronizes the data between the PPM and peripheral devices.
MPIO32B11 / C_CNRX0[6]	1	I/O	MPIO32B11	MIOS14 GPIO 11. This function allows the signals to be used as general-purpose inputs/outputs.
		I		TouCAN_C Receive Data. This is the serial data input signal for the TouCAN_C module.

- Drive JCOMP/$\overline{\text{RSTI}}$ high

Nexus mode is exited by:

- Hold JCOMP/$\overline{\text{RSTI}}$ low to reset Nexus port
- Hold TMS/$\overline{\text{EVTI}}$ high to disable Nexus mode at least 4 clocks before driving JCOMP/$\overline{\text{RSTI}}$ high
- Drive JCOMP/$\overline{\text{RSTI}}$ high

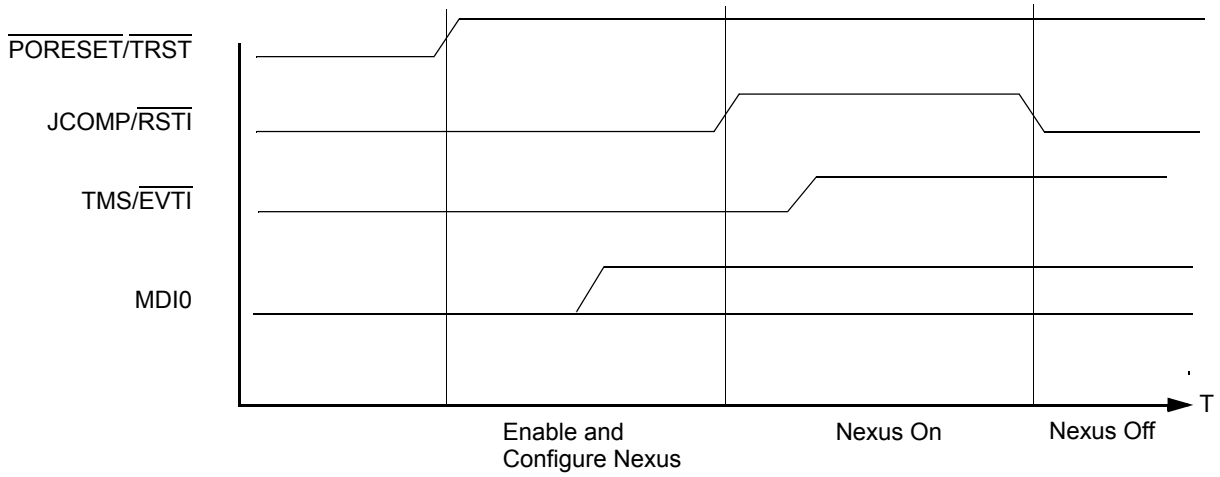

Figure 2-6. Debug Mode Selection (Nexus)

2.6 Reset State

During reset, a 130-µA (maximum) resistor "weakly pulls" all input signals, with the exception of the power-supply and clock-related signals, to a value based on conditions described in Appendix F, "Electrical Characteristics." In reset state, all I/O signals become inputs, and all outputs (except for CLKOUT, $\overline{\text{HRESET}}$, and $\overline{\text{SRESET}}$) are pulled only by the pull-up/pull-down.

2.6.1 Signal Functionality Configuration Out of Reset

The reset configuration word (RCW) defines the post-reset functionality of some multiplexed signals. For details on these signals and how they are configured, refer to Section 7.5.2, "Hard Reset Configuration Word."

The 2.6-V bus related signals have selectable output buffer drive strengths that are controlled by the COM0 bit in the USIU's system clock and reset control register (SCCR). The control is as follows:

0 = 2.6-V bus signals full drive (50-pF load)

1 = 2.6-V bus signals reduced drive (25-pF load)

2.6.2 Signal State During Reset

While $\overline{\text{HRESET}}$ is asserted, the reset-configuration value is latched from the data bus into various bits on the part. The function of many signals depends upon the value latched. If the value on the data bus changes, then the function of various signals may also change. This is especially true if the reset configuration word (RCW) comes from the Flash, because the Flash does not drive the RCW until 256 clocks after the start of

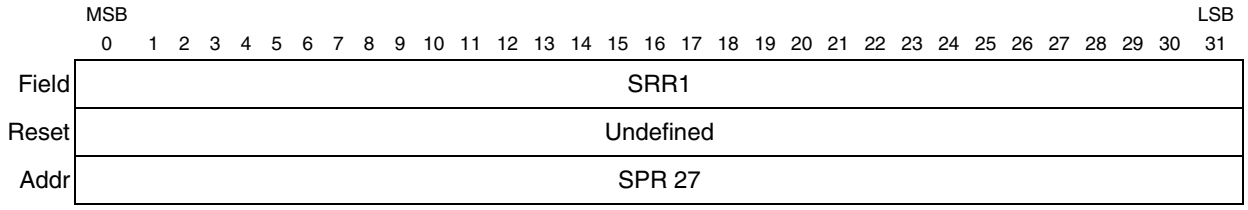

Figure 3-15. Machine Status Save/Restore Register 1 (SRR1)

In general, when an exception occurs, SRR1[0:15] are loaded with exception-specific information, and MSR[16:31] are placed into SRR1[16:31].

3.9.8 General SPRs (SPRG0–SPRG3)

SPRG0–SPRG3, SPRs 272-275, are provided for general operating system use, such as fast-state saves and multiprocessor-implementation support. SPRG0–SPRG3 are shown below.

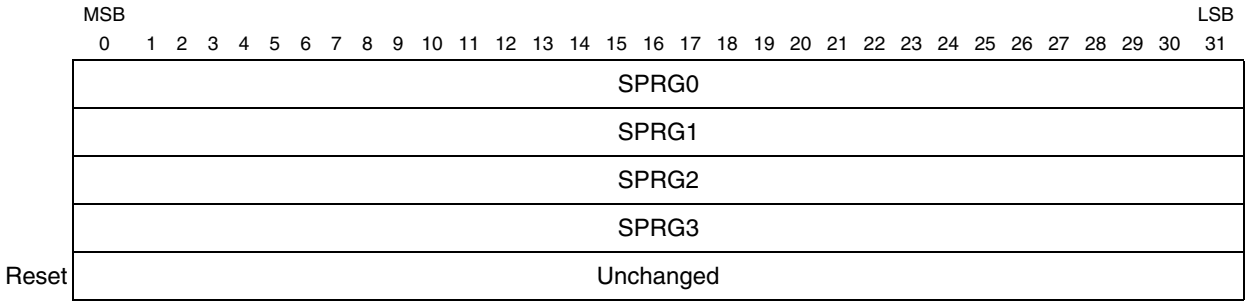

Figure 3-16. SPRG0–SPRG3 — General Special-Purpose Registers 0–3

Uses for SPRG0–SPRG3 are shown in Table 3-13.

Table 3-13. Uses of SPRG0–SPRG3

Register	Description
SPRG0	Software may load a unique physical address in this register to identify an area of memory reserved for use by the exception handler. This area must be unique for each processor in the system.
SPRG1	This register may be used as a scratch register by the exception handler to save the content of a GPR. That GPR then can be loaded from SPRG0 and used as a base register to save other GPRs to memory.
SPRG2	This register may be used by the operating system as needed.
SPRG3	This register may be used by the operating system as needed.

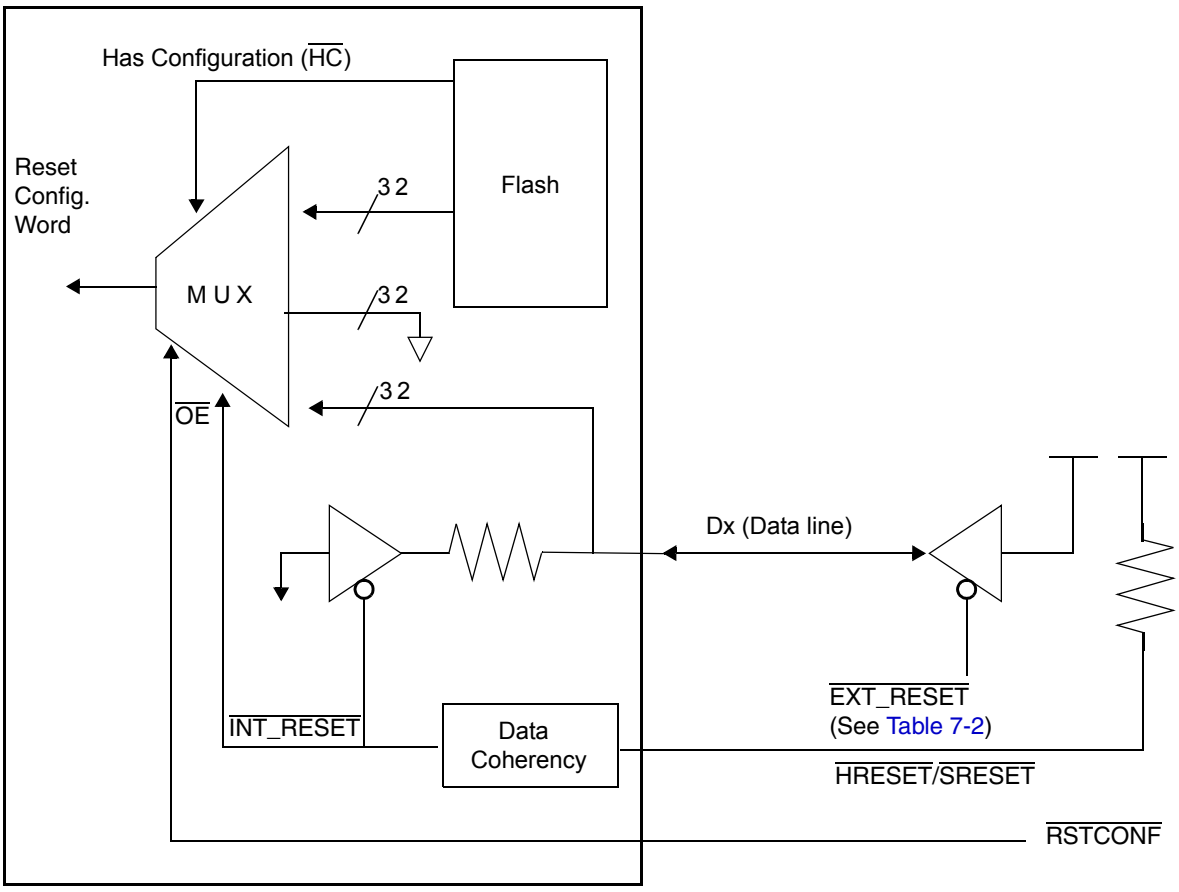

Figure 7-2. Reset Configuration Basic Scheme

During the assertion of the PORESET input signal, the chip assumes the default reset configuration. This assumed configuration changes if the input signal RSTCONF is asserted when the PORESET is negated or the CLKOUT starts to oscillate. To ensure that stable data is sampled, the hardware configuration is sampled every eight clock cycles on the rising edge of CLKOUT with a double buffer. The setup time required for the data bus is approximately 15 cycles (defined as Tsup in the following figures) and the maximum rise time of HRESET should be less than six clock cycles. In systems where an external reset configuration word and the TEXP output function are both required, RSTCONF should be asserted until SRESET is negated.

Figure 7-3 to Figure 7-6 provide sample reset configuration timings.

NOTE

Timing diagrams in the following figures are not to scale.

Table 7-5. RCW Bit Descriptions (continued)

Bits	Name	Description
24:25	OERC	Other Exceptions Relocation Control — These bits effect only if ETRE was enabled. See Table 4-2. Relocation offset: 00 Offset 0 01 Offset 64 Kbytes 10 Offset 512 Kbytes 11 Offset to 0x003F E000
26:27	—	Reserved
28:30	ISB	Internal Space Base Select — This field defines the initial value of the ISB field in the IMMR register. A detailed description is in Table 6-12. The default state is that the internal memory map is mapped to start at address 0x0000_0000. This bit must not be high in the reset configuration word.
31	DME	Dual Mapping Enable — This bit determines whether Dual mapping of the internal Flash is enabled. For a detailed description refer to Table 10-11. The default state is that dual mapping is disabled. 0 Dual mapping disabled 1 Dual mapping enabled

1 Bit 15 always comes from the internal Flash Reset Configuration Word (MPC563 only).

2 This bit should not be set on the MPC561/MPC562.

3 This bit is $\overline{\text{HC}}$ if read from the internal Flash Reset Configuration Word. See Section 21.2.3.1, “Reset Configuration Word (UC3FCFIG).”

4 Available only on the MPC562/MPC564, software should write "0" to this bit for MPC561/MPC563.

7.5.3 Soft Reset Configuration

When a soft reset event occurs, the MPC561/MPC563 reconfigures the development port. Refer to Chapter 23, “Development Support,” for details.

indicating that the module is locked in legacy mode. In order to change the value of the FLIP bit, the operating mode must first be unlocked by setting the LOCK bit. Only then can the FLIP bit be changed. Finally, the LOCK bit must be cleared again to protect the state of the FLIP bit from future writes.

1. Write LOCK = 1 to unlock operating mode bit.
2. Modify the value of FLIP as required.
   - FLIP = 0 legacy mode enabled
   - FLIP = 1 enhanced mode enabled
3. Write LOCK = 0 and new FLIP bit value to preserve the value of FLIP bit

- Example 1: switching from legacy mode to enhanced mode
  - QADCMCR = 0x280; LOCK =1, SUPV = 1
  - QADCMCR = 0x380; LOCK =1, write FLIP = 1, SUPV = 1
  - QADCMCR = 0x180; LOCK = 0, FLIP = 1, SUPV = 1

  Subsequent writes to the FLIP bit will have no effect while LOCK = 0.
- Example 2: switching from enhanced mode to legacy mode
  - QADCMCR = 0x280 or 0x380; LOCK = 1, SUPV =1 (Can write FLIP = x since value will not change)
  - QADCMCR = 0x280; LOCK = 1, FLIP = 0, SUPV = 1
  - QADCMCR = 0x080; LOCK = 0, FLIP = 0, SUPV =1

14.3.1.4 Supervisor/Unrestricted Address Space

The QADC64E memory map is divided into two segments: supervisor-only data space and assignable data space. Access to supervisor-only data space is permitted only when the software is operating in supervisor access mode. Assignable data space can be either restricted to supervisor-only access or unrestricted to both supervisor and user data space accesses. The SUPV bit in the QADCMCR designates the assignable space as supervisor or unrestricted.

The following information applies to accesses to address space located within the module's 16-bit boundaries and where the response is a bus error. See Table 14-6 for more information.

- Attempts to read a supervisor-only data space when not in the supervisor access mode and SUPV = 1, causes the bus master to assert a bus error condition. No data is returned. If SUPV = 0, the QADC64E asserts a bus error condition and no data is returned.
- Attempts to write to supervisor-only data space when not in the supervisor access mode and SUPV = 1, causes the bus master to assert a bus error condition. No data is written. If SUPV = 0, the QADC64E asserts a bus error condition and the register is not written.
- Attempts to read unimplemented data space in the unrestricted access mode and SUPV = 1, causes the bus master to assert a bus error condition and no data is returned. In all other attempts to read unimplemented data space, the QADC64E causes a bus error condition and no data is returned.
- Attempts to write unimplemented data space in the unrestricted access mode and SUPV= 1, causes the bus master to assert a bus error condition and no data is written. In all other

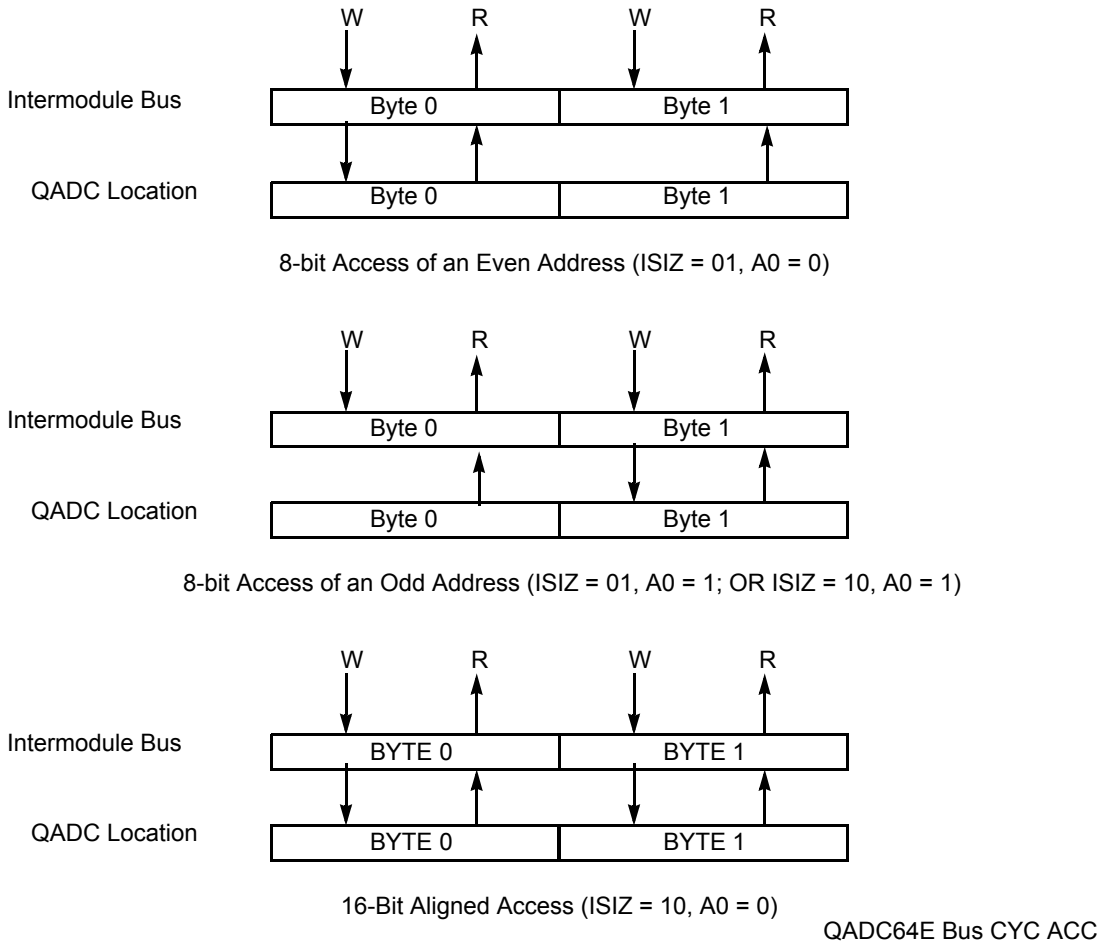

Figure 14-24. Bus Cycle Accesses

Byte access to an even address of a QADC64E location is shown in the top illustration of Figure 14-24. In the case of write cycles, byte 1 of the register is not disturbed. In the case of a read cycle, the QADC64E provides both byte 0 and byte 1.

Byte access to an odd address of a QADC64E location is shown in the center illustration of Figure 14-24. In the case of write cycles, byte 0 of the register is not disturbed. In the case of read cycles, the QADC64E provides both byte 0 and byte 1.

16-bit accesses to an even address read or write byte 0 and byte 1 as shown in the lowest illustration of Figure 14-24. The full 16 bits of data is written to and read from the QADC64E location with each access.

16-bit accesses to an odd address require two bus cycles; one byte of two different 16-bit QADC64E locations is accessed. The first bus cycle is treated by the QADC64E as an 8-bit read or write of an odd address. The second cycle is an 8-bit read or write of an even address. The QADC64E address space is organized into 16-bit even address locations, so a 16-bit read or write of an odd address obtains or provides the lower half of one QADC64E location, and the upper half of the following QADC64E location.

Since the sample amplifier is powered by V_{DDA} and V_{SSA}, it can accurately transfer input signal levels up to but not exceeding V_{DDA} and down to but not below V_{SSA}. If the input signal is outside of this range, the output from the sample amplifier is clipped.

In addition, V_{RH} and V_{RL} must be within the range defined by V_{DDA} and V_{SSA}. As long as V_{RH} is less than or equal to V_{DDA} and V_{RL} is greater than or equal to V_{SSA} and the sample amplifier has accurately transferred the input signal, resolution is ratiometric within the limits defined by V_{RL} and V_{RH}. If V_{RH} is greater than V_{DDA}, the sample amplifier can never transfer a full-scale value. If V_{RL} is less than V_{SSA}, the sample amplifier can never transfer a zero value.

Figure 14-48 shows the results of reference voltages outside the range defined by V_{DDA} and V_{SSA}. At the top of the input signal range, V_{DDA} is 10 mV lower than V_{RH}. This results in a maximum obtainable 10-bit conversion value of 0x3FE. At the bottom of the signal range, V_{SSA} is 15 mV higher than V_{RL}, resulting in a minimum obtainable 10-bit conversion value of three.

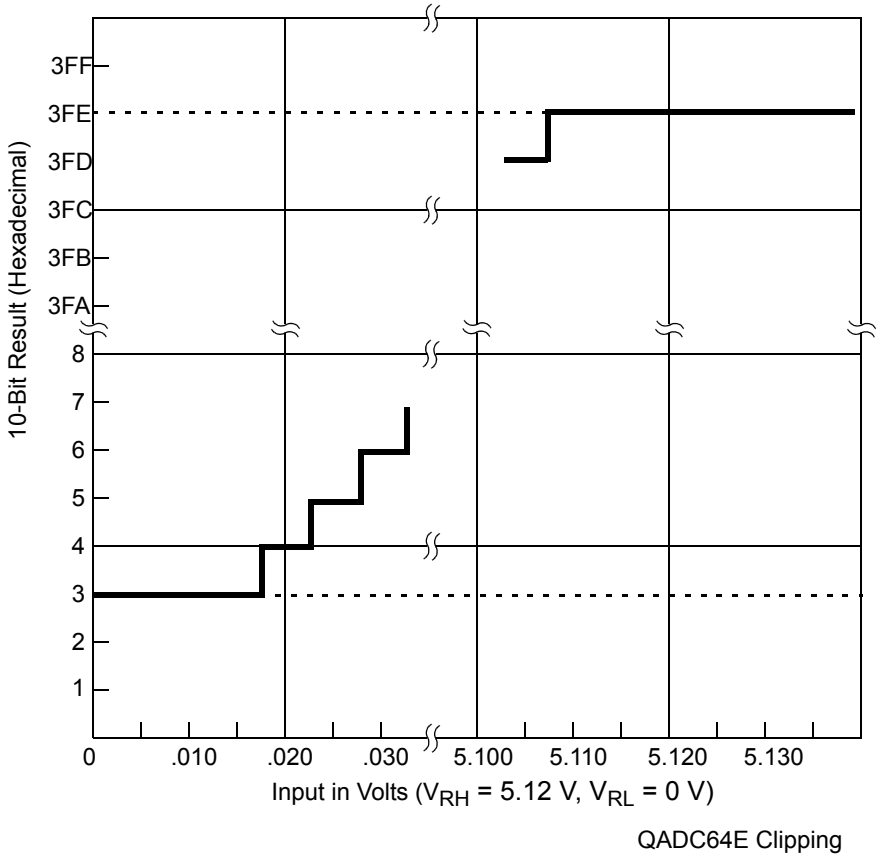

Figure 14-48. Errors Resulting from Clipping

14.6.3.1 Analog Supply Filtering and Grounding

Two important factors influencing performance in analog integrated circuits are supply filtering and grounding. Generally, digital circuits use bypass capacitors on every V_{DD}/V_{SS} signal pair. This applies to analog sub-modules also. The distribution of power and ground is equally important.

15.8.8 QSCI1 Receiver Block Diagram

The block diagram of the enhancements to the SCI receiver is shown below in Figure 15-38.

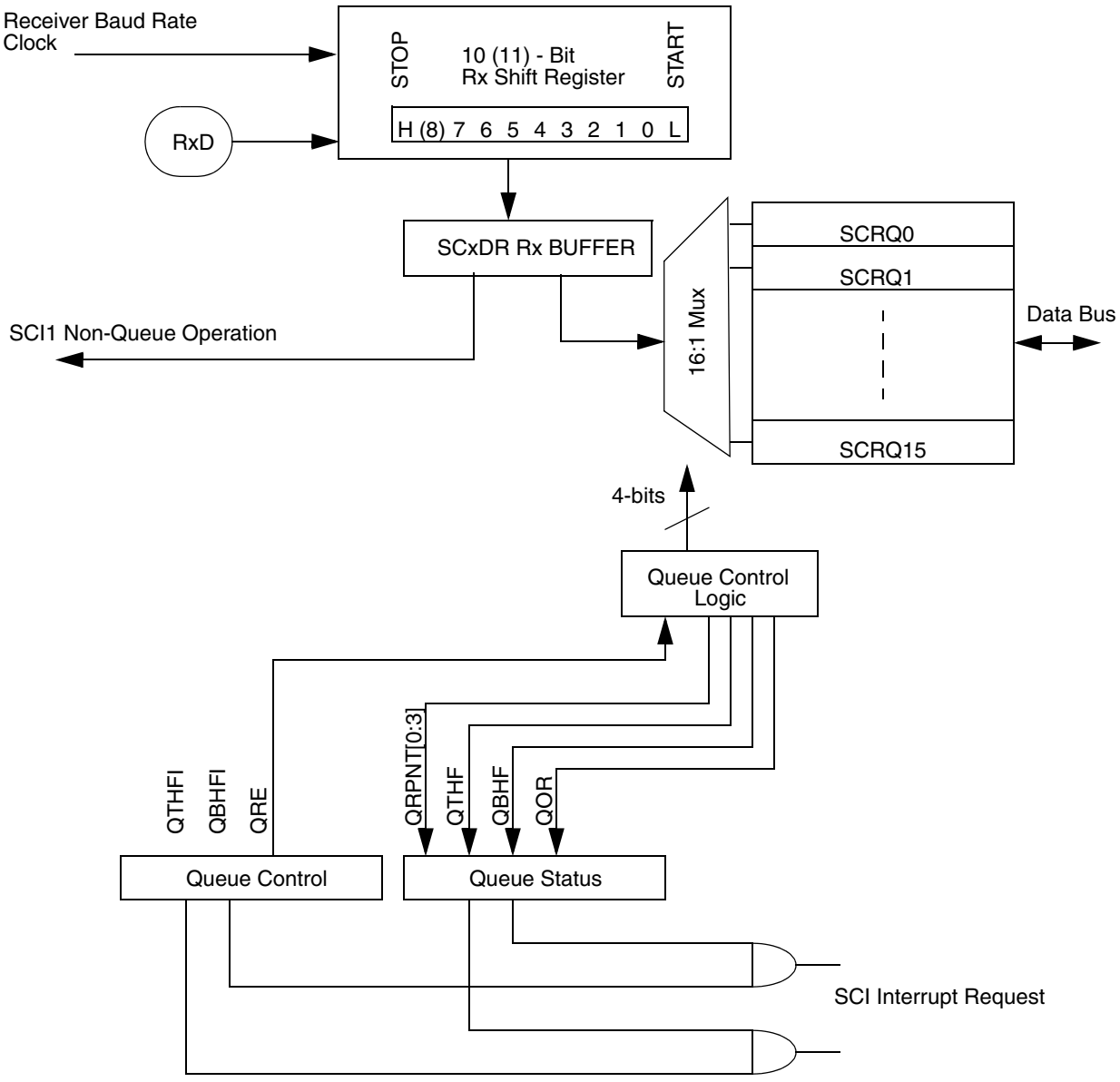

Figure 15-38. Queue Receiver Block Enhancements

15.8.9 QSCI1 Additional Receive Operation Features

Additional QSCI1 features include:

- Available on a single SCI channel (SCI1) implemented by the queue receiver enable (QRE) bit set by software. When the queue is enabled, software should ignore the RDRF bit.
- When the queue is disabled (QRE = 0), the SCI functions in single buffer receive mode (as originally designed) and RDRF and OR function as previously defined. Locations SCRQ[0:15] can

17.2 MIOS14 Key Features

The basic features of the MIOS14 are as follows:

- Modular architecture at the silicon implementation level
- Disable capability in each submodule to allow power saving when its function is not needed
- Six 16-bit counter buses to allow action submodules to use counter data
- When not used for timing functions, every channel signal can be used as a port signal: I/O, output only or input only, depending on the channel function.
- Submodules' signal status bits reflect the status of the signal
- MIOS14 counter prescaler submodule (MCPSM):
  - Centralized counter clock generator
  - Programmable 4-bit modulus down-counter
  - Wide range of possible division ratios: 2 through 16
  - Count inhibit under software control
- MIOS14 modulus counter submodule (MMCSM):
  - Programmable 16-bit modulus up-counter with built-in programmable 8-bit prescaler clocked by MCPSM output.
  - Maximum increment frequency of the counter:
    - Clocked by the internal MCPSM output: $f_{SYS} / 2$
    - Clocked by the external signal: $f_{SYS} / 4$
  - Flag setting and possible interrupt generation on overflow of the up-counter
  - Time counter on internal clock with interrupt capability after a pre-determined time
  - Optional signal usable as an external event counter (pulse accumulator) with overflow and interrupt capability after a pre-determined number of external events.
  - Usable as a regular free-running up-counter
  - Capable of driving a dedicated 16-bit counter bus to provide timing information to action submodules (the value driven is the contents of the 16-bit up-counter register)
  - Optional signal to externally force a load to the counter with modulus value
- MIOS14 double action submodule (MDASM):
  - Versatile 16-bit dual action unit allowing two events to occur before software intervention is required
  - Six software selectable modes allowing the MDASM to perform pulse width and period measurements, PWM generation, single input capture and output compare operations as well as port functions
  - Software selection of one of the six possible 16-bit counter buses used for timing operations
  - Flag setting and possible interrupt generation after MDASM action completion
  - Software selection of output pulse polarity
  - Software selection of totem-pole or open-drain output
  - Software readable output signal status

Table 17-29. MPWMSCR Bit Descriptions

Bits	Name	Description
0	PIN	Pin input status bit — The PIN bit reflects the state present on the MPWMSM signal. The software can thus monitor the pin state. The PIN bit is a read-only bit. Writing to the PIN bit has no effect.
1	DDR	Data direction register — The DDR bit indicates the direction for the signal when the PWM function is not used (disable mode). 0 signal is in input. 1 signal is in output. The DDR bit is cleared by reset. Table 17-30 lists the different uses for the polarity (POL) bit, the enable (EN) bit and the data direction register (DDR) bit.
2	FREN	Freeze enable bit — This active high read/write control bit enables the MPWMSM to recognize the freeze signal on the MIOB. 0 MPWMSM not frozen even if the MIOB freeze line is active. 1 MPWMSM frozen if the MIOB freeze line is active. The FREN is cleared by reset.
3	TRSP	Transparent mode — The TRSP bit indicates that the MPWMSM is in transparent mode. In transparent mode, when the software writes to either the MPWMPERR or MPWMPULR1 register the value written is immediately transferred to the counter or register MPWMPULR2 respectively. 0 Double-buffered mode. 1 Transparent mode. The TRSP bit is cleared by reset.
4	POL	Output polarity control bit — The POL bit works in conjunction with the EN bit and controls whether the MPWMSM drives the signal with the direct or the inverted value of the output flip-flop. Table 17-30 lists the different uses for the polarity (POL) bit, the enable (EN) bit and the data direction register (DDR) bit.
5	EN	Enable PWM signal generation — The EN bit defines whether the MPWMSM generates a PWM signal or is used as an I/O channel: 0 PWM generation disabled (signal can be used as I/O). 1 PWM generation enabled (the signal is in output mode). Each time the submodule is enabled, the value of CP is loaded into the prescaler. The EN bit is cleared by reset.
6:7	—	Reserved
8:15	CP	Clock prescaler — This 8-bit read/write data register stores the modulus value for loading into the built-in 8-bit clock prescaler. The value loaded defines the divide ratio for the signal that clocks the MPWMSM. The new value is loaded into the prescaler counter on the prescaler counter overflow, or upon the EN bit of the MPWMSCR being set. Table 17-31 gives the clock divide ratio according to the value of CP.

Table 17-30. PWMSM Output Signal Polarity Selection

Control Bits			Signal Direction	Signal State	Periodic Edge	Variable Edge	Optional Interruption
POL	EN	DDR					
0	0	0	Input	INPUT	—	—	—
0	0	1	Output	Always Low	—	—	—
0	1	X	Output	High Pulse	Falling Edge	Rising Edge	Falling Edge
1	0	0	Input	INPUT	—	—	—

Table 21-4. UC3FMCRE Bit Descriptions (continued)

Bits	Name	Description
4:5	SBDATA	Small block data space. Each small array block of the UC3F EEPROM may be mapped into data or both data and instruction address space. When a small array block is mapped into data address space, SBDATA[M] = 1, only data accesses will be allowed. When a small array block is mapped into both data and instruction address space, SBDATA[M] = 0, both data and instruction accesses will be allowed. If SBEN[M] = 0, the corresponding small block M is logically part of the host block and SBDATA[M] has no effect. Instead, the corresponding DATA[M] bit will be used to determine if the small block is mapped to Data or to both Data and Instruction address space. Like the DATA bits, the SBDATA bits are not actually used in the UC3F EEPROM module but are used by the BIU to determine access restrictions to the UC3F array. Block addresses are decoded in the BIU to determine which small array block is selected, and the selected small block's SBDATA bit is compared with the address space attributes to determine validity of an array access. 0 small block M is placed in both Data and Instruction address spaces 1 small block M is placed in Data address space
6:7	SBPROTECT	Small block protect. Each small block of the UC3F EEPROM can be individually protected from program or erase operation. The UC3F will perform all program and erase interlocks and even complete the program or erase sequence, but the program and erase voltages are not applied to locations within the protected small block(s). 0 small block M is unprotected 1 small block M is protected
8:9	—	Reserved
10:15	BIU	BIU configuration bits. These register bits are reserved for BIU functionality and are strictly outputs from the UC3F EEPROM.
16:18	MEMSIZ	Memory size. The MEMSIZ field is used to indicate the UC3F array size. The MEMSIZ bits are read only and writes have no effect. 000 UC3F array is 64 Kbytes 001 UC3F array is 128 Kbytes 010 UC3F array is 192 Kbytes 011 UC3F array is 256 Kbytes 100 unused 101 UC3F array is 512 Kbytes 110 unused 111 unused The Flash module on the MPC563 is 512 Kbytes.
19	BLK	Block size. The BLK bit is used to indicate the array block size used in the UC3F array. The BLK bit is read only and writes have no effect. 0 array block size is 32 Kbytes 1 block size is 64 Kbytes NOTE: All blocks are 64 Kbytes (i.e. BLK is always set)
20	MAP	Array address mapping. The MAP bit is used to indicate the UC3F array address mapping within a 2^N address space. The MAP bit is read only and writes have no effect. The MAP bit is more useful when the UC3F array is a non-2^N size. When MAP = 0, the UC3F array is mapped to the bottom (starting at address 0) of the 2^N space in which the array resides. For modules with 2^N array sizes, the MAP bit is always set to 0. When MAP = 1, the UC3F array is mapped to the top (ending at address all $F's) of the 2^N space in which the array resides. 0 UC3F array is mapped to bottom of 2^N address space 1 UC3F array is mapped to top of 2^N address space

Table 23-26. ICTRL Bit Descriptions (continued)

Bits	Mnemonic	Description	Function	
			Non-compressed mode[1]	Compressed Mode[2]
20	SIWP0EN	Software trap enable selection of the 1st I-bus watchpoint	0 = trap disabled (reset value) 1 = trap enabled	
21	SIWP1EN	Software trap enable selection of the 2nd I-bus watchpoint		
22	SIWP2EN	Software trap enable selection of the 3rd I-bus watchpoint		
23	SIWP3EN	Software trap enable selection of the 4th I-bus watchpoint		
24	DIWP0EN	Development port trap enable selection of the 1st I-bus watchpoint (read only bit)	0 = trap disabled (reset value) 1 = trap enabled	
25	DIWP1EN	Development port trap enable selection of the 2nd I-bus watchpoint (read only bit)		
26	DIWP2EN	Development port trap enable selection of the 3rd I-bus watchpoint (read only bit)		
27	DIWP3EN	Development port trap enable selection of the 4th I-bus watchpoint (read only bit)		
28	IFM	Ignore first match, only for I-bus breakpoints	0 = Do not ignore first match, used for “go to x” (reset value) 1 = Ignore first match (used for “continue”)	
29:31	ISCT_SER	RCPU serialize control and Instruction fetch show cycle	These bits control serialization and instruction fetch show cycles. See Table 23-27 for the bit definitions. NOTE: Changing the instruction show cycle programming starts to take effect only from the second instruction after the actual **mtspr** to ICTRL.	

1 Refer to Appendix A, “MPC562/MPC564 Compression Features,” for code compression-specific functionality.

2 MPC562/MPC564 only.

Table 23-27. ISCT_SER Bit Descriptions

Serialize Control (SER)	Instruction Fetch (ISCTL)	Functions Selected
0	00	RCPU is fully serialized and show cycles will be performed for all fetched instructions (reset value)
0	01	RCPU is fully serialized and show cycles will be performed for all changes in the program flow
0	10	RCPU is fully serialized and show cycles will be performed for all indirect changes in the program flow
0	11	RCPU is fully serialized and no show cycles will be performed for fetched instructions

Table 24-19. Public Messages Supported (continued)

Message Name	Minimum Packet Size (bits)	Maximum Packet Size (bits)	Packet Type	Packet Description	Direction
Program Trace — Indirect Branch Synchronization[2] Message (PTSM = 1)	6	6	Fixed	TCODE number = 12 (0xC)	From Device
	1	8	Variable	number of sequential instructions executed since last taken branch	
	1	23	Variable	full target address	
Data Trace — Data Write Synchronization Message	6	6	Fixed	TCODE number = 13 (0xD)	From Device
	1	1	Variable	number of messages canceled	
	1	25	Variable	full target address	
	8	32	Variable	data write value (8, 16, 32 bits)	
Data Trace — Data Read Synchronization Message	6	6	Fixed	TCODE number = 14 (0xE)	From Device
	1	1	Variable	number of messages canceled	
	1	25	Variable	full target address	
	8	32	Variable	data read value (8, 16, 32 bits)	
Watchpoint Message	6	6	Fixed	TCODE number = 15 (0xF)	From Device
	6	6	Fixed	number indicating watchpoint source	
Auxiliary Access — Device Ready for Upload/Download Message	6	6	Fixed	TCODE number = 16 (0x10)	From Device
Auxiliary Access — Upload Request Message	6	6	Fixed	TCODE number = 17 (0x11)	From Tool
	8	8	Fixed	opcode to enable selected configuration, status or data upload from MCU	
Auxiliary Access — Download Request Message	6	6	Fixed	TCODE number = 18 (0x12)	From Tool
	8	8	Fixed	opcode to enable selected configuration or data download to MCU	
	8	80	Variable	Depending upon opcode selected for download, information to be downloaded to device will vary.	
Auxiliary Access — Upload/Download Information Message	6	6	Fixed	TCODE number = 19 (0x13)	From Device / Tool
	8	80	Variable	1). For an access, depending on word size selected (SZ field in RWA register), variable-length packets of information (10, 18, or 34 bits) will be uploaded/downloaded from/to device. 2). Depending upon opcode selected for upload from internal READI registers, information to be uploaded to the device will vary.	

CONTROL BITS

See Table 19-24 for the PRAM Address Offset Map.

Figure D-9. NITC Parameters

D.8 Multiphase Motor Commutation (COMM)

The COMM function generates phase commutation signals for a variety of brushless motors, including three-phase brushless direct current motors. It derives the commutation state directly from the position decoded in FQD, eliminating the need for hall effect sensors.

The state sequence is implemented as a user-configurable state machine, providing a flexible approach with other general applications. A RCPU offset parameter is provided to allow the RCPU to advance or retard all swtiching angles on the fly. This feature is useful for torque maintenance at high speeds. See Freescale TPU Progamming Note *Multiphase Motor Commutation TPU Function (COMM), (TPUPN09/D)*.

Figure D-10 and Figure D-10 show all of the host interface areas for the COMM function.

CONTROL BITS

	NAME	OPTIONS	ADDRESSES
0 1 2 3	Channel Function Select	xxxx – FQD Function Number. Assigned during microcode assembly. See Table D-1	0x30YY0C – 0x30YY12
0 1	Host Sequence	00 – Primary Channel (Normal Mode) 01 – Secondary Channel (Normal Mode) 10 – Primary Channel (Fast Mode) 11 – Secondary Channel (Fast Mode)	0x30YY14 – 0x30YY16
0 1	Host Service Request	00 – No Host Service (Reset Condition) 01 – Not Used 10 – Read TCR1 11 – Initialize	0x30YY18 – 0x30YY1A
0 1	Channel Priority	00 – Disabled 01 – Low Priority 10 – Medium Priority 11 – High Priority	0x30YY1C – 0x30YY1E
0	Channel Interrupt Enable	x – Not Used	0x30YY0A
0	Channel Interrupt Status	x – Not Used	0x30YY20

PARAMETER RAM

ADDRESS OFFSETS	BITS 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	
0x30XXW0	EDGE_TIME	Param 0
0x30XXW2	POSITION_COUNT	Param 1
0x30XXW4	TCR1_VALUE	Param 2
0x30XXW6	CHAN_PINSTATE	Param 3
0x30XXW8	CORR_PINSTATE_ADDR	Param 4
0x30XXWA	EDGE_TIME_LSB_ADDR	Param 5
0x30XXWC		Param 6
0x30XXWE		Param 7

= Written By RCPU

= Written by RCPU and TPU

W = Channel Number

= Written By TPU

= Unused Parameters

For address offsets: XX=41 for TPU_A, 45 for TPU_B
YY=40 for TPU_A,
44 for TPU_B
See Table 19-24 for the PRAM Address Offset Map.

Figure D-22. FQD Parameters — Primary Channel

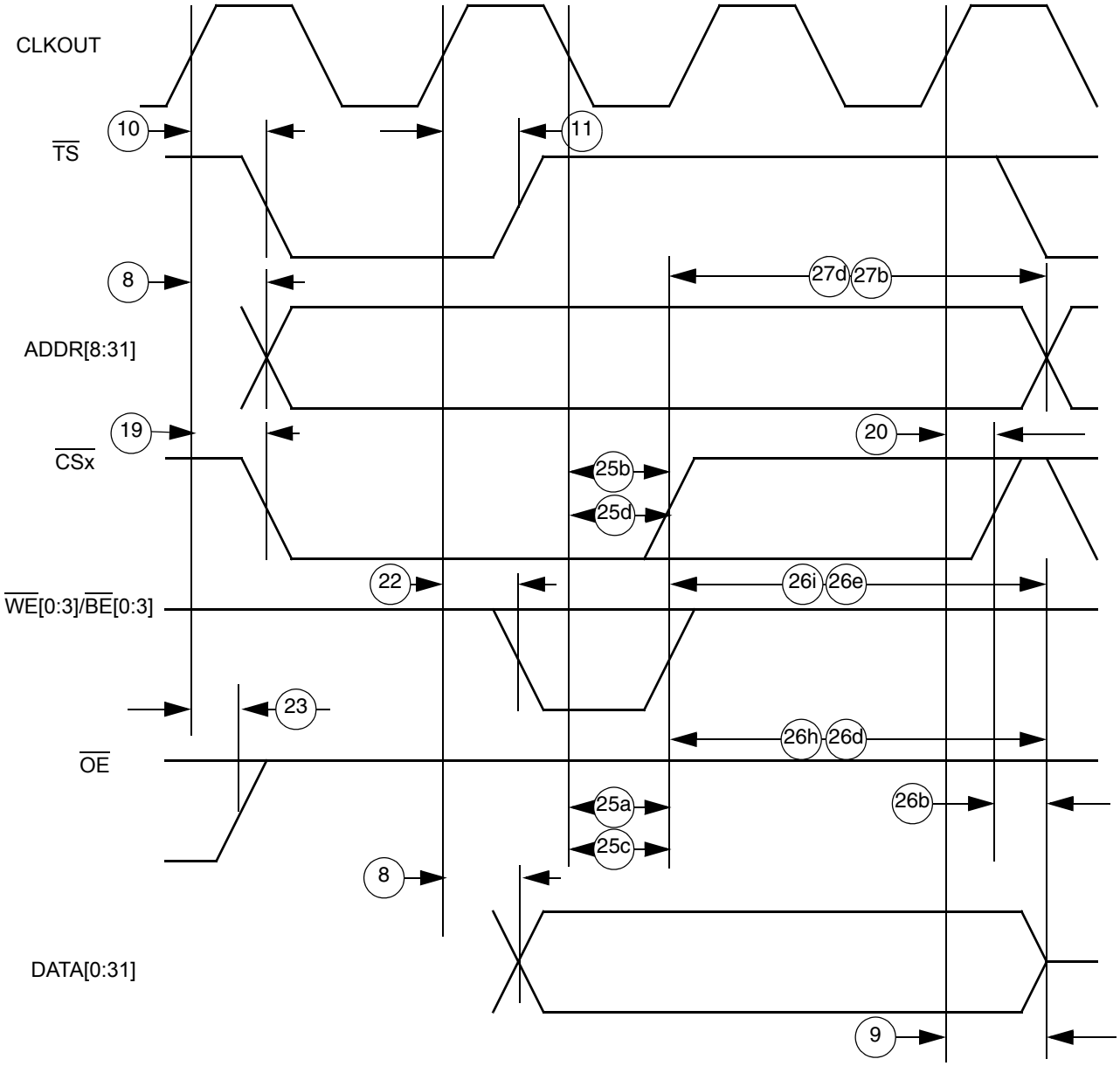

Figure F-24. External Bus Write Timing (GPCM Controlled – TRLX = '1', CSNT = '1')

F.15 QSMCM Electrical Characteristics

Table F-17. QSPI Timing

Note: ($T_A = T_L$ to T_H, 50 pF load on all QSPI pins unless otherwise noted)

Num	Function	Symbol	Min	Max	Unit
108	Operating Frequency[1] Master Slave	f_{OP}	 — —	 $f_{SYS}/4$ $f_{SYS}/4$	 Hz Hz
109	Cycle Time Master Slave	t_{QCYC}	 4*TC 4*TC	 510 * TC[2] —	 ns ns
110	Enable Lead Time Master Slave	t_{LEAD}	 2*TC 2*TC	 128 * TC —	 ns ns
111	Enable Lag Time Master Slave	t_{LAG}	 — 2*TC	 SCK/2 —	 ns ns
112	Clock (SCK) High or Low Time Master Slave[3]	t_{SW}	 2*TC– 60 2*TC– n	 255 * TC —	 ns ns
113	Sequential Transfer Delay Master Slave (Does Not Require Deselect)	t_{TD}	 17*TC 13*TC	 8192 * TC -	 ns ns
114	Data Setup Time (Inputs) Master Slave	t_{SU}	 30 20	 - -	 ns ns
115	Data Hold Time (Inputs) Master Slave	t_{HI}	 0 20	 - -	 ns ns
116	Slave Access Time	t_A	—	TC	ns
117	Slave MISO Disable Time	t_{DIS}	—	2 * TC	ns
118	Data Valid (after SCK Edge) Master Slave	t_V	 — —	 50 50	 ns ns
119	Data Hold Time (Outputs) Master Slave	t_{HO}	 0 0	 — —	 ns ns
120	SCK, MOSI, MISO Rise Time Input – Output – up to 50 pF, SLRC1 bit of PDMCR = “0” (slow) up to 200 pF, SLRC1 bit of PDMCR = “1” (fast) up to 200 pF, SLRC1 bit of PDMCR = "0" (slow)	 t_{rI} t_{RO} t_{RO} t_{RO}	 — — —	 1 200 21 300	 µs ns ns ns

Table G-10. Bus Operation Timing (continued)

Note: (V_{DD} = 2.6 V ± 0.1 V, V_{DDH} = 5.0 V ± 0.25 V, $T_A = T_L$ to T_H, 50 pF load unless noted otherwise)

	Characteristic	66 MHz		Unit
		Min	Max	
27d	$\overline{WE}$[0:3]/$\overline{BE}$[0:3] negated to ADDR[8:31] Invalid -GPCM- write access, TRLX='1', CSNT = '1'. $\overline{CS}$ negated to ADDR[8:31] Invalid -GPCM- write access, TRLX='1', CSNT = '1', ACS = 10,ACS = ='11', EBDF = 1	14.65	—	ns
28	ADDR[8:31], TSIZ[0:1], RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT Rising Edge. (Slave mode Setup Time)	3.5	—	ns
28a	Slave Mode D[0:31] valid to CLKOUT Rising Edge	3.7	—	ns
29	$\overline{TS}$ valid to CLKOUT Rising Edge (Setup Time)	2	—	ns
30	CLKOUT Rising Edge to $\overline{TS}$ Valid (Hold Time).	3.6	—	ns

1 The timing for $\overline{BR}$ output is relevant when the deviceMPC561/MPC563 is selected to work with external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC561/MPC563 is selected to work with internal bus arbiter.

2 The setup times required for $\overline{TA}$, $\overline{TEA}$, and $\overline{BI}$ are relevant only when they are supplied by the external device (and not the memory controller).

3 The maximum value of spec 8 for DATA[0:31] pins must be extended by 1.1 ns if the pins have been precharged to greater than V_{DDL}. This is the case if an external slave device on the bus is running at the max. value of VDATAPC. This is currently specified at 3.1 V. The 1.1 ns addition to spec 8 reflects the expected timing degradation for 3.1 V.

4 The device may be used without limitation in conjuction with 2.6 V external memories. Pre-discharge function is not available for 66-MHz operation.

5 The timing 27 refers to $\overline{CS}$ when ACS = '00' and to $\overline{WE}$[0:3]/$\overline{BE}$[0:3] when CSNT = '0'.

NOTE

The D[0:31] input timings 17 and 18 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

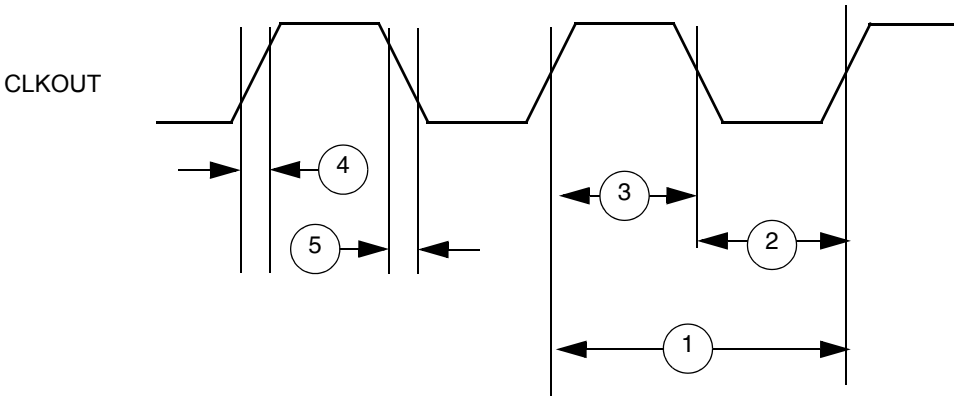

Figure G-10. CLKOUT Pin Timing