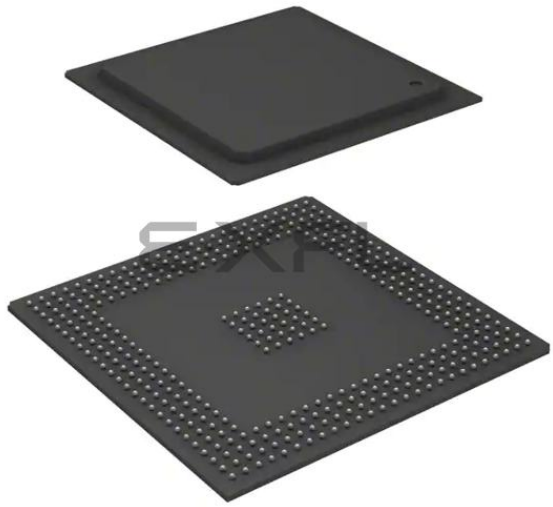

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Number of I/O	56
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 2.7V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
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Supplier Device Package	388-PBGA (27x27)
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Table 3-17. Instruction Set Summary (continued)

Mnemonic	Operand Syntax	Name
mullw (mullw. mullwo mullwo.)	rD,rA,rB	Multiply Low
nand (nand.)	rA,rS,rB	NAND
neg (neg. nego nego.)	rD,rA	Negate
nor (nor.)	rA,rS,rB	NOR
or (or.)	rA,rS,rB	OR
orc (orc.)	rA,rS,rB	OR with Complement
ori	rA,rS,UIMM	OR Immediate
oris	rA,rS,UIMM	OR Immediate Shifted
rfi	—	Return from Interrupt
rlwimi (rlwimi.)	rA,rS,SH,MB,ME	Rotate Left Word Immediate then Mask Insert
rlwinm (rlwinm.)	rA,rS,SH,MB,ME	Rotate Left Word Immediate then AND with Mask
rlwnm (rlwnm.)	rA,rS,rB,MB,ME	Rotate Left Word then AND with Mask
sc	—	System Call
slw (slw.)	rA,rS,rB	Shift Left Word
sraw (sraw.)	rA,rS,rB	Shift Right Algebraic Word
srawi (srawi.)	rA,rS,SH	Shift Right Algebraic Word Immediate
srw (srw.)	rA,rS,rB	Shift Right Word
stb	rS,d(rA)	Store Byte
stbu	rS,d(rA)	Store Byte with Update
stbux	rS,rA,rB	Store Byte with Update Indexed
stbx	rS,rA,rB	Store Byte Indexed
stfd	frS,d(rA)	Store Floating-Point Double
stfdu	frS,d(rA)	Store Floating-Point Double with Update
stfdux	frS,rB	Store Floating-Point Double with Update Indexed
stfdx	frS,rB	Store Floating-Point Double Indexed
stfiwx	frS,rB	Store Floating-Point as Integer Word Indexed
stfs	frS,d(rA)	Store Floating-Point Single
stfsu	frS,d(rA)	Store Floating-Point Single with Update
stfsux	frS,rB	Store Floating-Point Single with Update Indexed
stfsx	frS,r B	Store Floating-Point Single Indexed
sth	rS,d(rA)	Store Half-Word

Base Address Register (EIBADR)." This is the base address of a branch table. See Table 6-4 and Figure 4-3.

Each table entry must contain a branch absolute (ba) instruction to the first instruction of an interrupt service routine. Each table entry occupies two words (eight bytes) to support decompression on mode, where a branch instruction can be more than 32 bits long.

The memory space allocated for the external interrupt relocation table is up to 2 Kbytes. If part of the external interrupt relocation table entry is not used, it may be utilized for another purpose such as instruction code space or data space.

In order to activate the external interrupt relocation feature, the following steps are required:

1. Program the EIBADR register to the external interrupt branch table base address. See Section 4.6.2.5, "External Interrupt Relocation Table Base Address Register (EIBADR)."
2. Set the MSR[IP] bit.
3. Set the BBCMCR[EIR] bit. See Section 4.6.2.1, "BBC Module Configuration Register (BBCMCR)," for programming details.

NOTE

If both the enhanced external interrupt relocation and exception table relocation functions are activated simultaneously, the final external interrupt vector is defined by EEIR mechanism.

When the EEIR function is activated, any branch instruction execution with the 0xFFF0 0500 target address may cause unpredictable program execution.

Table 5-1. USIU Address Map

Address	Register
0x2F C000	USIU Module Configuration Register (SIUMCR) See Table 6-7 for bit descriptions.
0x2F C004	System Protection Control Register (SYPCR) See Table 6-15 for bit descriptions.
0x2F C008	Reserved
0x2F C00E[1]	Software Service Register (SWSR) See Table 6-16 for bit descriptions.
0x2F C010	Interrupt Pending Register (SIPEND).
0x2F C014	Interrupt Mask Register (SIMASK) See Section 6.2.2.2.4, “SIU Interrupt Mask Register (SIMASK),” for bit descriptions.
0x2F C018	Interrupt Edge Level Mask (SIEL) See Section 6.2.2.2.7, “SIU Interrupt Edge Level Register (SIEL),” for bit descriptions.
0x2F C01C	Interrupt Vector (SIVEC) See Section 6.2.2.2.8, “SIU Interrupt Vector Register (SIVEC),” for bit descriptions.
0x2F C020	Transfer Error Status Register (TESR) See Table 6-17 for bit descriptions.
0x2F C024	USIU General-Purpose I/O Data Register (SGPIODT1) See Table 6-23 for bit descriptions.
0x2F C028	USIU General-Purpose I/O Data Register 2 (SGPIODT2) See Table 6-24 for bit descriptions.
0x2F C02C	USIU General-Purpose I/O Control Register (SGPIOCR) See Table 6-25 for bit descriptions.
0x2F C030	External Master Mode Control Register (EMCR) See Table 6-13 for bit descriptions.
0x2F C038	Pads Module Configuration Register 2 (PDMCR2) See Table 2-6 for bit descriptions.
0x2F C03C	Pads Module Configuration Register (PDMCR) See Table 2-5 for bit descriptions.
0x2F C040	Interrupt Pend2 Register (SIPEND2) See Section 6.2.2.2.2, “SIU Interrupt Pending Register 2 (SIPEND2),” for bit descriptions.
0x2F C044	Interrupt Pend3 Register (SIPEND3) See Section 6.2.2.2.3, “SIU Interrupt Pending Register 3 (SIPEND3),” for bit descriptions.
0x2F C048	Interrupt Mask2 Register (SIMASK2) See Section 6.2.2.2.5, “SIU Interrupt Mask Register 2 (SIMASK2),” for details.
0x2F C04C	Interrupt Mask3 Register (SIMASK3) See Section 6.2.2.2.6, “SIU Interrupt Mask Register 3 (SIMASK3),” for details.
0x2F C050	Interrupt In-Service2 Register (SISR2) See Section 6.2.2.2.9, “Interrupt In-Service Registers (SISR2 and SISR3),” for details.
0x2F C054	Interrupt In-Service3 Register (SISR3) See Section 6.2.2.2.9, “Interrupt In-Service Registers (SISR2 and SISR3),” for details.

- Periodic Interrupt Timer (Section 6.1.9, “Periodic Interrupt Timer (PIT)”)—The SIU provides a timer to generate periodic interrupts for use with a real-time operating system or the application software. The PIT provides a period from 1 µs to 4 seconds with a four-MHz crystal or 200 ns to 0.8 ms with a 20-MHz crystal. The PIT function can be disabled.
- Software Watchdog Timer (Section 6.1.10, “Software Watchdog Timer (SWT)”)—The SWT asserts a reset or non-maskable interrupt, as selected by the system protection control register (SYPCR), if the software fails to service the SWT for a designated period of time (e.g., because the software is trapped in a loop or lost). After a system reset, this function is enabled with a maximum time-out period and asserts a system reset if the time-out is reached. The SWT can be disabled or its time-out period can be changed in the SYPCR. Once the SYPCR is written, it cannot be written again until a system reset.
- Freeze Support (Section 6.1.11, “Freeze Operation”)—The SIU allows control of whether the SWT, PIT, TB, DEC, and RTC should continue to run during freeze mode.
- Low Power Stop (Section 6.1.12, “Low Power Stop Operation”)—In low power modes, specific timers are frozen but others are not.

Figure 6-1 shows a block diagram of the system configuration and protection logic.

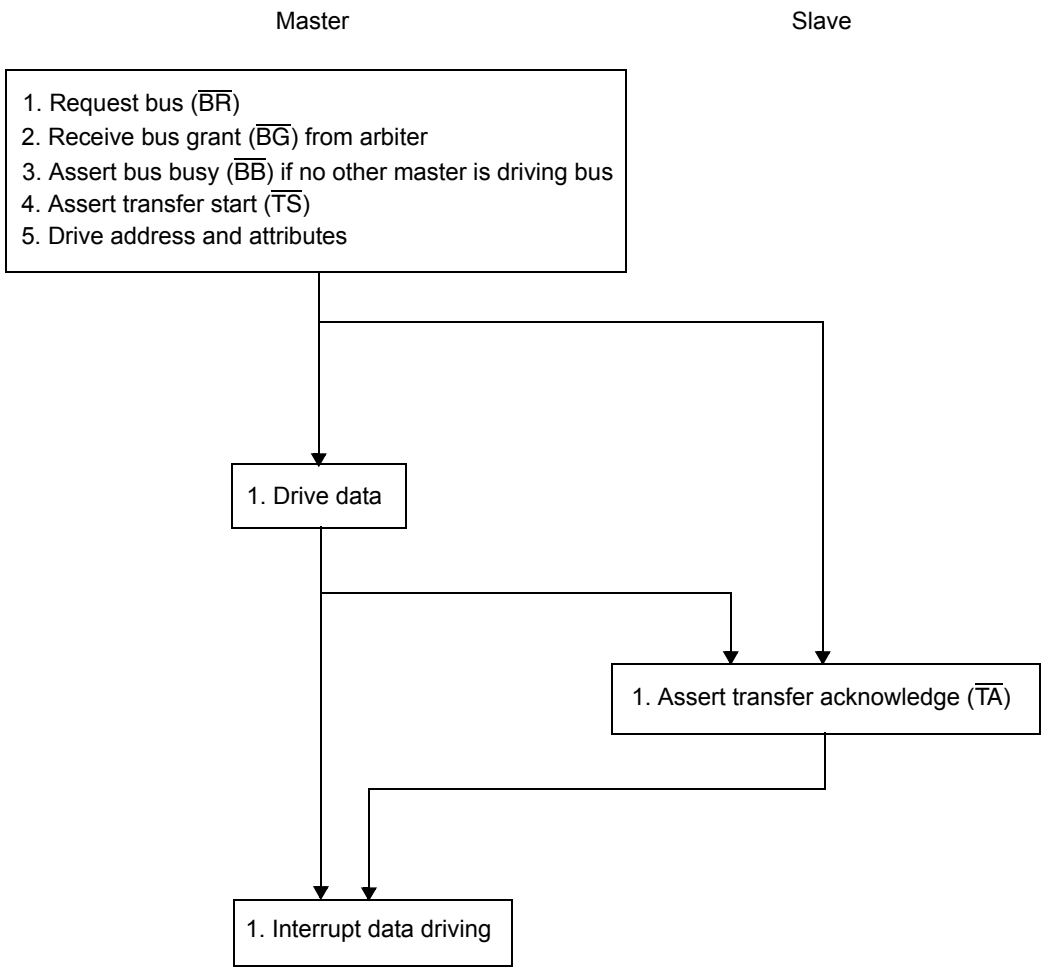


Figure 9-7. Basic Flow Diagram of a Single Beat Write Cycle

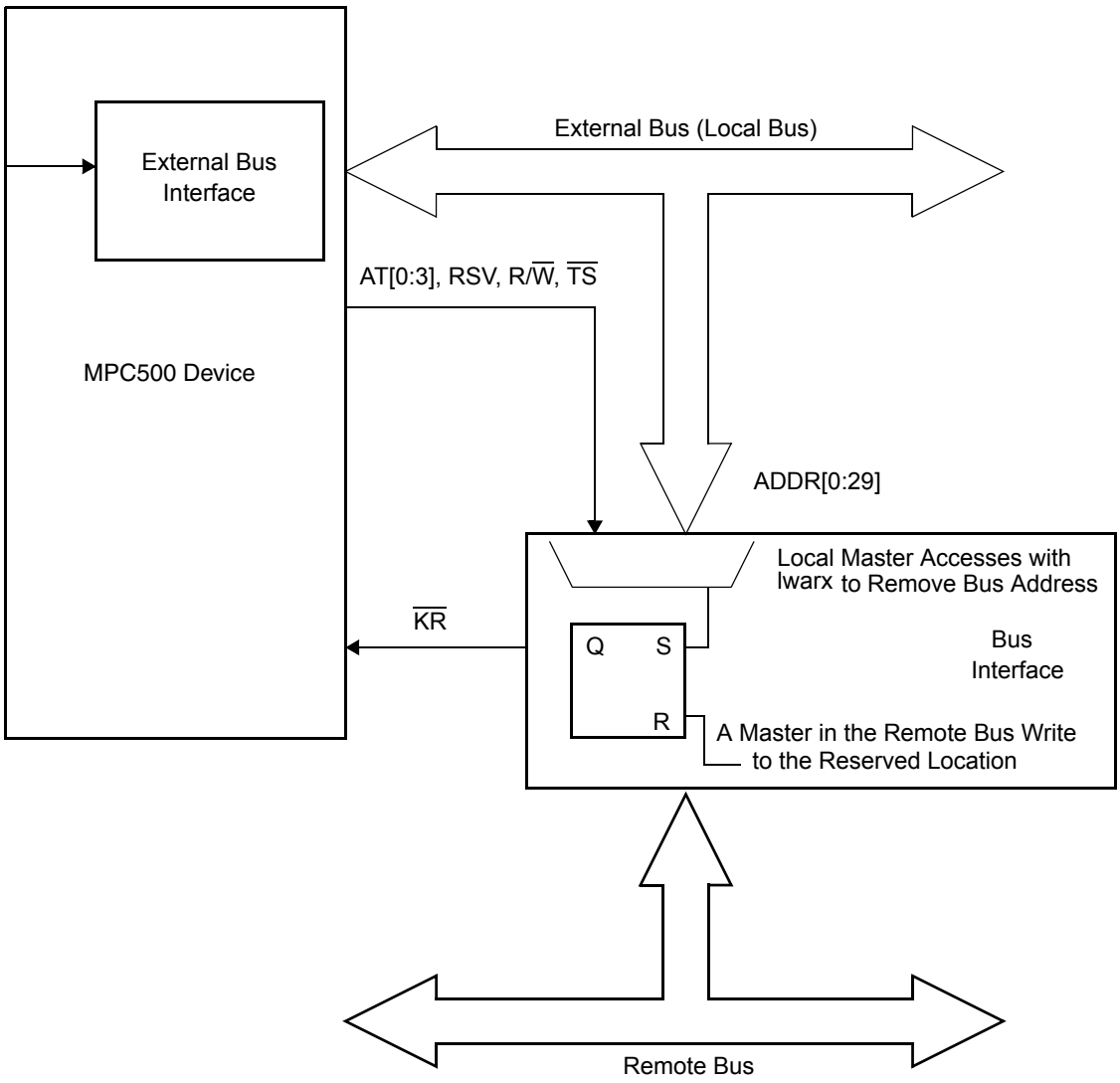


Figure 9-31. Reservation on Multi-level Bus Hierarchy

In this case, the bus interface block implements a reservation flag for the local bus master. The reservation flag is set by the bus interface when a load with reservation is issued by the local bus master and the reservation address is located on the remote bus. The flag is reset (negated) when an alternative master on the remote bus accesses the same location in a write cycle. If the MPC561/MPC563 begins a memory cycle to the previously reserved address (located in the remote bus) as a result of an stwcx instruction, the following two cases can occur:

- If the reservation flag is set, the buses interface acknowledges the cycle in a normal way
- If the reservation flag is reset, the bus interface should assert the $\overline{KR}$. However, the bus interface should not perform the remote bus write-access or abort it if the remote bus supports aborted cycles. In this case the failure of the stwcx instruction is reported to the RCPU.

13.2.2 Memory Map

The QADC64E occupies 1 Kbyte, or 512 16-bit entries, of address space. Ten 16-bit registers are control, port, and status registers, 64 16-bit entries are the CCW table, and 64 16-bit entries are the result table, and occupy 192 16-bit address locations because the result data is readable in three data alignment formats.

Each QADC64E module on the MPC561/MPC563 has its own memory space. Table 13-1 shows the memory map for QADC64E module A, it occupies 0x30 4800 to 0x30 4BFF. Table 13-2 displays the memory map for module B. Module B has the same offset scheme starting at 0x30 4C00. QADC64E B occupies 0x30 4C00 to 0x30 4FFF.

Table 13-1. QADC64E_A Address Map

Address	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15	Register
0x30 4800	STOP	FRZ					LOCK	FLIP	SUPV								Module Config.[1]
0x30 4802	TEST MODE																Test[1]
0x30 4804	IRL1						IRL2										Interrupt[1]
0x30 4806	PORTQA								PORTQB								Port Data
0x30 4808	DDRQA																Port Direction
0x30 480A	EMUX			TRG				PSH					PSA	PSL			Control 0
0x30 480C	CIE1	PIE1	SSE1	MQ1													Control 1
0x30 480E	CIE2	PIE2	SSE2	MQ2					RESUME	BQ2							Control 2
0x30 4810	CF1	PF1	CF2	PF2	TOR1	TOR2	QS			CWP							Status 0
0x30 4812			CWPQ1								CWPQ2						Status 1
0x30 4814-0x30 49FF	Reserved																
0x30 4A00-0x30 4A7F							P	BYP	IST	CHAN							CCWs
0x30 4A80-0x30 4AFF	0000 00						UNSIGNED RIGHT JUSTIFIED										Results
0x30 4B00-0x30 4B7F	SIGN	SIGNED LEFT JUSTIFIED								00 0000							Results
0x30 4B80 0x30 4BFF	UNSIGNED LEFT JUSTIFIED									00 0000							Results

[1] Registers are accessible only as supervisor data space

Table 15-12. QSPI Register Map (continued)

Access[1]	Address	MSB[2] 0	LSB 15
S/U	0x30 5180 – 0x30 51BF	Transmit Data RAM (32 half-words)	
S/U	0x30 51C0 – 0x30 51DF	Command RAM (32 bytes)	

1 S = Supervisor access only
S/U = Supervisor access only or unrestricted user access (assignable data space).

2 Eight-bit registers, such as SPCR3 and SPSR, are on 8-bit boundaries. 16-bit registers such as SPCR0 are on 16-bit boundaries.

To ensure proper operation, set the QSPI enable bit (SPE) in SPCR1 only after initializing the other control registers. Setting this bit starts the QSPI.

Rewriting the same value to a control register does not affect QSPI operation with the exception of writing NEWQP in SPCR2. Rewriting the same value to these bits causes the RAM queue pointer to restart execution at the designated location.

Before changing control bits, the QSPI should be halted. Writing a different value into a control register other than SPCR2 while the QSPI is enabled may disrupt operation. SPCR2 is buffered, preventing any disruption of the current serial transfer. After the current serial transfer is completed, the new SPCR2 value becomes effective.

15.6.1.1 QSPI Control Register 0 (SPCR0)

SPCR0 contains parameters for configuring the QSPI before it is enabled. The CPU has read/write access to SPCR0, but the QSPI has read access only. SPCR0 must be initialized before QSPI operation begins. Writing a new value to SPCR0 while the QSPI is enableddisrupts operation.

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	MSTR	WOMQ	BITS				CPOL	CPHA	SPBR							
$\overline{\text{SRESET}}$	0	0	0000				0	1	0000_0100							
Addr	0x30 5018															

Figure 15-11. QSPI Control Register 0 (SPCR0)

15.8.2.1 QSCI1 Control Register (QSCI1CR)

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	QTPNT				QTHFI	QBHFI	QTHEI	QBHEI	—	QTE	QRE	QTWE	QTSZ			
SRESET	0000_0000_0000_0000															
Addr	0x30 5028															

Figure 15-31. QSCI1 Control Register (QSCI1CR)

Table 15-32. QSCI1CR Bit Descriptions

Bits	Name	Description
0:3	QTPNT	Queue transmit pointer. QTPNT is a 4-bit counter used to indicate the next data frame within the transmit queue to be loaded into the SC1DR. This feature allows for ease of testability. This field is writable in test mode only; otherwise it is read-only.
4	QTHFI	Receiver queue top-half full interrupt. When set, QTHFI enables an SCI1 interrupt whenever the QTHF flag in QSCI1SR is set. The interrupt is blocked by negating QTHFI. This bit refers to the queue locations SCRQ[0:7]. 0 QTHF interrupt inhibited 1 Queue top-half full (QTHF) interrupt enabled
5	QBHFI	Receiver queue bottom-half full interrupt. When set, QBHFI enables an SCI1 interrupt whenever the QBHF flag in QSCI1SR is set. The interrupt is blocked by negating QBHFI. This bit refers to the queue locations SCRQ[8:15]. 0 QBHF interrupt inhibited 1 Queue bottom-half full (QBHF) interrupt enabled
6	QTHEI	Transmitter queue top-half empty interrupt. When set, QTHEI enables an SCI1 interrupt whenever the QTHE flag in QSCI1SR is set. The interrupt is blocked by negating QTHEI. This bit refers to the queue locations SCTQ[0:7]. 0 QTHE interrupt inhibited 1 Queue top-half empty (QTHE) interrupt enabled
7	QBHEI	Transmitter queue bottom-half empty interrupt. When set, QBHEI enables an SCI1 interrupt whenever the QBHE flag in QSCI1SR is set. The interrupt is blocked by negating QBHEI. This bit refers to the queue locations SCTQ[8:15]. 0 QBHE interrupt inhibited 1 Queue bottom-half empty (QBHE) interrupt enabled
8	—	Reserved
9	QTE	Queue transmit enable. When set, the transmit queue is enabled and the TDRE bit should be ignored by software. The TC bit is redefined to indicate when the entire queue is finished transmitting. When clear, the SCI1 functions as described in the previous sections and the bits related to the queue (Section 5.5 and its subsections) should be ignored by software with the exception of QTE. 0 Transmit queue is disabled 1 Transmit queue is enabled

TX_CONFIG_1 and TX_CONFIG_2 can only be written while PPM transmit mode is disabled (PPMPCR[ENTX] = 0). While transmit is enabled these registers read as 0x00 and writing them will return $\overline{\text{TEA}}$ (bus error access).

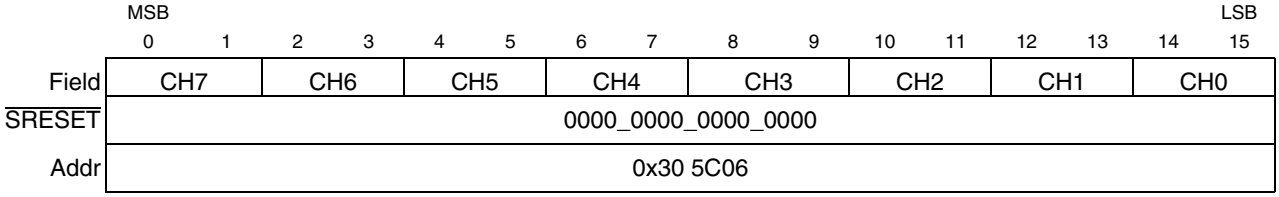


Figure 18-14. Transmit Configuration Register 1 (TX_CONFIG_1)

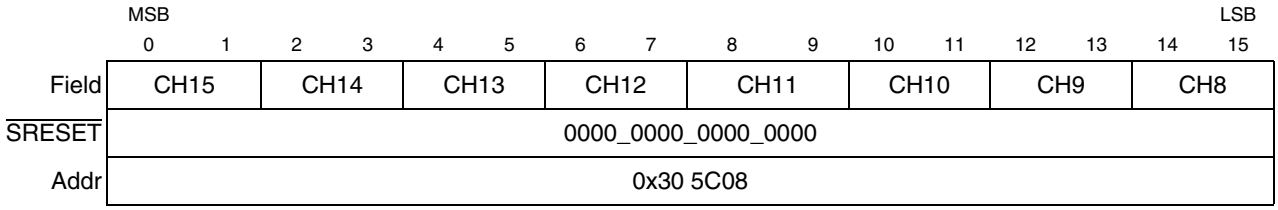


Figure 18-15. Transmit Configuration Register 2 (TX_CONFIG_2)

18.4.4 Receive Configuration Registers (RX_CONFIG_1 and RX_CONFIG_2)

The two receive configuration registers control which internal modules will receive data from the PPM. Each of the configuration registers contains eight separate 2-bit wide bit fields. Each of the 16 fields controls a multiplexer that selects a 1-bit channel from the PPM data receive register to an internal module. See Table 18-6 for more information on channel control and setting the channel values.

RX_CONFIG_1 and RX_CONFIG_2 can only be written while PPM receive mode is disabled (PPMPCR[ENRX] = 0). While receive mode is enabled these registers read as 0x00 and writing them will return $\overline{\text{TEA}}$ (bus error access).

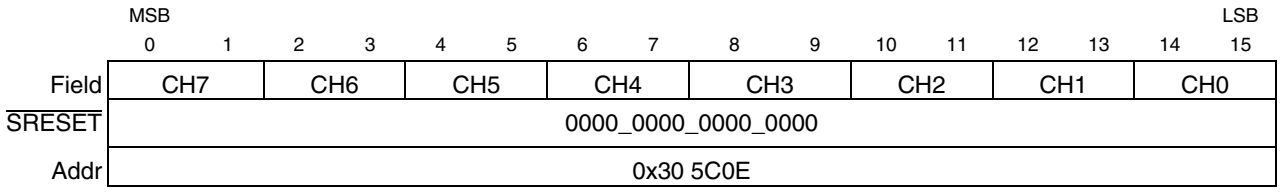


Figure 18-16. Receive Configuration Register 1 (RX_CONFIG_1)

19.4.1 TPU Module Configuration Register (TPUMCR)

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	STOP	TCR1P		TCR2P		EMU	T2CG	STF	SUPV	PSCK	TPU3	T2CSL	—			
SRESET	0	00		00		0	0	0	1	0	1	0	0000			
Addr	0x30 4000(TPU_A), 0x30 4400 (TPU_B)															

Figure 19-5. TPUMCR — TPU Module Configuration Register

Table 19-7. TPUMCR Bit Description

Bits	Name	Description
0	STOP	Low-power stop mode enable. If the STOP bit in TPUMCR is set, the TPU3 shuts down its internal clocks, shutting down the internal microengine. TCR1 and TCR2 cease to increment and retain the last value before the stop condition was entered. The TPU3 asserts the stop flag (STF) in TPUMCR to indicate that it has stopped. 0 Enable TPU3 clocks 1 Disable TPU3 clocks
1:2	TCR1P	Timer Count Register 1 prescaler control. TCR1 is clocked from the output of a prescaler. The prescaler divides its input by 1, 2, 4, or 8. This is a write-once field unless the PWOD bit in TPUMCR3 is set. 00 Divide by 1 01 Divide by 2 10 Divide by 4 11 Divide by 8 Refer to Section 19.3.8, “Prescaler Control for TCR1” for more information.
3:4	TCR2P	Timer Count Register 2 prescaler control. TCR2 is clocked from the output of a prescaler. The prescaler divides this input by 1, 2, 4, or 8. This is a write-once field unless the PWOD bit in TPUMCR3 is set. 00 Divide by 1 01 Divide by 2 10 Divide by 4 11 Divide by 8 Refer to Section 19.3.9, “Prescaler Control for TCR2” for more information.
5	EMU	Emulation control. In emulation mode, the TPU3 executes microinstructions from DPTRAM exclusively. Access to the DPTRAM via the IMB3 is blocked, and the DPTRAM is dedicated for use by the TPU3. After reset, this bit can be written only once. 0 TPU3 and DPTRAM operate normally 1 TPU3 and DPTRAM operate in emulation mode[1]
6	T2CG	TCR2 clock/gate control 0 TCR2 pin used as clock source for TCR2 1 TCR2 pin used as gate of DIV8 clock for TCR2 Refer to Section 19.3.9, “Prescaler Control for TCR2” for more information.
7	STF	Stop flag. 0 TPU3 is operating normally 1 TPU3 is stopped (STOP bit has been set)
8	SUPV	Supervisor data space 0 Assignable registers are accessible from user or supervisor privilege level 1 Assignable registers are accessible from supervisor privilege level only

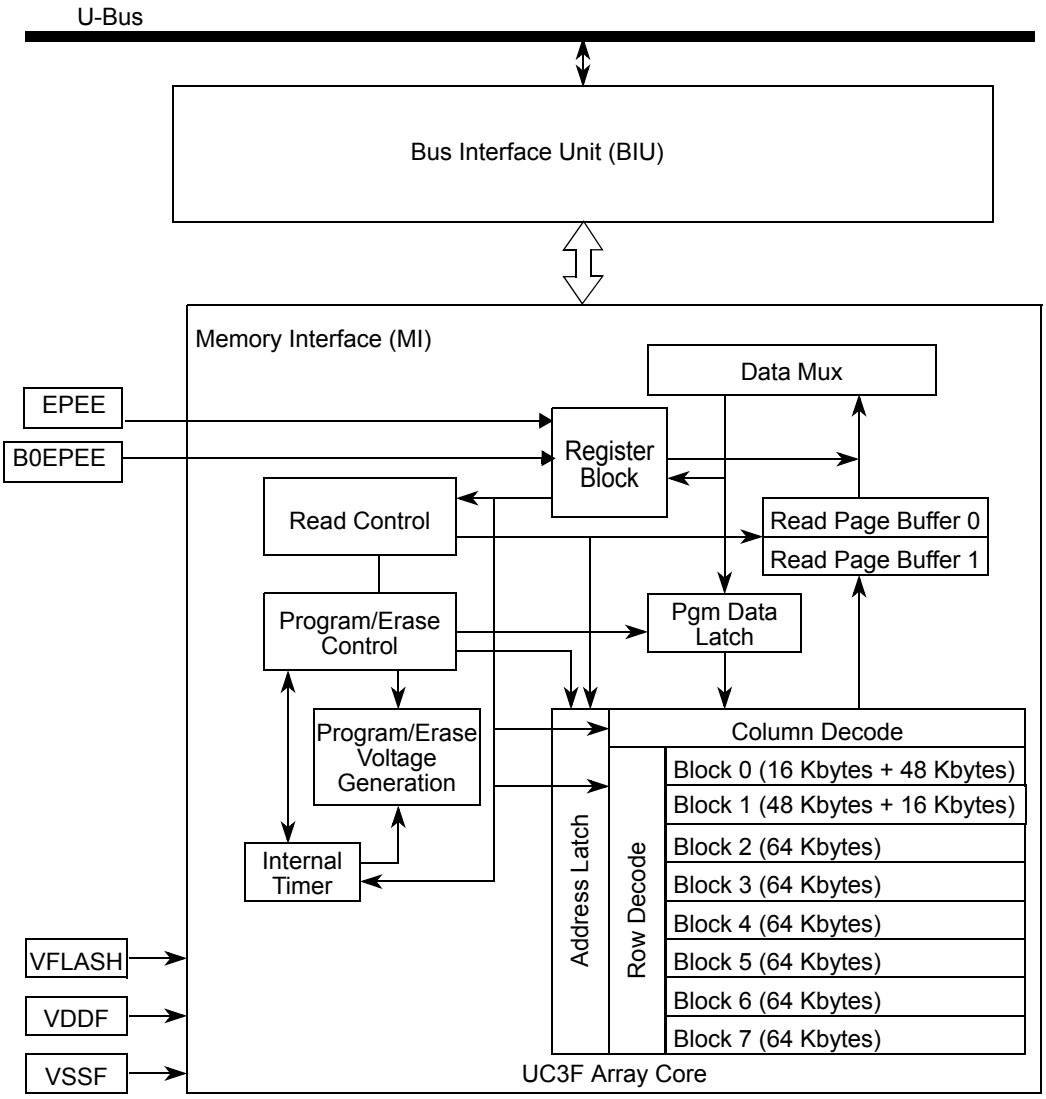


Figure 21-1. Block Diagram for a 512 Kbyte UC3F Module Configuration

The UC3F EEPROM module array is divided into array blocks to allow for independent erase, address attributes restrictions, and protection from program and erase for each array block. The size of a large array block in the UC3F module is fixed at 64 Kbytes. The size of a subdivided large block becomes the original large array block size minus 16 Kbytes (64 Kbytes – 16 Kbytes = 48 Kbytes). The size of the small block, which is the remainder of the large block, is always 16 Kbytes. The total UC3F EEPROM array is distributed into eight large blocks, two of which contain small blocks. Information is transferred to the UC3F EEPROM by long-word (64 bits), word (32 bits), half-word (16 bits), or byte (8 bits).

To improve system performance, each array read access retrieves 32 bytes of information. These 32 bytes may be copied into one of two read page buffers aligned to the low order addresses. The two read page buffers are independently updated by page management logic contained in the BIU which interfaces to the UC3F EEPROM module.

Table 21-3. UC3FMCR Bit Descriptions

Bits	Name	Description
0	STOP	Array stop control. Writes to the STOP bit have no effect while in program or erase operation (SES = 1). The STOP bit is always readable whenever the registers are enabled. When STOP = 1, the reset state of STOP is 1 and the UC3F array is disabled; internal circuits are switched into a low power state. The STOP bit may be used to implement low power standby modes or power management schemes. The UC3FMCR remains readable and writable when STOP = 1 so that the STOP bit may be deasserted. Attempts to program or erase the array while STOP = 1 have no effect. SES cannot be set to 1 when STOP = 1. When STOP = 0, the reset state of STOP is 0 and the UC3F array is enabled for accesses. All registers that were disabled with STOP = 1 are now enabled. A STOP recovery time of 1 μs is required for biases in the UC3F array to reach their appropriate states to resume normal operation. Operations to the UC3F array should be delayed for at least 1μs after clearing the STOP bit. 0 = UC3F array is enabled 1 = UC3F array is disabled (low-power mode)
1	$\overline{\text{LOCK}}$[1]	Lock control. The default reset state of $\overline{\text{LOCK}}$ is 1. This enables writing of all fields in the Flash registers. Once the $\overline{\text{LOCK}}$ bit has been asserted ($\overline{\text{LOCK}}$ = 0) in normal operating mode, the write-lock can only be disabled again by a reset. When the device is in background debug mode and CSC = 0, the $\overline{\text{LOCK}}$ bit may be written from a 0 to a 1. When the $\overline{\text{LOCK}}$ control bit is cleared to 0, the write-locked register bits: FIC, SUPV, SBSUPV[0:1], DATA, SBDATA, PROTECT, SBPROTECT, and SBEN[0:1] are locked. Writes to these bits while $\overline{\text{LOCK}}$ = 0 will have no effect. $\overline{\text{LOCK}}$ can be written to 0 once after reset when UC3FCTL[CSC] = 0 to allow protection of the write-locked register bits after initialization. **WARNING:** If the lock protection mechanism is enabled ($\overline{\text{LOCK}}$ = 0) before PROTECT and SBPROTECT are cleared, the device must use background debug mode to program or erase the UC3F EEPROM.
2	—	Reserved
3	FIC	Force information censorship. The default reset state of FIC is normal censorship operation (FIC = 0). The FIC bit is write protected by the $\overline{\text{LOCK}}$ bit and the UC3FCTL[CSC] bit. Writes will have no effect if $\overline{\text{LOCK}}$ = 0 or CSC = 1. Once FIC is set (FIC = 1), it cannot be cleared except by a reset. The FIC bit can be read whenever the registers are enabled. The FIC bit is a censorship emulation mode used to aid in the development of custom techniques for controlling the ACCESS bit without setting CENSOR[0:1] to the information censorship state. Using FIC to force information censorship allows testing of the hardware and software for setting ACCESS without setting CENSOR[0:1] = 11 and risk permanently setting the device into an unusable information censorship state. 0 = normal uc3f censorship operation 1 = forces the uc3f into information censorship mode
4	SIE	Shadow information enable. The default reset state of SIE is 0. The SIE bit is write protected in program operation (SES = 1 and PE = 0). The SIE bit can be read whenever the registers are enabled. When SIE = 1, normal array accesses are disabled, and the two shadow information rows are enabled. Array accesses are directed to the shadow row while SIE = 1. When an array location is read in this mode, only the lower 6 address bits are used to select which 64 bytes of the 512-byte shadow row are read. The upper address bits are not used for shadow row decoding. The read page buffer address monitor is reset whenever SIE is modified making the next UC3F array access an off page access. 0 = normal array access 1 = disables normal array access and selects the shadow information rows

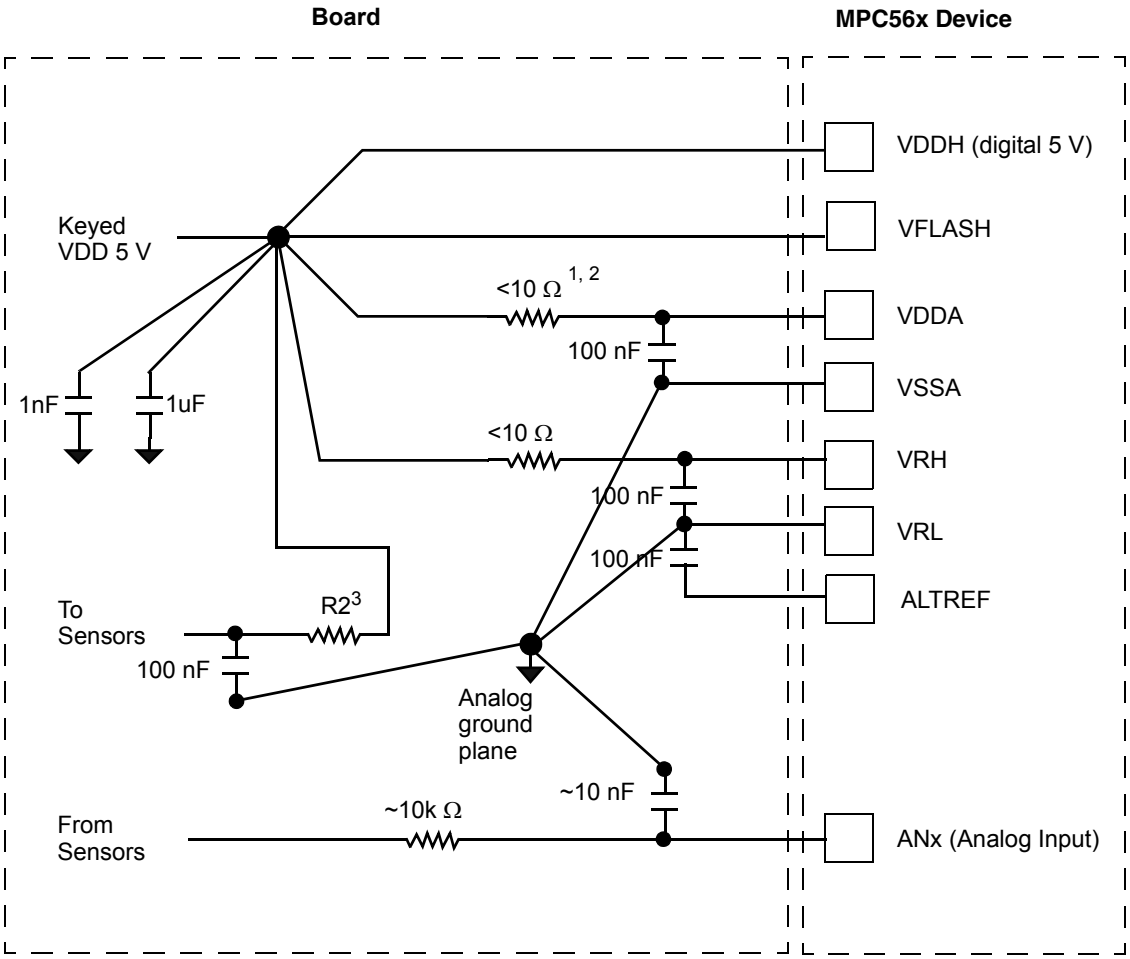
Table 25-2. MPC563 Boundary Scan Bit Definition (continued)

BSDL Bit	Cell Type	Pin/Port Name	BSDL Function	Safe Value	Control Cell	Disable Value	Disable Result	Pin Function	Pad Type
347	BC_2	*	controlr	0					
348	BC_7	ADDR_SGPIOA18	bidir	0	347	0	Z	IO	26v5vs
349	BC_2	*	controlr	0					
350	BC_7	ADDR_SGPIOA9	bidir	0	349	0	Z	IO	26v5vs
351	BC_2	*	controlr	0					
352	BC_7	ADDR_SGPIOA17	bidir	0	351	0	Z	IO	26v5vs
353	BC_2	*	controlr	0					
354	BC_7	ADDR_SGPIOA16	bidir	0	353	0	Z	IO	26v5vs
355	BC_2	*	controlr	0					
356	BC_7	ADDR_SGPIOA10	bidir	0	355	0	Z	IO	26v5vs
357	BC_2	*	controlr	0					
358	BC_7	ADDR_SGPIOA15	bidir	0	357	0	Z	IO	26v5vs
359	BC_2	*	controlr	0					
360	BC_7	ADDR_SGPIOA14	bidir	0	359	0	Z	IO	26v5vs
361	BC_2	*	controlr	0					
362	BC_7	ADDR_SGPIOA13	bidir	0	361	0	Z	IO	26v5vs
363	BC_2	*	controlr	0					
364	BC_7	ADDR_SGPIOA11	bidir	0	363	0	Z	IO	26v5vs
365	BC_2	*	controlr	0					
366	BC_7	ADDR_SGPIOA12	bidir	0	365	0	Z	IO	26v5vs
367	BC_2	*	controlr	0					
368	BC_7	BI_B_STS_B	bidir	0	367	0	Z	IO	26v
369	BC_2	*	controlr	0					
370	BC_7	BURST_B	bidir	0	369	0	Z	IO	26v
371	BC_2	*	controlr	0					
372	BC_7	BDIP_B	bidir	0	371	0	Z	IO	26v
373	BC_2	*	controlr	0					
374	BC_7	TA_B	bidir	0	373	0	Z	IO	26v
375	BC_2	*	controlr	0					
376	BC_7	TS_B	bidir	0	375	0	Z	IO	26v
377	BC_2	*	controlr	0					
378	BC_7	TSIZ1	bidir	0	377	0	Z	IO	26v
379	BC_2	*	controlr	0					
380	BC_7	TSIZ0	bidir	0	379	0	Z	IO	26v
381	BC_2	*	controlr	0					
382	BC_7	TEA_B	bidir	0	381	0	Z	IO	26v

Table 25-2. MPC563 Boundary Scan Bit Definition (continued)

BSDL Bit	Cell Type	Pin/Port Name	BSDL Function	Safe Value	Control Cell	Disable Value	Disable Result	Pin Function	Pad Type
383	BC_2	*	internal	1					
384	BC_2	OE_B	output2	1				O	26v
385	BC_2	*	controlr	0					
386	BC_7	RD_WR_B	bidir	0	385	0	Z	IO	26v
387	BC_2	*	internal	1					
388	BC_2	CS3_B	output2	1				O	26v
389	BC_2	*	internal	1					
390	BC_2	CS2_B	output2	1				O	26v
391	BC_2	*	internal	1					
392	BC_2	CS1_B	output2	1				O	26v
393	BC_2	*	internal	1					
394	BC_2	CS0_B	output2	1				O	26v
395	BC_2	*	internal	1					
396	BC_2	WE_B_AT3	output2	1				O	26v
397	BC_2	*	internal	1					
398	BC_2	WE_B_AT2	output2	1				O	26v
399	BC_2	*	internal	1					
400	BC_2	WE_B_AT1	output2	1				O	26v
401	BC_2	*	internal	1					
402	BC_2	WE_B_AT0	output2	1				O	26v
403	BC_2	*	controlr	0					
404	BC_7	BR_B_VF1_IWP2	bidir	0	403	0	Z	IO	26v
405	BC_2	*	controlr	0					
406	BC_7	BG_B_VF0_LWP1	bidir	0	405	0	Z	IO	26v
407	BC_2	*	controlr	0					
408	BC_7	BB_B_VF2_IWP3	bidir	0	407	0	Z	IO	26v
409	BC_2	*	controlr	0					
410	BC_7	SGPIOC7_IRQOUT_B_LWP0	bidir	0	409	0	Z	IO	26v
411	BC_2	*	controlr	0					
412	BC_7	IRQ1_B_RSV_B_SGPIOC1	bidir	0	411	0	Z	IO	26v5vs
413	BC_2	*	controlr	0					
414	BC_7	IRQ0_B_SGPIOC0_MDO4	bidir	0	413	0	Z	IO	26v5vs
415	BC_2	*	controlr	0					
416	BC_7	IRQ2_B_CR_B_SGPIOC2_IMDO5_MTS_B	bidir	0	415	0	Z	IO	26v

Figure C-1. MPC561/MPC563 Power Distribution Diagram — 2.6 V



1. 10 ohms is recommended because I_{REF} (max) is 250 μA per QADC64. 10 Ohm x 2 modules x 250 μA = 5 mV (approximately one count, or one LSB)
2. The QADC64 circuit design allows for VDDA being less than VRH with a value of up to 10 ohms in this RC filter.
3. This size of resistor R_2 depends on the sensor load current. It should be sized to match the voltage at VRH.

Figure C-2. Power Distribution Diagram — 5 V and Analog

active, these performance figures will be degraded; however, the scheduler assures that the worst-case latency in any TPU3 application can be closely approximated. TPU3 reference manual guidelines and information given in the SIOP-state timing table should be used to perform an analysis on any proposed TPU3 application that appears to approach the TPU's performance limits.

Table D-4. SIOP State Timing[1]

State Number and Name	Max. RCPU Clock Cycles	Number of RAM Accesses by TPU3
S1 SIOP_INIT HSQ = X0 X1	 28 38	 7 7
S2 DATA_OUT HSQ = X0 X1	 14 24	 4 4
S3 DATA_IN HSQ = 0X 1X	 14 28	 4 6

1 Execution times do not include the time slot transition time (TST = 10 or 14 RCPU clocks).

D.20.3.1 XFER_SIZE Greater Than 16

XFER_SIZE is normally programmed to be in the 1- to 16-bit range to match the size of SIOP_DATA, and has thus been shown as a 5-bit value in the host interface diagram. However, the TPU3 actually uses all 16 bits of the XFER_SIZE parameter when loading BIT_COUNT. In some unusual circumstances this can be used to an advantage. If an input device is producing a data stream of greater than 16 bits then manipulation of XFER_SIZE will allow selective capturing of the data. In clock-only mode, the extended XFER_SIZE can be used to generate up to 0xFFFF clocks.

D.20.3.2 Data Positioning

As stated above, the TPU3 does not "justify" the data position in SIOP_DATA. Therefore, in the case of a byte transfer, the data output will be sourced from one byte and the data input will shift into the other byte. This is true for all data sizes except 16 bits, in which case the full SIOP_DATA register is used for both data output and input.

D.20.3.3 Data Timing

In the example given in Figure D-33, the data output transitions are shown as being completely synchronous with the relevant clock edge and it is assumed that the data input is latched exactly on the opposite clock edge. This is the simplest way to show the examples, but is not strictly true. Since the TPU3 is a multi-tasking system, and the data channels are manipulated directly by microcode software while servicing the clock edge, there is a finite delay between the relevant clock edge and the data-out being valid or the data-in being latched. This delay is equivalent to the latency in servicing the clock channel due to other TPU3 activity and is shown as 'Td' in the timing diagram. Td is the delay between the clock edge and the next output data being valid and also the delay between the opposite clock edge and the input data being read. For the vast majority of applications, the delay Td will not present a problem and can be ignored. Only for a system which heavily loads the TPU3 should the worst case latency be calculated for

F.8 Power-Up/Down Sequencing

The supply symbols used in this section are described in Table F-9.

Table F-9. Power Supply Pin Groups

Symbol	Types of Power Pins
V_{DDH} (High Voltage Supply Group)	Supply to the 5-V pads for output driver (V_{DDH})
	Supply to the analog (QADC64E) circuitry (V_{DDA})
	High voltage supply to the flash module (V_{FLASH})[1]
V_{DDL} (Low Voltage Supply Pins)	Supply to low voltage pad drivers (QVDDL, NVDDL)
	Supply to all low voltage internal logic (V_{DD})
	Supply to low voltage flash circuitry (V_{DDF})[1]
	Supply to system PLL
V_{DDKA} (Low Voltage Keep-Alive Supply Pins[2]	Supply to IRAMSTBY
	Supply to oscillator and other circuitry for keep-alive functions (KAPWR).

1 These power supplies are only available on the MPC563 and MPC564.

2 Any supply in the V_{DDKA} group can be powered with the V_{DDL} if the function which it supplies is not required during “Keep-alive.”

There are two power-up/down options. Choosing which one is required for an application will depend upon circuitry connected to 2.6-V compliant pins and dual 2.6-V/5-V compliant pins. Power-up/down option A is required if 2.6-V compliant pins and dual 2.6-V/5-V compliant pins are connected to the 5-V supply with a pull-up resistor or driven by 5-V logic during power-up/down. In applications for which this scenario is not true the power-up/down option B may be implemented. Option B is less stringent and easier to ensure over a variety of applications.

Refer to Table 2-1 for a list of 2.6 V and dual 2.6V/5 V compliant pins.

The power consumption during power-up/down sequencing will stay below the operating power consumption specifications when following these guidelines.

NOTE:

The V_{DDH} ramp voltage should be kept below 50V/ms and the V_{DDL} ramp rate less that 25V/ms.

F.8.1 Power-Up/Down Option A

The Option A power-up sequence (excluding V_{DDKA}) is

1. $V_{DDH} \leq V_{DDL} + 3.1$ V (V_{DDH} cannot lead V_{DDL} by more than 3.1 V)
2. $V_{DDH} \geq V_{DDL} - 0.5$ V (V_{DDH} cannot lag V_{DDL} by more than 0.5 V)

The first step in the sequence is required is due to gate-to-drain stress limits for transistors in the pads of 2.6-V compliant pins and dual 2.6-V/5-V compliant pins. Damage can occur if gate-to-drain voltage potential is greater than 3.1 V. This is only a concern at power-up/down. The second step in the sequence

W

X

Z