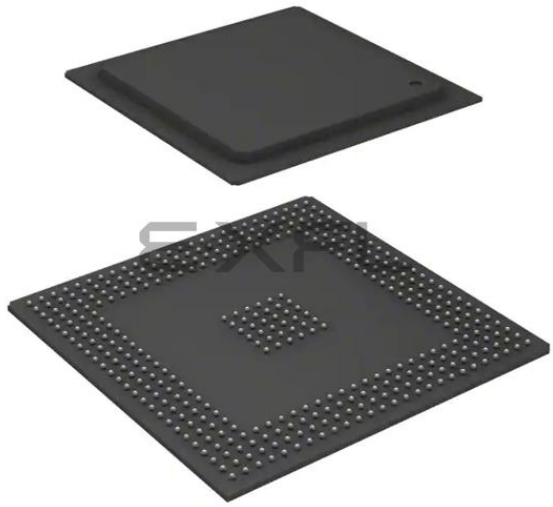

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Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	56
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 2.7V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	388-BBGA
Supplier Device Package	388-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc564mzp66r2

Contents

Table 3-3. Development Support SPRs[1] (continued)

SPR Number (Decimal)	Special-Purpose Register
158	I-bus Support Control Register (ICTRL) See Table 23-26 for bit descriptions.
159	Breakpoint Address Register (BAR) See Table 23-28 for bit descriptions.
630	Development Port Data Register (DPDR) See Section 23.6.13, "Development Port Data Register (DPDR)," for bit descriptions.

1 All development-support SPRs are implementation-specific.

Unless otherwise noted, reserved fields should be written with a zero when written and return zero when read. An exception to this rule is XER[16:23]; see Section 3.7.5, "Integer Exception Register (XER)." These bits are set to the value written to them and return that value when read.

3.7 User Instruction Set Architecture (UISA) Register Set

The UISA registers can be accessed by either user- or supervisor-level instructions. The general-purpose registers are accessed through instruction operands.

3.7.1 General-Purpose Registers (GPRs)

Integer data is manipulated in the integer unit's thirty-two 32-bit GPRs, shown below. These registers are accessed as source and destination registers through operands in the instruction syntax.

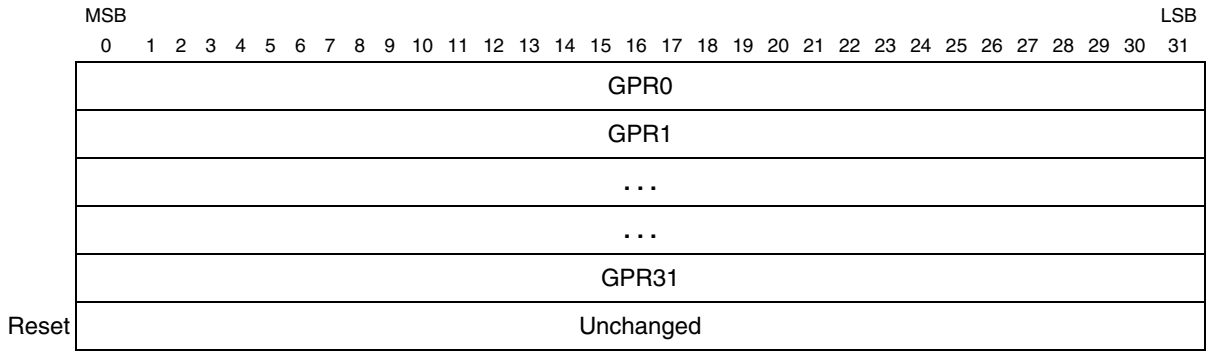


Figure 3-4. General-Purpose Registers (GPRs)

3.7.2 Floating-Point Registers (FPRs)

The PowerPC ISA architecture provides 32 64-bit FPRs. These registers are accessed as source and destination registers through operands in floating-point instructions. Each FPR supports the double-precision, floating-point format. Every instruction that interprets the contents of an FPR as a

Table 3-25. Register Settings following a Machine Check Exception (continued)

Register Name	Bits	Description
Machine State Register (MSR)	IP	No change
	ME	No change
	LE	Bit is copied from ILE
	DCMPEN	This bit is set according to (BBCMCR[EN_COMP] AND BBCMCR[EXC_COMP])
	Other	Cleared to 0
Data/Storage Interrupt Status Register (DSISR)[3]	0:14	Cleared to 0
	15:16	Set to bits [29:30] of the instruction if X-form and to 0b00 if D-form
	17	Set to bit 25 of the instruction if X-form and to Bit 5 if D-form
	18:21	Set to bits [21:24] of the instruction if X-form and to bits [1:4] if D-form
	22:31	Set to bits [6:15] of the instruction
Data Address Register (DAR)[3]	All	Set to the effective address of the data access that caused the interrupt

1 If the exception occurs due to a data error caused by a Load/Store instruction and the processor in Decompression On mode, the SRR0 register will contain the address of the Load/Store instruction in compressed format. If the exception occurs due to an instruction fetch in Decompression On mode, the SRR0 register will contain an indeterminate value.

2 This bit is loaded from the corresponding bit in the MSR when an interrupt is taken. The appropriate bit in MSR is loaded from this bit when an RFI is executed.

3 DSISR and DAR registers are only updated when the machine check exception is caused by a data access violation.

when a machine check exception is taken, instruction execution resumes at offset 0x0200 from the base address indicated by MSR[IP].

3.15.4.3 Data Storage Exception (0x0300)

A data storage exception is never generated by the RCPU. The software may branch to this location as a result of implementation-specific data storage protection error exception.

3.15.4.4 Instruction Storage Exception (0x0400)

An instruction storage interrupt is never generated by them RCPU. The software may branch to this location as a result of an implementation-specific instruction storage protection error exception.

3.15.4.5 External Interrupt (0x0500)

The external interrupt exception is taken on assertion of the internal $\overline{\text{IRQ}}$ line to the RCPU, that is driven by on-chip interrupt controller. The interrupt may be caused by the assertion of an external $\overline{\text{IRQ}}$ signal, by a USIU timer, or by an internal chip peripheral. Refer to Section 6.1.4, “Enhanced Interrupt Controller,” for more information on the interrupt controller.

Section 4.6.2.3, “Region Attribute Registers (MI_RA[0:3]),” and Section 4.6.2.4, “Global Region Attribute Register (MI_GRA)” for details.

4.6 BBC Programming Model

4.6.1 Address Map

The BBC consists of three separately addressable sections within the internal chip address space:

1. BBC and IMPU control registers. These are mapped in the SPR registers area and may be programmed by using the RCPU mtspr/mfspr instructions.
2. Decompressor vocabulary RAM (DECRAM). The DECRAM array occupies the 2-Kbyte physical memory (8 Kbytes of the MPC561/MPC563 address space is allocated for DECRAM).
3. Decompressor class configuration registers (DCCR) block. It consists of 15 decompression class configuration registers. These registers are available for word wide read/write accesses through U-bus. The registers occupy a 64-byte physical block (8-Kbyte chip address space is allocated for the register block).

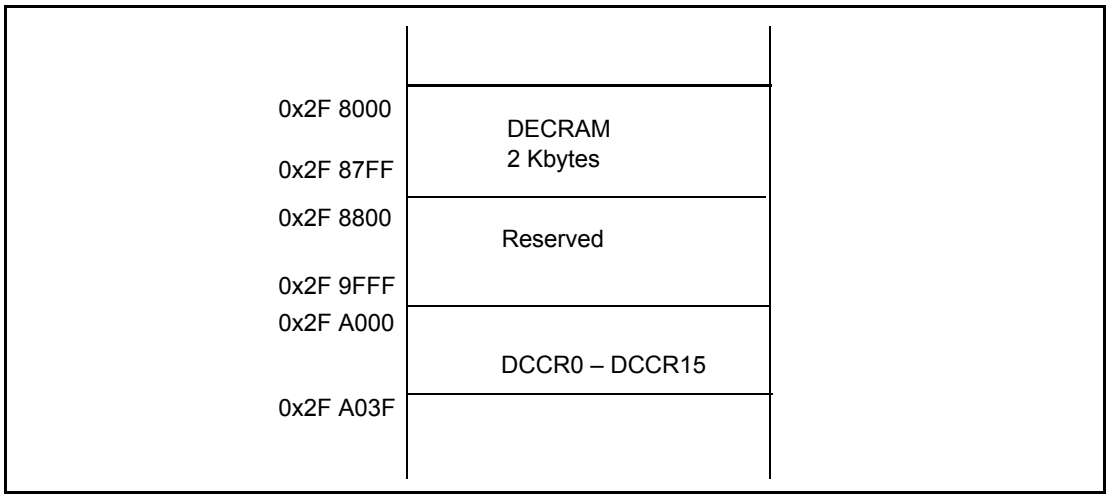


Figure 4-6. MPC561/MPC563 Memory Map

4.6.1.1 BBC Special Purpose Registers (SPRs)

Table 4-3. BBC SPRs

SPR Number (Decimal)	Address for External Master Access (Hex)	Register Name
528	0x2100	IMPU Global Region Attribute Register (MI_GRA). See Table 4-8 for bits descriptions.
529	0x2300	External Interrupt Relocation Table Base Address Register (EIBADR). See Table 4-9 for bits descriptions.
560	0x2110	BBC Module Configuration Register (BBCMCR). See Table 4-4 for bits descriptions

- The Internal PLL enters the lock state and the system clock is active.
- The PORESET pin is negated.

If limp mode is enabled, the internal PLL is not required to be locked before the chip exits power-on reset.

The internal MODCK[1:3] values are sampled at the rising edge of PORESET. After exiting the power-on reset state, the MPC561/MPC563 continues to drive the HRESET and SRESET pins for 512 system clock cycles. When the timer expires (after 512 cycles), the configuration is sampled from data bus pins, if required (see Section 7.5.1, "Hard Reset Configuration") and the MPC561/MPC563 stops driving the HRESET and SRESET pins.

The PORESET pin has a glitch detector to ensure that low spikes of less than 20 ns are rejected. The internal PORESET signal asserts only if the PORESET pin asserts for more than 100 ns.

7.1.2 Hard Reset

HRESET (hard reset) is an active low, bidirectional I/O pin. The MPC561/MPC563 can detect an external assertion of HRESET only if it occurs while the MPC561/MPC563 is not asserting HRESET.

When the MPC561/MPC563 detects assertion of the external HRESET pin or a cause to assert the internal HRESET line is detected, the chip starts to drive the HRESET and SRESET for 512 cycles. When the timer expires (after 512 cycles) the configuration is sampled from data pins (refer to Section 7.5.1, "Hard Reset Configuration") and the chip stops driving the HRESET and SRESET pins. An external pull-up resistor should drive the HRESET and SRESET pins high. After detecting the negation of HRESET or SRESET, the MPC561/MPC563 waits 16 clock cycles before testing the presence of an external hard or soft reset.

The HRESET pin has a glitch detector to ensure that low spikes of less than 20 ns are rejected. The internal HRESET will be asserted only if HRESET is asserted for more than 100 ns.

The HRESET is an open collector type pin.

7.1.3 Soft Reset

SRESET (soft reset) is an active low, bidirectional I/O pin. The MPC561/MPC563 can only detect an external assertion of SRESET if it occurs while the MPC561/MPC563 is not asserting SRESET.

When the MPC561/MPC563 detects the assertion of external SRESET or a cause to assert the internal SRESET line, the chip starts to drive the SRESET for 512 cycles. When the timer expires (after 512 cycles) the debug port configuration is sampled from the DSDI and DSCK pins and the chip stops driving the SRESET pin. An external pull-up resistor should drive the SRESET pin high. After the MPC561/MPC563 detects the negation of SRESET, it waits 16 clock cycles before testing the presence of an external soft reset.

The SRESET is an open collector type pin.

7.1.4 Loss of PLL Lock

If the PLL detects a loss of lock, erroneous external bus operation will occur if synchronous external devices use the MPC561/MPC563 input clock. Erroneous operation could also occur if devices with a PLL

memory to three-state the bus before the bus discharge is initiated. EHTR has a slight performance reduction impact since it adds a clock gap between some read and write cycles.

NOTE

EHTR also adds one idle clock for two consecutive read cycles from different memory banks.

NOTE

The pre-disharge will not occur, when using multiple processors with a common bus accessing an external device, if the processor that initiates a read is different from the processor that initiated the previous write. Perform a write to the external device to discharge the external bus, or read a value of 0x0 from the external device, prior to accessing another MCU on the same bus.

9.5.3.1 Operating Conditions

Pre-discharge mode should be enabled in the following cases:

- When external devices can charge the data bus to a higher voltage level than 3.1 volts
- And when one or more of the following occurs:
  - The MPC561/MPC563 uses write accesses to any external memory
  - Data show cycles are enabled
  - Instruction show cycles are enabled in code compression mode (MPC562/MPC564 only)

NOTE

In the case of code compression program tracking (3rd case above), the PREDIS_EN bit should only be set when program tracking is not required since pre-discharge mode overwrites the compression show cycles data. The user should not set PREDIS_EN bit when program tracking is required on development system, and set PREDIS_EN bit on the production version. EHTR can always be set to keep the same system performance during development, and production phases.

9.5.3.2 Initialization Sequence

Systems that require pre-discharge operation should include the following steps:

- Execute boot sequence
- Set EHTR bit in all relevant memory banks during the memory controller initialization phase (configure ORx, and BRx) if it is required to extend the time between read cycles, and pre-discharge phase of write cycles.
- Set PREDIS_EN in PDMCR2 register
- Start to write data to external devices

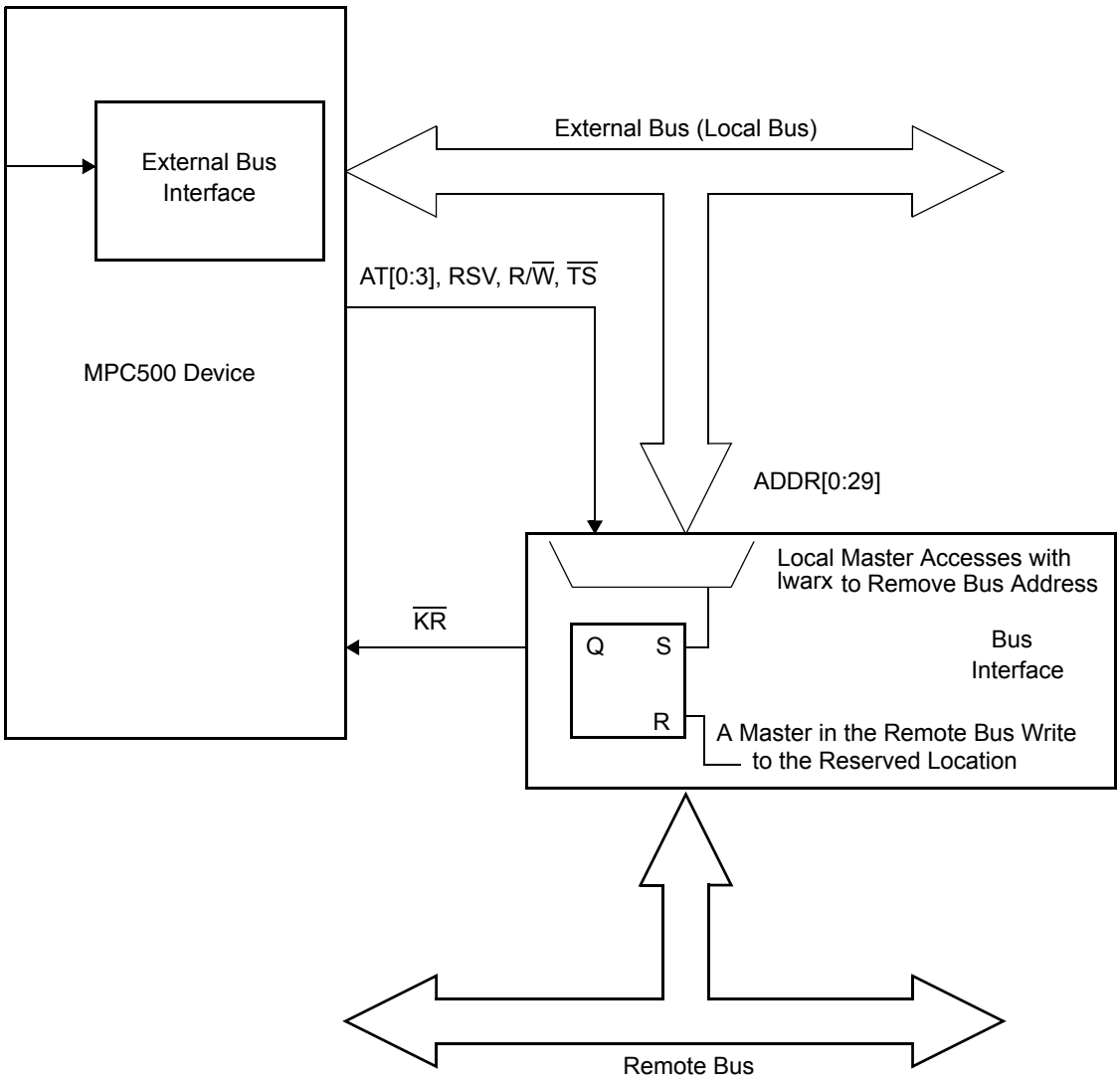


Figure 9-31. Reservation on Multi-level Bus Hierarchy

In this case, the bus interface block implements a reservation flag for the local bus master. The reservation flag is set by the bus interface when a load with reservation is issued by the local bus master and the reservation address is located on the remote bus. The flag is reset (negated) when an alternative master on the remote bus accesses the same location in a write cycle. If the MPC561/MPC563 begins a memory cycle to the previously reserved address (located in the remote bus) as a result of an stwcx instruction, the following two cases can occur:

- If the reservation flag is set, the buses interface acknowledges the cycle in a normal way
- If the reservation flag is reset, the bus interface should assert the $\overline{KR}$. However, the bus interface should not perform the remote bus write-access or abort it if the remote bus supports aborted cycles. In this case the failure of the stwcx instruction is reported to the RCPU.

9.5.11.2 Termination Signals Protocol Summary

Table 9-9 summarizes how the MPC561/MPC563 recognizes the termination signals provided by the slave device that is addressed by the initiated transfer.

Table 9-9. Termination Signals Protocol

$\overline{\text{TEA}}$	$\overline{\text{TA}}$	$\overline{\text{RETRY}}$	Action
Asserted	X	X	Transfer error termination
Negated	Asserted	X	Normal transfer termination
Negated	Negated	Asserted	Retry transfer termination

9.5.12 Bus Operation in External Master Modes

When an external master takes ownership of the external bus and the MPC561/MPC563 is programmed for external master mode operation, the external master can access the internal space of the MPC561/MPC563 (see Section 6.1.2, “External Master Modes”). In external master mode, the external master owns the bus, and the direction of most of the bus signals is inverted, relative to its direction when the MPC561/MPC563 owns the bus.

The external master gets ownership of the bus and asserts $\overline{\text{TS}}$ in order to initiate an external master access. The access is directed to the internal bus only if the input address matches the internal address space. The access is terminated with one of the followings outputs: $\overline{\text{TA}}$, $\overline{\text{TEA}}$, or $\overline{\text{RETRY}}$. If the access completes successfully, the MPC561/MPC563 asserts $\overline{\text{TA}}$, and the external master can proceed with another external master access or relinquish the bus. If an address or data error is detected internally, the MPC561/MPC563 asserts $\overline{\text{TEA}}$ for one clock. $\overline{\text{TEA}}$ should be negated before the second rising edge after it is sampled asserted in order to avoid the detection of an error for the next bus cycle initiated. $\overline{\text{TEA}}$ is an open drain pin, and the negation timing depends on the attached pull-up. The MPC561/MPC563 asserts the $\overline{\text{RETRY}}$ signal for one clock in order to retry the external master access.

If the address of the external access does not match the internal memory space, the internal memory controller can provide the chip-select and control signals for accesses that belong to one of the memory controller regions. This feature is explained in Chapter 10, “Memory Controller.”

Figure 9-35 and Figure 9-36 illustrate the basic flow of read and write external master accesses.

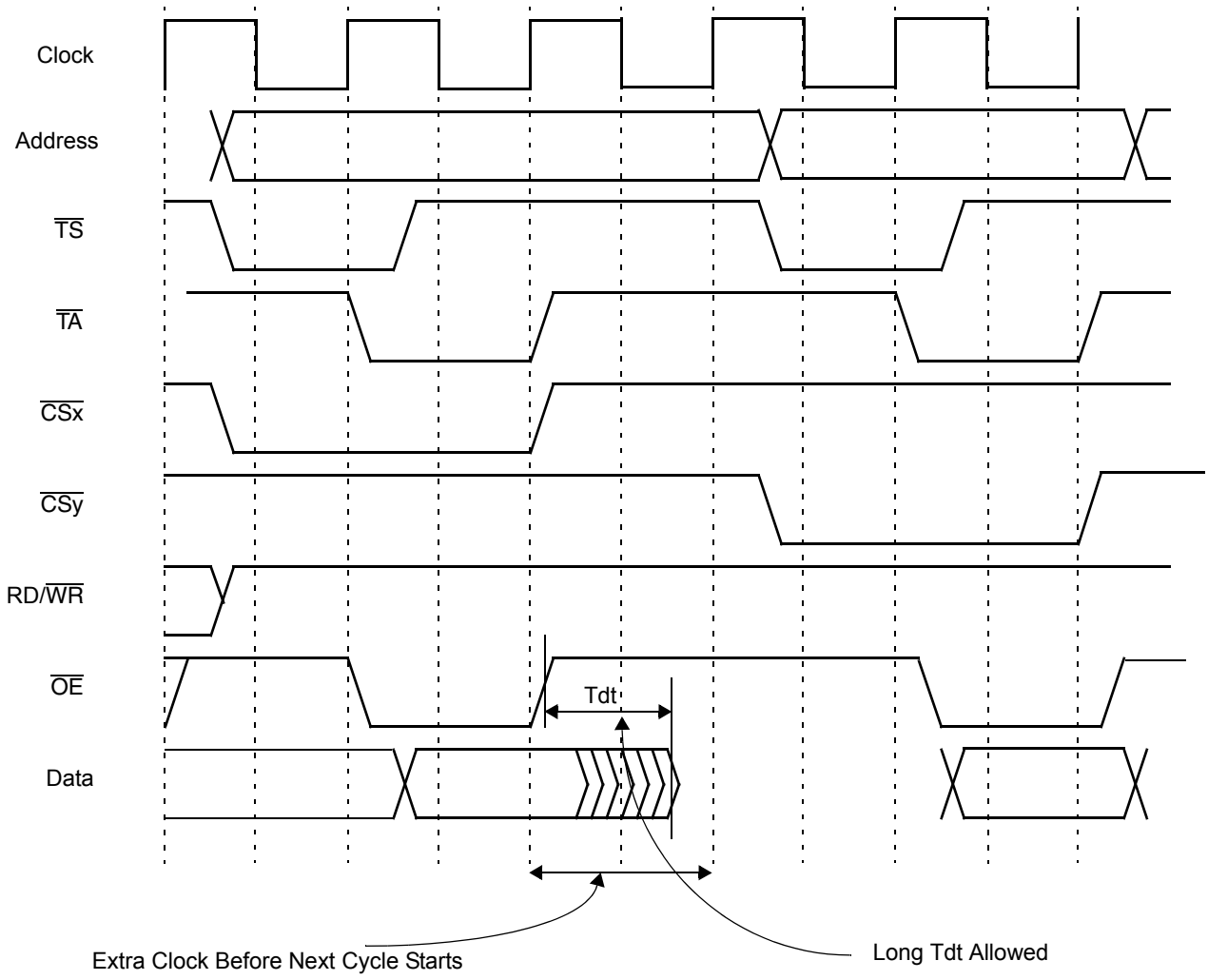


Figure 10-17. Consecutive Accesses
(Read After Read From Different Banks, EHTR = 1)

Figure 10-18 shows two consecutive read cycles from the same bank. Even though EHTR = 1, no extra clock cycle is inserted between the memory cycles. (In the case of two consecutive read cycles to the same region, data contention is not a concern.)

When a trigger event causes a CCW execution in progress to be aborted, the aborted conversion is shown as a ragged end of a shortened CCW rectangle.

The situation diagrams also show when key status bits are set. Table 13-23 describes the status bits.

Table 13-23. Status Bits

Bit	Function
CF Flag	Set when the end of the queue is reached
PF Flag	Set when a queue completes execution up through a pause bit
Trigger Overrun Error (TOR)	Set when a new trigger event occurs before the queue is finished serving the previous trigger event

Below the queue execution flows are three sets of blocks that show the status information that is made available to the software. The first two rows of status blocks show the condition of each queue as:

- Idle
- Active
- Pause
- Suspended (queue 2 only)
- Trigger pending

The third row of status blocks shows the 4-bit QS status register field that encodes the condition of the two queues. Two transition status cases, QS = 0011 and QS = 0111, are not shown because they exist only very briefly between stable status conditions.

The first three examples in Figure 13-27 through Figure 13-29 (S1, S2, and S3) show what happens when a new trigger event is recognized before the queue has completed servicing the previous trigger event on the same queue.

In situation S1 (Figure 13-27), one trigger event is being recognized on each queue while that queue is still working on the previously recognized trigger event. The trigger overrun error status bit is set, and otherwise, the premature trigger event is ignored. A trigger event that occurs before the servicing of the previous trigger event is completed does not disturb the queue execution in progress.

configures the corresponding signal as an input. The software is responsible for ensuring that DDR bits are not set to one on signals used for analog inputs. When the DDR bit is set to one and the signal is selected for analog conversion, the voltage sampled is that of the output digital driver as influenced by the load.

NOTE

Caution should be exercised when mixing digital and analog inputs. This should be isolated as much as possible. Rise and fall times should be as large as possible to minimize AC coupling effects.

There are two special cases to consider for the digital I/O port operation. When QACR0[EMUX] bit is set, enabling external multiplexing, the data direction register settings are ignored for the bits corresponding to PORTQA[2:0], which are the three multiplexed address output signals, MA[2:0]. The MA[2:0] signals are forced to be digital outputs, regardless of the data direction setting, and the multiplexed address outputs are driven. The data returned during a port data register read is the value of the multiplexed address latches which drive MA[2:0], regardless of the data direction setting.

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	DDQA7	DDQA6	DDQA5	DDQA4	DDQA3	DDQA2	DDQA1	DDQA0	DDQB7	DDQB6	DDQB5	DDQB4	DDQB3	DDQB2	DDQB1	DDQB0
$\overline{\text{SRESET}}$	0000_0000_0000_0000															
Addr	0x30 4808 (DDRQA_A); 0x30 4C08 (DDRQA_B); 0x30 4809 (DDRQB_A); 0x30 4C09 (DDRQB_B)															

Figure 14-8. Port*x* Data Direction Register (DDRQA and DDRQB)

14.3.5 Control Register 0

Control Register 0 defines whether external multiplexing is enabled, assigns external triggers to the conversion queues and sets up the QCLK prescaler parameter field. All of the implemented control register fields can be read or written but reserved fields read zero and writes have no effect. Typically, they are written once when software initializes the QADC64E and are not changed afterwards.

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	EMUX	—		TRG	—					PRESCALER						
$\overline{\text{SRESET}}$	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1
Addr	0x30 480A (QACR0_A); 0x30 4C0A (QACR0_B)															

Figure 14-9. Control Register 0 (QACR0)

Table 16-26. IMASK Bit Descriptions

Bits	Name	Description
0:7, 8:15	IMASKH, IMASKL	IMASK contains two 8-bit fields, IMASKH and IMASKL. IMASK can be accessed with a 16-bit read or write, and IMASKH and IMASKL can be accessed with byte reads or writes. IMASK contains one interrupt mask bit per buffer. It allows the CPU to designate which buffers will generate interrupts after successful transmission/reception. Setting a bit in IMASK enables interrupt requests for the corresponding message buffer.

16.7.14 Interrupt Flag Register (IFLAG)

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	IFLAGH								IFLAGL							
$\overline{\text{SRESET}}$	0000_0000_0000_0000															
Addr	0x30 70A4 (IFLAG_A); 0x30 74A4 (IFLAG_B); 0x30 78A4 (IFLAG_C)															

Figure 16-21. Interrupt Flag Register (IFLAG)

Table 16-27. IFLAG Bit Descriptions

Bits	Name	Description
0:7, 8:15	IFLAGH, IFLAGL	IFLAG contains two 8-bit fields, IFLAGH and IFLAGL. IFLAG can be accessed with a 16-bit read or write, and IFLAGH and IFLAGL can be accessed with byte reads or writes. IFLAG contains one interrupt flag bit per buffer. Each successful transmission/reception sets the corresponding IFLAG bit and, if the corresponding IMASK bit is set, an interrupt request will be generated. To clear an interrupt flag, first read the flag as a one, and then write it as a zero. Should a new flag setting event occur between the time that the CPU reads the flag as a one and writes the flag as a zero, the flag is not cleared. This register can be written to zeros only.

16.7.15 Error Counters (RXECTR, TXECTR)

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	RXECTR								TXECTR							
$\overline{\text{SRESET}}$	0000_0000_0000_0000															
Addr	0x30 70A6 (RxECTR_A/TxECTR_A); 0x30 74A6 (RxECTR_B/TxECTR_B); 0x30 78A6 (TxECTR_C/TxECTR_C)															

Figure 16-22. Receive Error Counter (RXECTR), Transmit Error Counter (TXECTR)

Table 16-28. RXECTR, TXECTR Bit Descriptions

Bits	Name	Description
0:7, 8:15	RXECTR, TXECTR	Both counters are read only, except when the TouCAN is in test or debug mode.

SHORT_REG[SH_ET2]. ETRIG1 can be shorted to A_TPUCH15 and ETRIG2 can be shorted to B_TPUCH15.

Since the ETRIG1 and ETRIG2 signals are shared with PCS6 and PCS7 respectively, the PPM shorting will allow both ETRIG and PCS functions to be available. By setting up A_TPUCH15 and/or B_TPUCH15 as output signals, enabling a short to ETRIG1 and/or ETRIG2 and sending a trigger signal from the TPU channels, the QADC64E can be successfully triggered, leaving the ETRIG signals free to be configured for PCS functions.

18.3.2.4 T2CLK

Each of the two TPU modules has an input clock, T2CLK. The A_T2CLK and B_T2CLK signals are shared with PCS4 and PCS5 respectively. The T2CLK signals can be shorted internally by SHORT_REG[SH_T2CLK] so that only one signal needs to be input to the device, leaving the other signal free for PCS functionality.

18.3.3 PPM Module Pad Configuration

The PPM module has six pads associated with it, four I/O pads PPM_RX[0:1] and PPM_TX[0:1] and two clock outputs PPM_TCLK and PPM_TSYNC. All six PPM signals are multiplexed with MIOS signals. In order to be able to access the PPM functions the signals must be configured appropriately. PPM pad control is done in the PDMCR2 register.

As well as enabling signal functions, this register can configure the PPM pads for 2.6-V or 5-V operation. Refer to Chapter 2, “Signal Descriptions,” for more details.

18.4 PPM Registers

18.4.1 Module Configuration Register (PPMMCR)

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	STOP	RESERVED							SUPV	RESERVED						
SRESET	0000_0000_0000_0000															
Addr	0x30 5C00															

Figure 18-8. Module Configuration Register (PPMMCR)

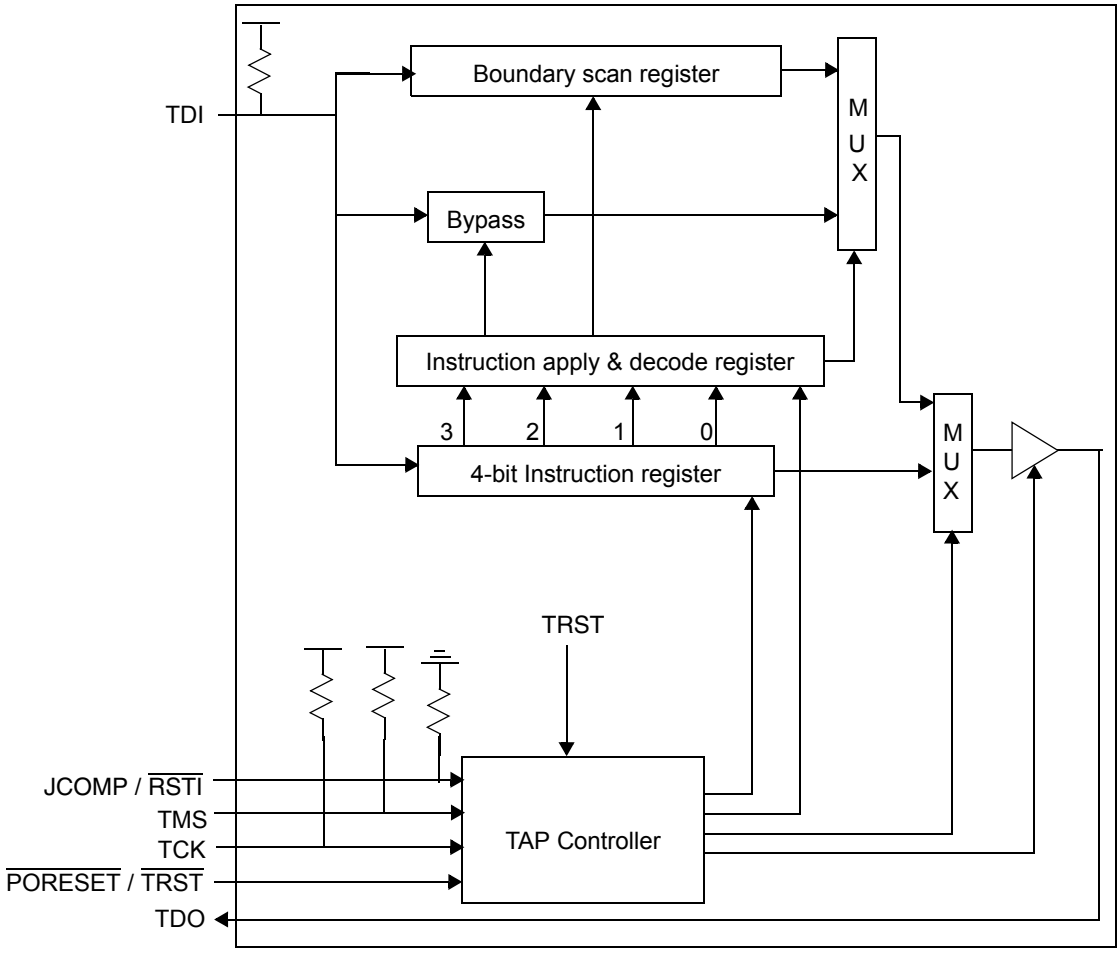


Figure 25-2. Test Logic Block Diagram

25.1.2 Entering JTAG Mode

To enable JTAG on reset for board test JCOMP/$\overline{\text{RSTI}}$ must be high on $\overline{\text{PORESET}}$ rising edge as shown in Figure 25-3.

NOTE

JTAG puts all output pins in fast slew rate mode. Enough current cannot be supplied to allow all the pins to be switched simultaneously, so this should be avoided.

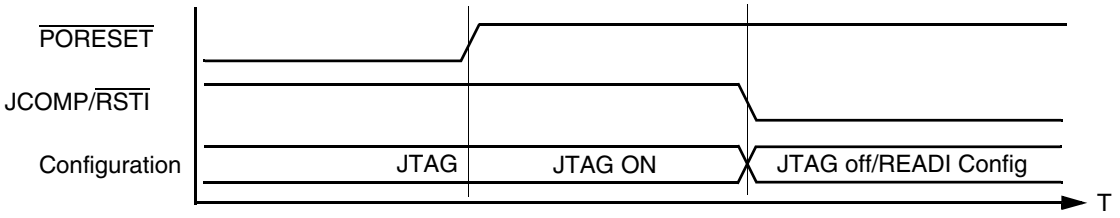


Figure 25-3. JTAG Mode Selection

A.2.7 Class Code Compression Algorithm Rules

- Compressed instruction length may vary between 6 and 36 bits and is even.
- A compressed instruction can begin at any even location in a memory word.
- An instruction source may be compressed as a single 32-bit segment or as two independent 16-bit segments.
- Possible partitions of an instruction for compression are:
  - One 32-bit bypass segment
  - One 32-bit compressed segment
  - One 16-bit compressed segment and one 16-bit bypass segment
  - Two 16-bit compressed segments
- A bypass field is always the second field of the two possible. Length of a bypass field can be zero, 10, 15, 16 or 32 bits.
- The class prefix in a compressed instruction is 4 bits long and covers up to 16 classes.
- The vocabulary table pointer of each field may be 2 to 9 bits long.
- Vocabulary table pointers are reversed in the code. This means the pointer's LSB will be the first bit.
- In a class with a single segment of full compression, data is fetched from both memories.
- Every vocabulary table in the DECRAM is 16 bytes (8 entries) aligned (3 LSBs zeroed).

A.2.8 Bypass Field Compression Rules

The bypass field can be either a full bypass, (i.e., the whole segment from the un-compressed instruction appears as is in the compressed instruction), or it can be represented in one of several compression encoding formats. These formats are hard-wired in the decompression module.

A.2.8.1 Branch Right Segment Compression #1

For the MPC562/MPC564, a 15-bit bypass is used to indicate that the AA bit of a branch instruction should be inserted with a value of zero. The decompression process is performed as shown in Figure A-4.

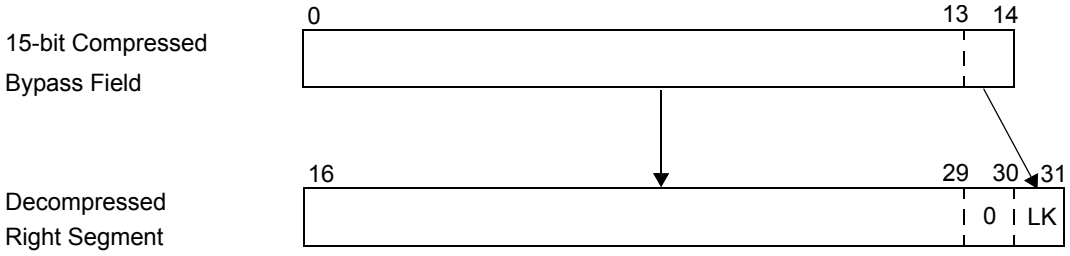


Figure A-4. Branch Right Segment Compression #1

This bypass is coded by a value of "13" (0xD) in the TP2LEN field of the DCCR register.

$R_{\theta JC}$ is device related and cannot be influenced. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the air flow can be changed around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for ceramic packages with heat sinks where about 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

The simplest thermal model of a package which has demonstrated reasonable accuracy (about 20 percent) is a two resistor model consisting of a junction to board and a junction to case thermal resistance. The junction to case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board. temperature.

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_B = board temperature (°C)

$R_{\theta JB}$ = package junction to board resistance (°C/W)

P_D = power dissipation in package (Ω)

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction to board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application (2), or a more accurate and complex model of the package can be used in the thermal simulation. Consultation on the creation of the complex model is available.

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = thermal characterization parameter

P_D = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 specification published by JEDEC using a 40 gauge type-T thermocouple epoxied to the top center of the package case. The thermocouple

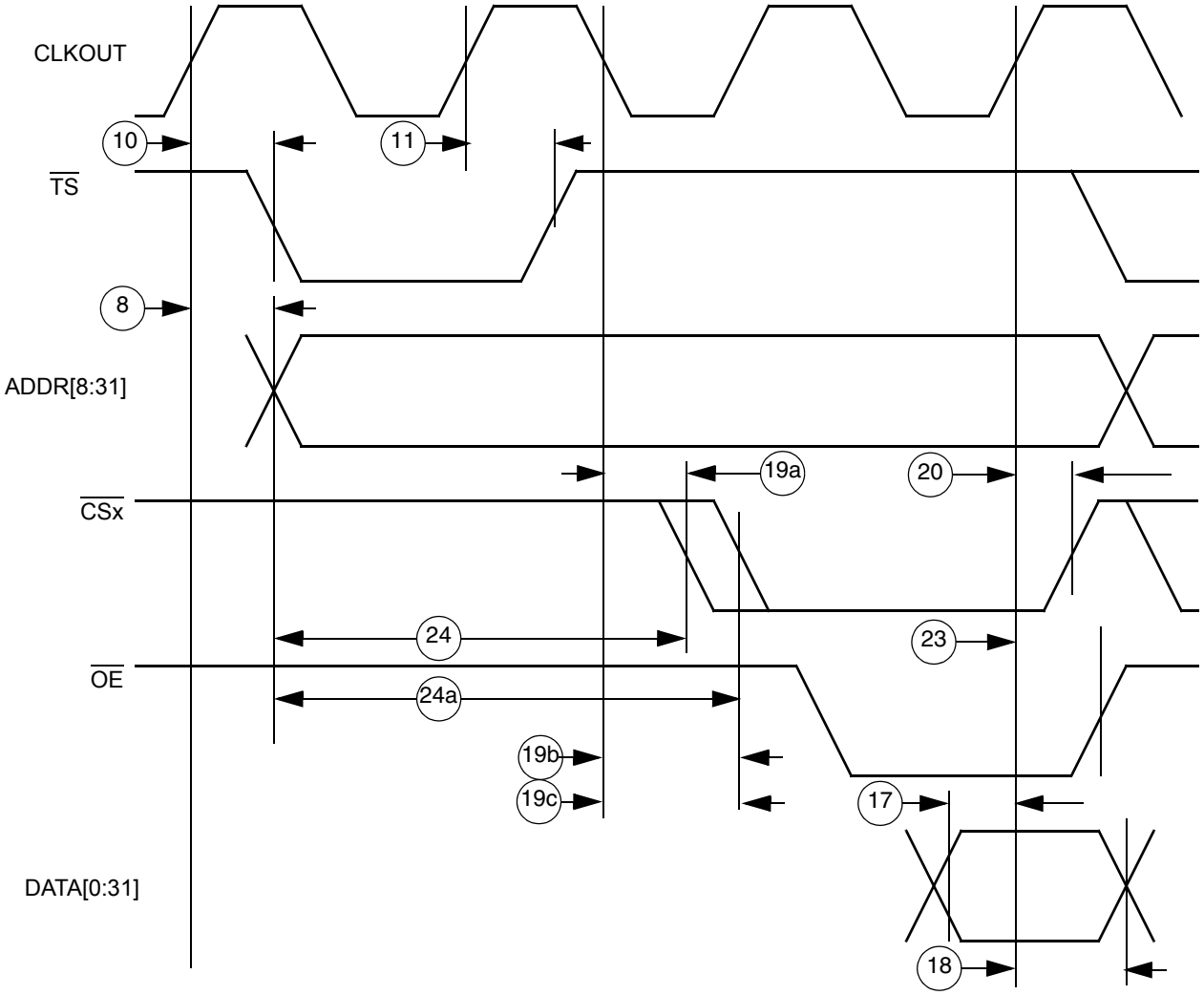


Figure G-18. External Bus Read Timing (GPCM Controlled – TRLX = '1', ACS = '10', ACS = '11')

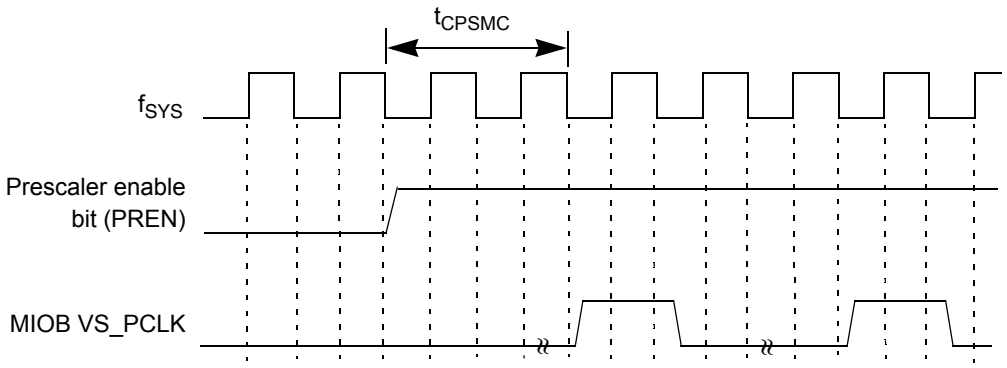
Table G-23. MCPSM Timing Characteristics

Note: After reset MCPSMSCR_PSL[3:0] is set to 0b0000.

Note: VS_PCLK is the MIOS prescaler clock which is distributed to all the counter (e.g., MPWMSM and MMCSM) submodules.

Characteristic	Symbol	Delay	Unit
MCPSM enable to VS_PCLK pulse[1]	t_{CPSMC}	(MCPSMSCR_PSL[3:0]) -1	System Clock Cycles

1 The MCPSM clock prescaler value (MCPSMSCR_PSL[3:0]) should be written to the MCPSMSCR (MCPSM Status/Control Register) before rewriting the MCPSMSCR to set the enable bit (MCPSMSCR_PREN). If this is not done the prescaler will start with the old value in the MCPSMSCR_PSL[3:0] before reloading the new value into the counter.



Note 1: f_{SYS} is the internal system clock for the IMB3 bus.
Note 2: The numbers associated with the f_{SYS} ticks refer to the IMB3 internal state.
Note 3: vs_pclk is the MIOS prescaler clock which is distributed around the MIOS to counter modules such as the MMCSM and MPWMSM.

Figure G-46. MCPSM Enable to VS_PCLK Pulse Timing Diagram

G.21.1 MPWMSM Timing Characteristics

Table G-24. MPWMSM Timing Characteristics

Note: All delays are in system clock periods.

Characteristic	Symbol	Min	Max
PWMSM output resolution	t_{PWMR}	— [1]	2.0 [2]
PWM output pulse[3]	t_{PWMO}	2.0	—
MPWMI input pin to MPWMSCR_PIN status set	t_{PIN}	1	2
CPSM enable to output set[4]	t_{PWMP}	(MPWMPERR - MPWMPULR + 1) * (256 - MPWMSCR_CP) * MCPSMSCR_PSL + 1	
MPWMSM Enable to output set (MIN)[5]	t_{PWME}	(MPWMPERR - MPWMPULR) * (256 - MPWMSCR_CP) * MCPSMSCR_PSL + 3 + (255 - MPWMSCR_CP) * MCPSMSCR_PSL[6]	