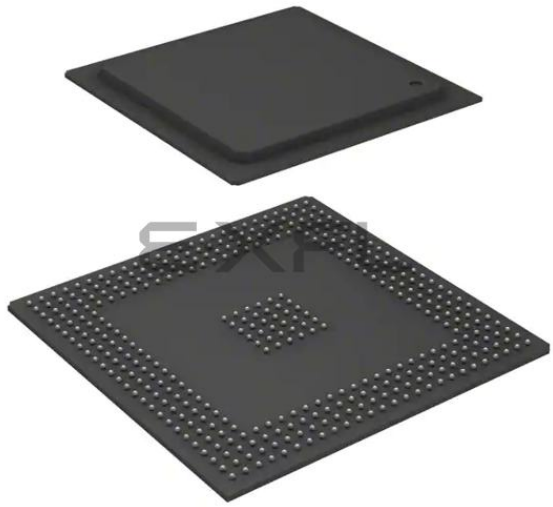

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Details	
Product Status	Not For New Designs
Core Processor	PowerPC
Core Size	32-Bit Single-Core
Speed	56MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	64
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 2.7V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	388-BBGA
Supplier Device Package	388-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc561mvr56d

Tables

Table 2-1. MPC561/MPC563 Signal Descriptions (continued)

Signal Name	No. of Signals	Type	Function after Reset[1]	Description
VSS	1	I	VSS	VSS. Zero supply/ground level for internal logic/external bus.
IRAMSTBY	1	I	IRAMSTBY	SRAM Keep-Alive Power. This is an input current source for an internal regulator that supplies voltage to all SRAM modules in standby mode. This pad connects through a voltage regulator and a voltage switch to the following modules: CALRAM (32-Kbyte SRAM), DPTRAM (8-Kbyte SRAM), BBC DECRAM (2-Kbyte vocabulary SRAM).

1 This is the function after $\overline{\text{PORESET}}$/$\overline{\text{TRST}}$ and $\overline{\text{HRESET}}$.

2 This signal also included the MDO5 function on the K27S mask set of the MPC561.

3 This signal was ECK on K27S mask set of MPC561.

4 Only the MCP563/MPC564 have Flash memory.

5 The input only applies in legacy mode.

6 C_CNTX0 and C_CNRX0 can be shared either with the MIOS14 GPIO pins (MPIO32B12, MPIO32B11) or with the QSMCM SC12 pins (TXD2 / QGPO2, RXD2 / QGPI2). The selection is made by the TCNC bits in the PDMCR2 register. Refer to Section 2.4, “Pad Module Configuration Register (PDMCR2).”

2.2.1 MPC561/MPC563 Signal Multiplexing

Table 2-2 describes the signal multiplexing that occurs between different modules of the MPC561/MPC563. Most of the signal functions are controlled by the PDMCR2 register.

Table 2-2. MPC561/MPC563 Signal Sharing

Signal Name	Module Sharing
C_CNTX0/MPIO32B12, C_CNRX0/MPIO32B11	TouCAN shared with MIOS14 GPIO
TXD2/QGPO2/C_CNTX0 RXD2/QGPI2/C_CNRX0	TouCAN shared with QSMCM SCI2
MPIO32B5/MDO5	READI submodule shared with MIOS14 GPIO
MPIO32B6/MPWM4, MPIO32B7/MPWM5, MPIO32B8/MPWM20, MPIO32B9/MPWM21	MIOS14 PWM submodule shared with MIOS14 GPIO
VF0/MPIO32B0/MDO1, VF1/MPIO32B1/MCKO, VF2/MPIO32B2/$\overline{\text{MSEI}}$, VFLS0/MPIO32B3/$\overline{\text{MSEO}}$	Debug pins shared with MIOS14 GPIO and READI
MPIO32B13/PPM_TCLK MPIO32B14/PPM_RX0 MPIO32B15/PPM_TX0	PPM submodule shared with MIOS14 GPIO
MPWM2/PPM_TX1 MPWM3/PPM_RX1	PPM submodule shared with MIOS14 PWM submodule

Table 7-1. Reset Action Taken for Each Reset Cause

Reset Source	Reset Logic and PLL States Reset	System Configuration Reset	Clock Module Reset	$\overline{\text{HRESET}}$ Pin Driven	Debug Port Configuration	Other Internal Logic Reset	$\overline{\text{SRESET}}$ Pin Driven
Power-On Reset ($\overline{\text{PORESET}}$)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Hard Reset ($\overline{\text{HRESET}}$) Sources: • External Hard Reset • Loss of Lock • On-Chip Clock Switch • Illegal Low-Power Mode • Software Watchdog • Checkstop • Debug Port Hard Reset	No	Yes	Yes	Yes	Yes	Yes	Yes
Soft Reset ($\overline{\text{SRESET}}$) Sources: • External Soft Reset • Debug Port Soft Reset • JTAG Reset	No	No	No	No	Yes	Yes	Yes

7.3 Data Coherency During Reset

The MPC561/MPC563 supports data coherency and avoids data corruption during reset. If a cycle is executing when any $\overline{\text{SRESET}}$ or $\overline{\text{HRESET}}$ source is detected, then the cycle will either complete or will not start before generating the corresponding reset control signal. There are reset sources, however, when the MPC561/MPC563 generates an internal reset due to special internal situations where this protection is not supported. See Section 7.4, “Reset Status Register (RSR).”

In the case of large operand size (32 or 16 bits) transactions to a smaller port size, the cycle is split into two 16-bit or four 8-bit cycles. In this case, data coherency is assured and data will not be corrupted.

In the case where the core executes an unaligned load/store cycle which is broken down into multiple cycles, data coherency is NOT assured between these cycles (i.e., data could be corrupted).

Contention may occur if a write access is in progress to external memory and $\overline{\text{SRESET}}$/$\overline{\text{HRESET}}$ is asserted and the external reset configuration word (RCW) is used. In this case, the external RCW drivers, usually activated by $\overline{\text{HRESET}}$/$\overline{\text{SRESET}}$ lines, will drive the data bus together with the MPC561/MPC563. Thus the data in the RAM may be corrupted regardless of the data coherency mechanism in the MPC561/MPC563.

Table 7-2. Reset Configuration Word and Data Corruption/Coherency

Reset Driven	Reset to Use for Data Coherency ($\overline{\text{EXT\_RESET}}$)	Comments
$\overline{\text{HRESET}}$	$\overline{\text{SRESET}}$	

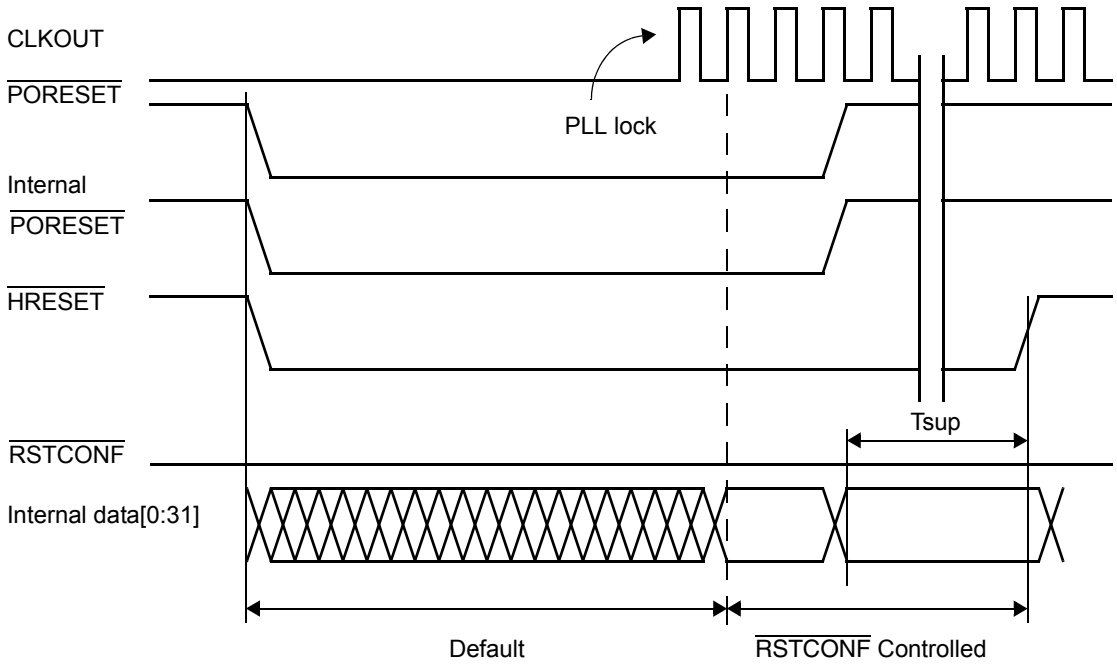

Figure 7-5. Reset Configuration Timing for "Long" PORESET Assertion, Limp Mode Disabled

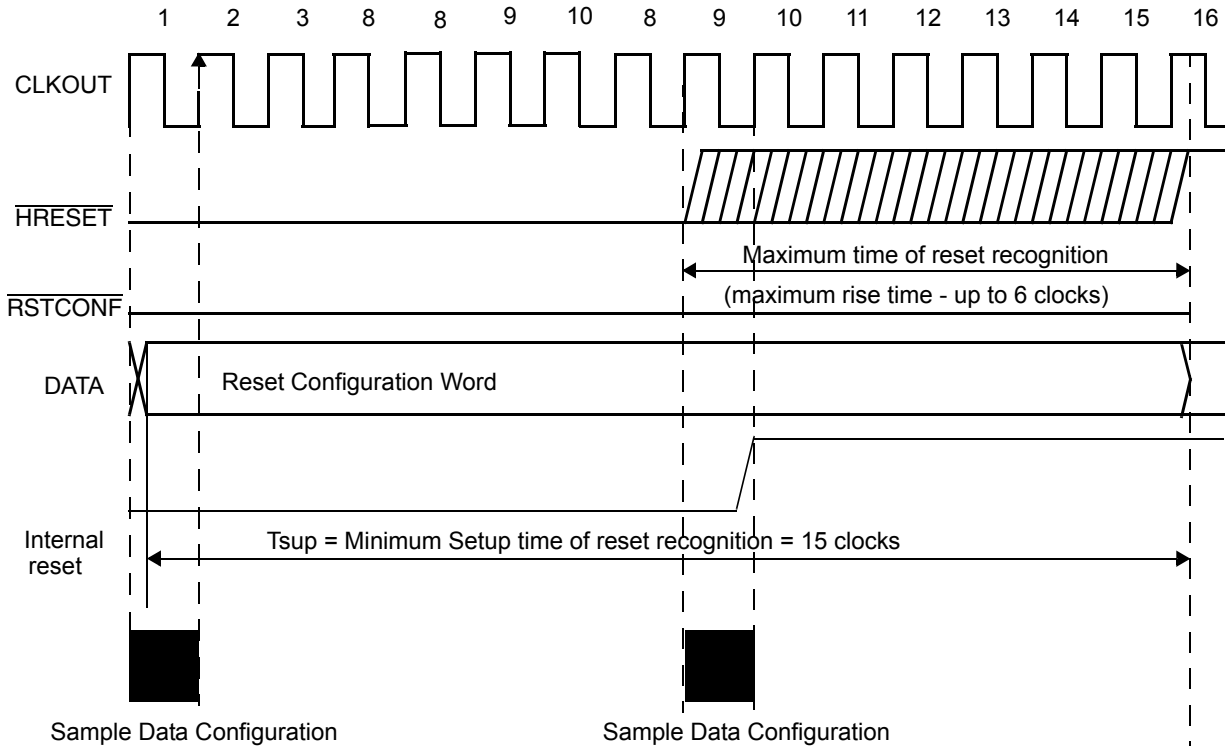

Figure 7-6. Reset Configuration Sampling Timing Requirements

8.2.1 Frequency Multiplication

The PLL can multiply the input frequency by any integer between one and 4096. The multiplication factor depends on the value of the MF[0:11] bits in the PLPRCR register. While any integer value from one to 4096 can be programmed, the resulting VCO output frequency must be at least 15 MHz. The multiplication factor is set to a predetermined value during power-on reset as defined in Table 8-1.

8.2.2 Skew Elimination

The PLL is capable of eliminating the skew between the external clock entering the chip (EXTCLK) and both the internal clock phases and the CLKOUT pin, making it useful for tight synchronous timings. Skew elimination is active only when the PLL is enabled and programmed with a multiplication factor of one or two (MF = 0 or 1). The timing reference to the system PLL is the external clock input (EXTCLK pin).

8.2.3 Pre-Divider

A pre-divider before the phase comparator enables additional system clock resolution when the crystal oscillator frequency is 20 MHz. The division factor is determined by the DIVF[0:4] bits in the PLPRCR.

8.2.4 PLL Block Diagram

As shown in Figure 8-3, the reference signal, OSCCLK, goes to the phase comparator. The phase comparator controls the direction (up or down) that the charge pump drives the voltage across the external filter capacitor (XFC). The direction depends on whether the feedback signal phase lags or leads the reference signal. The output of the charge pump drives the VCO. The output frequency of the VCO is divided down and fed back to the phase comparator for comparison with the reference signal, OSCCLK. The MF values, zero to 4095, are mapped to multiplication factors of one to 4096. Note that when the PLL is operating in 1:1 mode (refer to Table 8-1), the multiplication factor is one (MF = 0). The PLL output frequency is twice the maximum system frequency. This double frequency is needed to generate GCLK1 and GCLK2 clocks. On power-up, with a 4-MHz or 20-MHz crystal and the default MF settings, VCOOUT will be 40 MHz and the system clock will be 20 MHz.

The equation for VCOOUT is:

$$\text{VCOOUT} = \frac{\text{OSCCLK}}{\text{DIVF} + 1} \times (\text{MF} + 1) \times 2$$

NOTE

When operating with the backup clock, the system clock (and CLKOUT) is one-half of the ring oscillator frequency, (i.e., the system clock is approximately 11 MHz). The time base and PIT clocks will be twice the system clock frequency.

In the case of initial system power up, or if KAPWR is lost, an external circuit must assert power on reset ($\overline{\text{PORESET}}$). Once KAPWR is valid, $\overline{\text{PORESET}}$ must be asserted long enough to allow the external oscillator to start up and stabilize for the device to come out of reset in normal (non limp) mode.

Table 10-8. BR0–BR3 Bit Descriptions

Bits	Name	Description
0:16	BA	Base address. These bits are compared to the corresponding unmasked address signals among ADDR[0:16] to determine if a memory bank controlled by the memory controller is being accessed by an internal bus master. (The address types are also compared.) These bits are used in conjunction with the AM[0:16] bits in the OR.
17:19	AT	Address type. This field can be used to require accesses of the memory bank to be limited to a certain address space type. These bits are used in conjunction with the ATM bits in the OR. Note that the address type field uses only AT[0:2] and does not need AT3 to define the memory type space. For a full definition of address types, refer to Section 9.5.8.6, “Address Types.”
20:21	PS	Port size 00 32-bit port 01 8-bit port 10 16-bit port 11 Reserved
22	SST	Short Setup Time – This field specifies the setup time required for this memory region. 0 Normal setup time (like the MPC555) 1 Short Setup Time selected Note that an external burst access with short setup timing will corrupt any USIU register load/store if SCCR[EBDF] is not 0b00. Refer to Table 8-9.
23	WP	Write protect. An attempt to write to the range of addresses specified in a base address register that has this bit set can cause the $\overline{\text{TEA}}$ signal to be asserted by the bus-monitor logic (if enabled), causing termination of this cycle. 0 Both read and write accesses are allowed 1 Only read accesses are allowed. The $\overline{\text{CSx}}$ signal and $\overline{\text{TA}}$ are not asserted by the memory controller on write cycles to this memory bank. WPER is set in the MSTAT register if a write to this memory bank is attempted
24	—	Reserved
25	BL	Burst Length – This field specifies the maximum number of words that may comprise a burst access for this memory region. This field has an effect only in the case when the burst accesses are initiated by the USIU (SIUMCR[BURST_EN] =1). 0 Burst access of up to 4 words 1 Burst access of up to 8 words
26	WEBS	Write-enable/byte-select. This bit controls the functionality of the $\overline{\text{WE}}$/$\overline{\text{BE}}$ pads. 0 The $\overline{\text{WE}}$/$\overline{\text{BE}}$ pads operate as $\overline{\text{WE}}$ 1 The $\overline{\text{WE}}$/$\overline{\text{BE}}$ pads operate as $\overline{\text{BE}}$
27	TBDIP	Toggle-burst data in progress. TBDIP determines how long the $\overline{\text{BDIP}}$ strobe will be asserted for each data beat in the burst cycles.
28	LBDIP	Late-burst-data-in-progress (LBDIP). This bit determines the timing of the first assertion of the $\overline{\text{BDIP}}$ signal in burst cycles. NOTE: Do not set both LBDIP and TBDIP bits in a region’s base registers; behavior in such cases is unpredictable. 0 Normal timing for $\overline{\text{BDIP}}$ assertion (asserts one clock after negation of $\overline{\text{TS}}$) 1 Late timing for $\overline{\text{BDIP}}$ assertion (asserts after the programmed number of wait states)
29	SETA	External transfer acknowledge 0 $\overline{\text{TA}}$ generated internally by memory controller 1 $\overline{\text{TA}}$ generated by external logic. Note that programming the timing of $\overline{\text{CS}}$/$\overline{\text{WE}}$/$\overline{\text{OE}}$ strobes may have no meaning when this bit is set

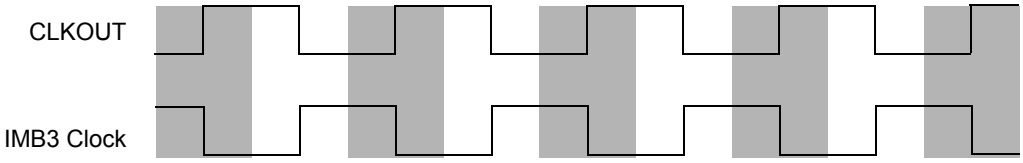

Figure 12-2. IMB3 Clock – Full-Speed IMB3 Bus

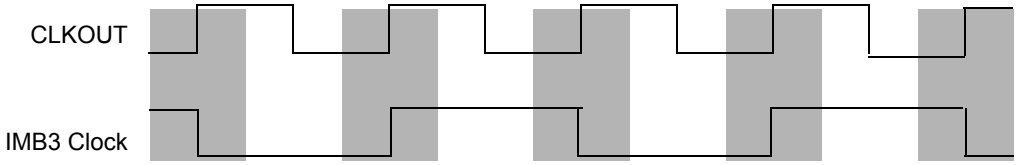

Figure 12-3. IMB3 Clock – Half-Speed IMB3 Bus

Table 12-2 shows the number of system clock cycles that the UIMB requires to perform each type of bus cycle. It is assumed that the IMB3 is available to the UIMB at all times (fastest possible case).

Table 12-2. Bus Cycles and System Clock Cycles

Bus Cycle (from U-bus Transfer Start to U-bus Transfer Acknowledge)	Number of System Clock Cycles	
	Full Speed	Half Speed
Normal write	4	6
Normal read	4	6
Dynamically-sized write	6	10
Dynamically-sized read	6	10

NOTE

The UIMB interface dynamically interprets the port size of the addressed module during each bus cycle, allowing bus transfers to and from 16-bit and 32-bit IMB3 modules. During a bus transaction, the slave module on the IMB3 signals its port size (16- or 32-bit) via an internal port size signal.

12.4 Interrupt Operation

The interrupts from the modules on the IMB3 are propagated to the interrupt controller in the USIU through the UIMB interface. The UIMB interrupt synchronizer latches the interrupts from the modules on the IMB3 and drives them onto the U-bus, where they are latched by the USIU interrupt controller.

12.4.1 Interrupt Sources and Levels on IMB3

The IMB3 has eight interrupt lines. There can be a maximum of 32 levels of interrupts from the modules on IMB3 bus. A single module can be a source for more than one interrupt. For example, the QSMCM can generate two interrupts (one for QSCI1/QSCI2 and another for QSPI). In this case, the QSMCM has two interrupt sources. Each of these two sources can assert the interrupt on any of the 32 levels.

register fields can be read or written but reserved fields read zero and writes have no effect. Typically, they are written once when software initializes the QADC64E and are not changed afterwards.

	MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
Field	EMUX	—		TRG	—			PSH					PSA	PSL		
$\overline{\text{SRESET}}$	0	00		0	000			0_0001					0	011		
Addr	0x30 480A (QACR0_A); 0x30 4C0A (QACR0_B)															

Figure 13-9. Control Register 0 (QACR0)

Table 13-9. QACR0 Bit Descriptions

Bits	Name	Description
0	EMUX	Externally multiplexed mode. The EMUX bit configures the QADC64E for externally multiplexed mode, which affects the interpretation of the channel numbers and forces the MA[2:0] signals to be outputs. See Table 13-7 for more information. 0 Internally multiplexed, 16 possible channels 1 Externally multiplexed, 41 possible channels
1:2	—	Reserved
3	TRG	Trigger assignment. TRG allows the software to assign the ETRIG[2:1] signals to queue 1 and queue 2. 0 ETRIG1 triggers queue 1; ETRIG2 triggers queue 2 1 ETRIG1 triggers queue 2; ETRIG2 triggers queue 1 Refer to Section 13.7.2, “External Trigger Input Signals.”
4:6	—	Reserved
7:11	PSH	Prescaler clock high time. The PSH field selects the QCLK high time in the prescaler. PSH value plus 1 represents the high time in IMB3 clocks
12	PSA	Note that this bit location is maintained for software compatibility with previous versions of the QADC64E. It serves no functional benefit in the MPC561/MPC563 and is not operational.
13:15	PSL	Prescaler clock low time. The PSL field selects the QCLK low time in the prescaler. PSL value plus 1 represents the low time in IMB3 clocks

NOTE

Details of how to calculate values for PSH, PSA, and PSL, as well as examples, are given in Section 13.5.5, “QADC64E Clock (QCLK) Generation.”

13.3.6 Control Register 1 (QACR1)

Control register 1 is the mode control register for the operation of queue 1. The application software defines the queue operating mode for the queue, and may enable a completion and/or pause interrupt. All of the control register fields are read/write data. However, the SSE1 bit always reads as zero. Most of the bits are typically written once when the software initializes the QADC64E, and not changed afterwards.

Analog supplies should be isolated from digital supplies as much as possible. This necessity stems from the higher performance requirements often associated with analog circuits. Therefore, deriving an analog supply from a local digital supply is not recommended. However, if for economic reasons digital and analog power are derived from a common regulator, filtering of the analog power is recommended in addition to the bypassing of the supplies already mentioned.

NOTE

An RC low pass filter could be used to isolate the digital and analog supplies when generated by a common regulator. If multiple high precision analog circuits are locally employed (i.e., two A/D converters), the analog supplies should be isolated from each other as sharing supplies introduces the potential for interference between analog circuits.

Grounding is the most important factor influencing analog circuit performance in mixed signal systems (or in stand-alone analog systems). Close attention must be paid not to introduce additional sources of noise into the analog circuitry. Common sources of noise include ground loops, inductive coupling, and combining digital and analog grounds together inappropriately.

The problem of how and when to combine digital and analog grounds arises from the large transients which the digital ground must handle. If the digital ground is not able to handle the large transients, the current from the large transients can return to ground through the analog ground. It is the excess current overflowing into the analog ground which causes performance degradation by developing a differential voltage between the true analog ground and the microcontroller's ground signal. The end result is that the ground observed by the analog circuit is no longer true ground and often ends in skewed results.

Two similar approaches designed to improve or eliminate the problems associated with grounding excess transient currents involve star-point ground systems. One approach is to star-point the different grounds at the power supply origin, thus keeping the ground isolated. Refer to Figure 14-49.

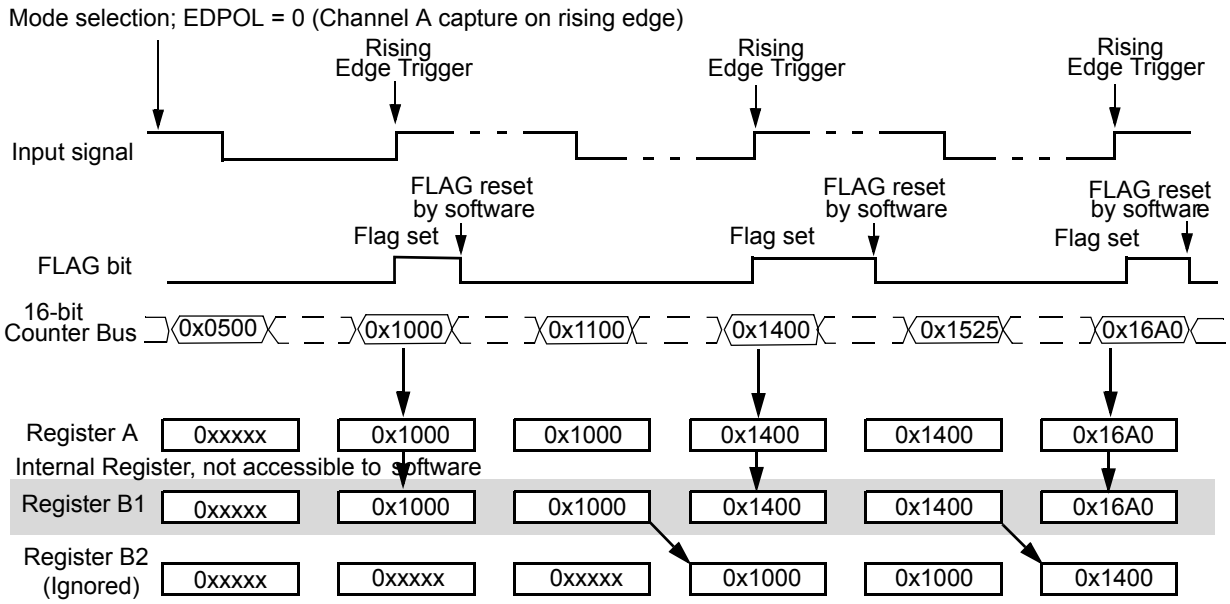

Figure 17-18. MDASM Input Capture Example

17.9.3.5 Output Compare (OCB and OCAB) Modes

Output compare mode (either OCA or OCB) is selected by setting MODE[0:3] to 0b010x. The MODE0 controls the activation criteria for the FLAG line, (i.e., when a compare occurs only on channel B or when a compare occurs on either channel).

This mode allows the MDASM to perform four different output functions:

- Single-shot output pulse (two edges), with FLAG line activated on the second edge
- Single-shot output pulse (two edges), with FLAG line activated on both edges
- Single-shot output transition (one edge)
- Output port signal, with output compare function disabled

In this mode the leading and trailing edges of variable width output pulses are generated by calculated output compare events occurring on channels A and B, respectively. OC mode may also be used to perform a single output compare function, or may be used as an output port bit.

In this mode, channel B is accessed via register B2. A write to register B2 writes the same value to register B1 even though the contents of B1 are not used in this mode. Both channels work together to generate one ‘single shot’ output pulse signal. Channel A defines the leading edge of the output pulse, while channel B defines the trailing edge of the pulse. FLAG line activation can be done when a match occurs on channel B only or when a compare occurs on either channel (as defined by the MODE0 in the MDASMSCR register).

When this mode is first selected, (i.e., coming from disable mode, both comparators are disabled). Each comparator is enabled by writing to its data register; it remains enabled until the next successful comparison is made on that channel, whereupon it is disabled. The values stored in registers A and B are compared with the count value on the selected 16-bit counter bus when their corresponding comparators are enabled.

Chapter 18
Peripheral Pin Multiplexing (PPM) Module

The peripheral pin multiplexing (PPM) module has two main functions. The first function allows the PPM to act as a parallel-to-serial communications module. Using the PPM in this way can reduce the number of signals required to connect the MPC561/MPC563 to an external device or devices. The second function allows the PPM to short internal signals thus giving increased access to multiple functions multiplexed on the same device signal. See Figure 18-1 for a comparison of the MPC555 N-Signal I/O and the MPC561/MPC563 PPM I/O.

18.1 Key Features

- Synchronous serial interface between MCU and an external device
- Four internal parallel data sources can be multiplexed through the PPM
  - TPU3_A: 16 channels
  - TPU3_B: 16 channels
  - MIOS: 12 PWM channels, four MDA channels
  - Internal GPIO: 16 general-purpose inputs, 16 general-purpose outputs
- Software configurable stream size
  - One 16-bit transmit stream and one 16-bit receive stream
  - Two parallel 8-bit transmit streams and two parallel 8-bit receive streams
- Software configurable clock (PPM_TCLK) based on system clock
- Software selectable clock modes
  - Serial peripheral interface (SPI) mode
  - Time division multiplexing (TDM) mode
- Software selectable operation modes
  - Continuous mode – Continuously transmit/receive data through PPM
  - Start-transmit-receive (STR) mode – transmit/receive only when STR mode selected
- Software configurable internal module shorting of the following signals:
  - TouCAN_A[A_CNRX0, A_CNTX0] to TouCAN_B[B_CNRX0, B_CNTX0] and/or TouCAN_C[C_CNRX0, C_CNTX0]
  - TouCAN_B[B_CNRX0, B_CNTX0] to TouCAN_C[C_CNRX0, C_CNTX0]
  - A_TPUCH0 to B_TPUCH0
  - A_TPUCH1 to B_TPUCH1
  - A_TPUCH15 to ETRIG1
  - B_TPUCH15 to ETRIG2

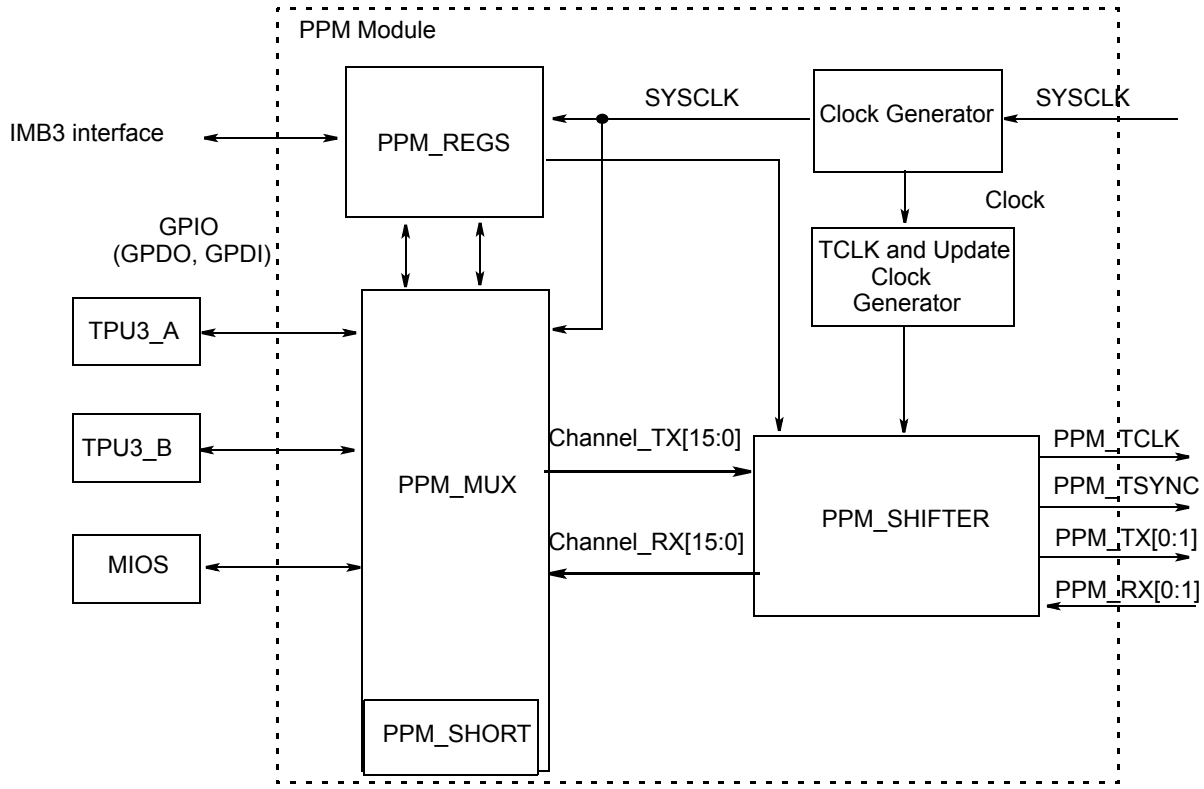

Figure 18-2. Block Diagram of PPM Module

18.3.1.1 Internal Multiplexing

In the MPC561/MPC563 devices, the PPM module supports multiplexing of four modules: TPU3_A, TPU3_B, MIOS and GPIO registers, internal to the PPM. Internal multiplexers route data between the MCU internal modules and the external device through the PPM. Four configuration registers, TX_CONFIG_1, TX_CONFIG_2, RX_CONFIG_1 and RX_CONFIG_2, control these internal multiplexers. By programming the configuration registers the PPM multiplexers select which internal module will drive data out of the PPM and which will receive data from the PPM.

The TX_CONFIG and RX_CONFIG registers allocate two bits to control each of the 16 internal multiplexers. During transmit operations, the TX_CONFIG registers determine which internal module's data will be sampled and routed to the transmit sample-and-shift register, TX_DATA. During receive operations, data in the receive sample-and-shift register, RX_SHIFTER, is routed to the internal module specified by the value of the RX_CONFIG registers, or in the case where GPDI is the destination, data is routed directly from PPM_RX[0:1]. Refer to Figure 18-4.

Table 18-9. SHORT_REG[SH_TPU] Bit Settings

SH_TPU1	A_TPUCH1	B_TPUCH1	Effect on TPU3 Modules
1	Input	Input	Data on pad A_TPUCH1 will be the input to A_TPUCH1 and B_TPUCH1
1	Input	Output	Output data on B_TPUCH1 will be the input to A_TPUCH1
1	Output	Input	Output on A_TPUCH1 will be the input data to B_TPUCH1
1	Output	Output	No Short
0	X	X	No Short

MPC561/MPC563

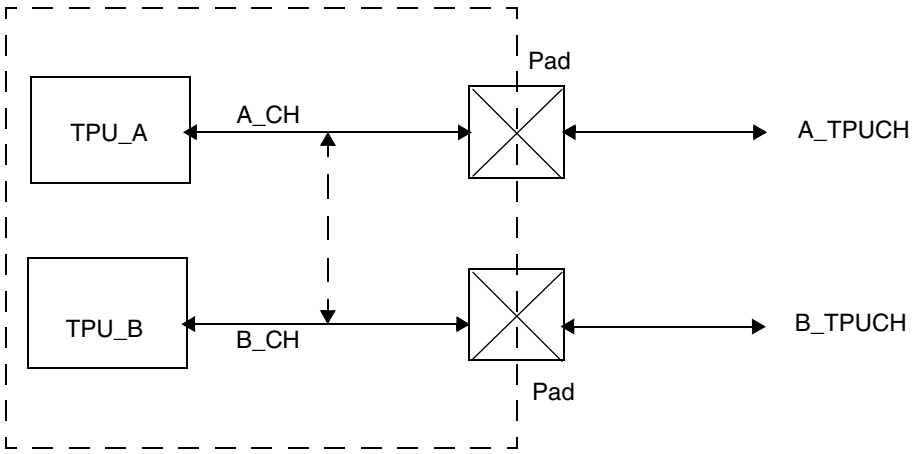

Figure 18-25. Short Between TPU Channels

18.4.11 Short Channels Register (SHORT_CH_REG)

SHORT_CH_REG allows the shorting of transmit channels from the PPM using the bit field SHORT[7:0]. The PPM normally transmits data by right-shifting TX_DATA at the rate of one bit per PPM_TCLK cycle, TX_DATA15 first. Shorts can be enabled for transmit data bits TX_DATA[1, 3, 5, 7, 9, 11, 13, and 15]. Where a short is enabled for any of these transmit data bits, that bit will be transmitted for two PPM_TCLK cycles, during its own bit time and the bit time of the following transmit data bit.

EXAMPLE

If SHORT_CH*x* = 1, transmit TX_DATA*x* during TX_DATA*x* bit time and repeat TX_DATA*x* during TX_DATA[*x*-1] bit time.

Table 19-20. System Clock Frequency/Minimum Guaranteed Detected Pulse

101	128	6.4 µs	3.88 µs	3.20 µs	2.29 µs
110	256	12.8 µs	7.76 µs	6.40 µs	4.57 µs
111	512	25.6 µs	15.51 µs	12.80 µs	9.14 µs

19.4.12 TPU Module Configuration Register 3 (TPUMCR3)

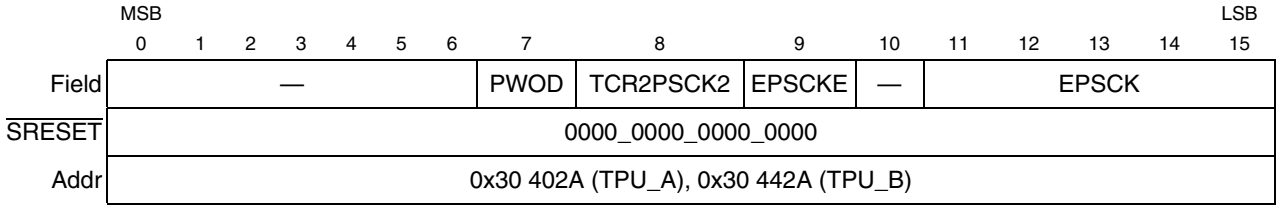

Figure 19-22. TPUMCR3 — TPU Module Configuration Register 3

Table 19-21. TPUMCR3 Bit Descriptions

Bits	Name	Description
0:6	—	Reserved
7	PWOD	Prescaler write-once disable bit. The PWOD bit does not lock the EPSCK field and the EPSCKE bit. 0 Prescaler fields in MCR are write-once 1 Prescaler fields in MCR can be written anytime
8	TCR2PSCK2	TCR2 prescaler 2 0 Prescaler clock source is divided by one. 1 Prescaler clock is divided. See divider definitions in Table 19-5.
9	EPSCKE	Enhanced pre-scaler enable 0 Disable enhanced prescaler (use standard prescaler) 1 Enable enhanced prescaler. System clock will be divided by the value in EPSCK field.
10	—	Reserved
11:15	EPSCK	Enhanced prescaler value that will be loaded into the enhanced prescaler counter. Prescaler value(EPSCK + 1) x 2. Refer to Section 19.3.8, “Prescaler Control for TCR1,” for details.

Table 25-1. MPC561 Boundary Scan Bit Definition (continued)

BSDL Bit	Cell Type	Pin/Port Name	BSDL Function	Safe Value	Control Cell	Disable Value	Disable Result	Pin Function	Pad Type
98	BC_2	*	controlr	0					
99	BC_7	A_AN57_PQA5	bidir	0	98	0	Z	IO	5vsa
100	BC_2	*	controlr	0					
101	BC_7	A_AN58_PQA6	bidir	0	100	0	Z	IO	5vsa
102	BC_2	*	controlr	0					
103	BC_7	A_AN59_PQA7	bidir	0	102	0	Z	IO	5vsa
104	BC_2	*	controlr	0					
105	BC_7	B_AN0_ANW_PQB0	bidir	0	104	0	Z	IO	5vsa
106	BC_2	*	controlr	0					
107	BC_7	B_AN1_ANX_PQB1	bidir	0	106	0	Z	IO	5vsa
108	BC_2	*	controlr	0					
109	BC_7	B_AN2_ANY_PQB2	bidir	0	108	0	Z	IO	5vsa
110	BC_2	*	controlr	0					
111	BC_7	B_AN3_ANZ_PQB3	bidir	0	110	0	Z	IO	5vsa
112	BC_2	*	controlr	0					
113	BC_7	B_AN48_PQB4	bidir	0	112	0	Z	IO	5vsa
114	BC_2	*	controlr	0					
115	BC_7	B_AN49_PQB5	bidir	0	114	0	Z	IO	5vsa
116	BC_2	*	controlr	0					
117	BC_7	B_AN50_PQB6	bidir	0	116	0	Z	IO	5vsa
118	BC_2	*	controlr	0					
119	BC_7	B_AN51_PQB7	bidir	0	118	0	Z	IO	5vsa
120	BC_2	*	controlr	0					
121	BC_7	B_AN52_MA0_PQA0	bidir	0	120	0	Z	IO	5vsa
122	BC_2	*	controlr	0					
123	BC_7	B_AN53_MA1_PQA1	bidir	0	122	0	Z	IO	5vsa
124	BC_2	*	controlr	0					
125	BC_7	B_AN54_MA2_PQA2	bidir	0	124	0	Z	IO	5vsa
126	BC_2	*	controlr	0					
127	BC_7	B_AN55_PQA3	bidir	0	126	0	Z	IO	5vsa
128	BC_2	*	controlr	0					
129	BC_7	B_AN56_PQA4	bidir	0	128	0	Z	IO	5vsa
130	BC_2	*	controlr	0					
131	BC_7	B_AN57_PQA5	bidir	0	130	0	Z	IO	5vsa
132	BC_2	*	controlr	0					
133	BC_7	B_AN58_PQA6	bidir	0	132	0	Z	IO	5vsa

Memory map tables use the notation shown below:

Notations Used in the Access Column

S = Supervisor access only

U = User access

T = Test access

Notations Used in the Reset Column

— (em dash) = Untouched

S = $\overline{\text{SRESET}}$

H = $\overline{\text{HRESET}}$

M = $\overline{\text{Module Reset}}$

POR = $\overline{\text{Power-On Reset}}$

U = Unchanged

X = Unknown

R = $\overline{\text{RSTI}}$

In each table, the codes in the Reset column indicate which reset affects register values.

Table B-1. SPR (Special Purpose Registers)

Address	Access	Symbol	Register	Size	Reset
CR	U	CR	Condition State Register See Section 3.7.4 for bit descriptions.	32	—
FPSCR	U	FPSCR	Floating-Point Status and Control Register See Table 3-5 for bit descriptions.	32	—
MSR	S	MSR	Machine State Register See Table 3-11 for bit descriptions.	32	—
SPR 1	U	XER	Integer Exception Register See Table 3-10 for bit descriptions.	32	—
SPR 8	U	LR	Link Register See Section 3.7.6 for bit descriptions.	32	—
SPR 9	U	CTR	Count Register See Section 3.7.7 for bit descriptions.	32	—
SPR 18	S	DSISR	DAE/Source Instruction Service Register See Section 3.9.2 for bit descriptions.	32	—
SPR 19	S	DAR	Data Address Register See Section 3.9.3 for bit descriptions.	32	—
SPR 22	S	DEC	Decrementer Register See Section 3.9.5 for more information.	32	POR
SPR 26	S	SRR0	Machine Status Save/Restore Register 0 See Section 3.9.6 for bit descriptions.	32	—
SPR 27	S	SRR1	Machine Status Save/Restore Register1 See Section 3.9.7 for bit descriptions.	32	—
SPR 80	S	EIE	External Interrupt Enable See Section 3.9.10.1 for bit descriptions.	32	—

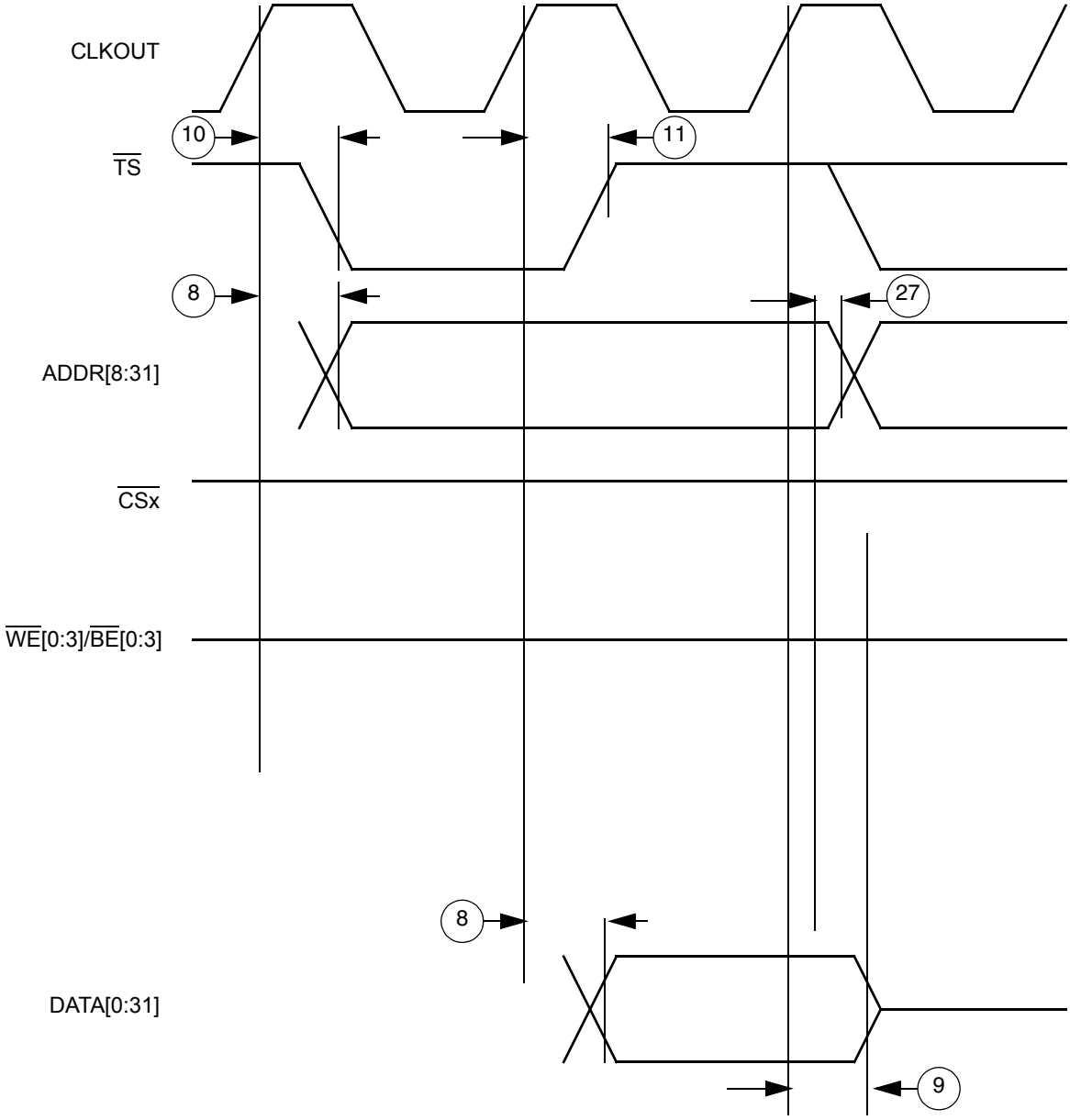

Figure F-21. Address and Data Show Cycle Bus Timing

F.22 Pin Summary

Table F-28. MPC561/MPC563 Signal Names and Pin Names

Signal Name	Pin Name	Ball Assignment
USIU		
ADDR/SGPIOA[8:31]	addr_sgpioa8	AF9
	addr_sgpioa9	AF8
	addr_sgpioa10	AC6
	addr_sgpioa11	Y4
	addr_sgpioa12	Y3
	addr_sgpioa13	AD7
	addr_sgpioa14	AE7
	addr_sgpioa15	AF7
	addr_sgpioa16	AD8
	addr_sgpioa17	AE8
	addr_sgpioa18	AC7
	addr_sgpioa19	AD9
	addr_sgpioa20	AC8
	addr_sgpioa21	AD10
	addr_sgpioa22	AF10
	addr_sgpioa23	AC9
	addr_sgpioa24	AD11
	addr_sgpioa25	AD12
	addr_sgpioa26	AC11
	addr_sgpioa27	AF11
	addr_sgpioa28	AE11
	addr_sgpioa29	AE12
	addr_sgpioa30	AE10
	addr_sgpioa31	AE9

NOTES

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M-1994.

2. DIMENSIONS IN MILLIMETERS.

3. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM A.

4. PRIMARY DATUM A AND THE SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX	DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	1.95	2.55							
A1	0.40	0.60							
A2	0.50	0.70							
A3	1.05	1.25							
b	0.50	0.70							
D	27.00 BSC								
D1	25.00 REF								
D2	23.30	24.70							
E	27.00 BSC								
E1	25.00 REF								
E2	23.30	24.70							
e	1.00 BSC								

CASE NO.	1164-01
STANDARD	JEDEC MO-151 AAL-1
REFERENCE	
TITLE	388 PBGA 27 X 27, 1.0 PITCH

SHEET 2 OF 2

Figure F-65. MPC561/MPC563 Package Footprint (2 of 2)

Table G-10. Bus Operation Timing (continued)

Note: (V_{DD} = 2.6 V ± 0.1 V, V_{DDH} = 5.0 V ± 0.25 V, $T_A = T_L$ to T_H, 50 pF load unless noted otherwise)

	Characteristic	66 MHz		Unit
		Min	Max	
19b	CLKOUT Falling Edge to $\overline{CS}$ asserted -GPCM- ACS = 11, TRLX = 0 or 1	4	9	ns
19c	CLKOUT Falling Edge to $\overline{CS}$ asserted -GPCM- ACS = 11, TRLX = 0, EBDF = 1	6.69	12.69	ns
20	CLKOUT Rising Edge to $\overline{CS}$ negated -GPCM- Read Access or Write access when CSNT = 0 or write access when CSNT = 1 and ACS = 00	1.55	4.85	ns
21	ADDR[8:31] to $\overline{CS}$ asserted -GPCM- ACS = 10, TRLX = 0	1.2	—	ns
21a	ADDR[8:31] to $\overline{CS}$ asserted -GPCM- ACS = 11, TRLX = 0	5.1	—	ns
22	CLKOUT Rising Edge to $\overline{OE}$, $\overline{WE}$[0:3]/$\overline{BE}$[0:3] asserted	1	5.45	ns
23	CLKOUT Rising Edge to $\overline{OE}$ negated	1.45	5.06	ns
24	ADDR[8:31] to $\overline{CS}$ asserted -GPCM- ACS = 10, TRLX = 1	13.95	—	ns
24a	ADDR[8:31] to $\overline{CS}$ asserted -GPCM- ACS = 11, TRLX = 1	17	—	ns
25	CLKOUT Rising Edge to $\overline{WE}$[0:3]/$\overline{BE}$[0:3] negated -GPCM-write access CSNT = ‘0‘	—	4.75	ns
25a	CLKOUT Falling Edge to $\overline{WE}$[0:3]/$\overline{BE}$[0:3] negated -GPCM-write access TRLX = ‘0’ or ‘1’, CSNT = ‘1, EBDF = 0’.	4.5	9.5	ns
25b	CLKOUT Falling Edge to $\overline{CS}$ negated -GPCM-write access TRLX = ‘0’ or ‘1’, CSNT = ‘1’, ACS = ‘10’ or ACS=’11’, EBDF = 0	4.5	9.5	ns
25c	CLKOUT Falling Edge to $\overline{WE}$[0:3]/$\overline{BE}$[0:3] negated -GPCM-write access TRLX = ‘0’, CSNT = ‘1, EBDF = 1’.	5.5	12.69	ns
25d	CLKOUT Falling Edge to $\overline{CS}$ negated -GPCM-write access TRLX = ‘0’, CSNT = ‘1’, ACS = ‘10’ or ACS=’11’, EBDF = 1	6.25	17	ns
26	$\overline{WE}$[0:3]/$\overline{BE}$[0:3] negated to D[0:31] High Z -GPCM- write access, CSNT = ‘0’	1.95	—	ns
26a	$\overline{WE}$[0:3]/$\overline{BE}$[0:3] negated to D[0:31] High Z -GPCM- write access, TRLX = ‘0’, CSNT = ‘1’, EBDF = 0	4.85	—	ns
26b	$\overline{CS}$ negated to D[0:31], High Z -GPCM- write access, ACS = ‘00’, TRLX = ‘0’ & CSNT = ‘0’	1.95	—	ns