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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, EBI/EMI, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/mb9af156nbpmc-g-jne2

4. List of Pin Function

4.1 List of Pin Numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
1	1	B1	1	B1	VCC	-	
2	2	C1	2	C1	P50	E	K
					SIN3_1		
					AIN0_2		
					TIOB8_0		
					INT00_0		
					MADATA00_0		
3	3	C2	3	C2	P51	E	K
					SOT3_1 (SDA3_1)		
					BIN0_2		
					TIOB9_0		
					INT01_0		
					MADATA01_0		
4	4	B3	4	B3	P52	E	K
					SCK3_1 (SCL3_1)		
					ZIN0_2		
					TIOB10_0		
					INT02_0		
					MADATA02_0		
5	5	D1	5	D1	P53	E	K
					SIN6_0		
					TIOB11_0		
					TIOA1_2		
					INT07_2		
					MADATA03_0		

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
-	12	E4	12	G2	P33	E	K
					ADTG_6		
					SIN6_1		
					TIOB3_1		
					INT04_0		
					MADATA10_0		
			-	-	SIN9_0		
18	-	-	-	-	P34	E	J
					SOT9_0 (SDA9_0)		
					FRCK0_0		
					TIOB4_1		
					TIOA15_2		
					MNALE_0		
-	13	F1	-	-	P34	E	J
					SOT9_0 (SDA9_0)		
					FRCK0_0		
					TIOB4_1		
					TIOA15_2		
					MADATA11_0		
19	-	-	-	-	P35	E	K
					SCK9_0 (SCL9_0)		
					IC03_0		
					TIOB5_1		
					TIOB15_2		
					INT08_1		
					MNCLE_0		
-	14	F2	-	-	P35	E	K
					SCK9_0 (SCL9_0)		
					IC03_0		
					TIOB5_1		
					TIOB15_2		
					INT08_1		
					MADATA12_0		

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
111	-	-	-	-	P65	E	K
					SCK5_1 (SCL5_1)		
					TIOB7_0		
					TIOB12_2		
					INT23_0		
112	-	-	-	-	P64	E	K
					SOT5_1 (SDA5_1)		
					TIOA7_0		
					INT10_2		
113	93	D6	73	B5	P63	E	K
					TIOB15_1		
					INT03_0		
					MWEX_0		
	-	-	-	-	SIN5_1		
114	94	C5	74	C5	P62	E	K
					ADTG_3		
					SCK5_0 (SCL5_0)		
					TIOA15_1		
					INT07_1		
					MOEX_0		
115	95	B4	75	B4	P61	E	J
					SOT5_0 (SDA5_0)		
					TIOB2_2		
116	96	C4	76	C4	P60	H[1]	Q
					SIN5_0		
					IGTRG_1		
					TIOA2_2		
					INT15_1		
					WKUP3		
					CEC1_0		
					MRDY_0		

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
External Bus	MADATA13_0		15	15	F3	-	-
	MADATA14_0		16	16	G1	-	-
	MADATA15_0		17	17	G2	-	-
	MALE_0	Latch enable signal for multiplex	104	89	B6	69	B7
	MRDY_0	External RDY input signal	116	96	C4	76	C4
	MCLKOUT_0	External bus clock output pin	99	84	A7	66	A8
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2	C1	2	C1
	INT00_1		97	82	C8	-	-
	INT00_2		102	87	D7	67	C8
	INT01_0	External interrupt request 01 input pin	3	3	C2	3	C2
	INT01_1		98	83	D9	-	-
	INT01_2		85	-	-	-	-
	INT02_0	External interrupt request 02 input pin	4	4	B3	4	B3
	INT02_1		63	53	J10	43	J10
	INT02_2		82	-	-	-	-
	INT03_0	External interrupt request 03 input pin	113	93	D6	73	B5
	INT03_1		66	56	H9	46	H9
	INT03_2		14	9	E1	9	E2
	INT04_0	External interrupt request 04 input pin	17	12	E4	12	G2
	INT04_1		69	59	G9	49	F10
	INT04_2		15	10	E2	10	E3
	INT05_0	External interrupt request 05 input pin	89	74	C10	60	C10
	INT05_1		75	65	F9	55	E10
	INT05_2		16	11	E3	11	G1
	INT06_0	External interrupt request 06 input pin	23	18	F4	13	G3
	INT06_1		88	73	C11	59	C11
	INT06_2		50	45	K8	35	K8
	INT07_0	External interrupt request 07 input pin	24	19	G3	14	H1
	INT07_1		114	94	C5	74	C5
	INT07_2		5	5	D1	5	D1
	INT08_0	External interrupt request 08 input pin	34	29	K5	-	-
	INT08_1		19	14	F2	-	-
	INT08_2		8	8	D5	8	E1
	INT09_0	External interrupt request 09 input pin	35	30	J5	-	-
	INT09_1		20	15	F3	-	-
	INT09_2		11	-	-	-	-
	INT10_0	External interrupt request 10 input pin	36	31	H5	21	L5
	INT10_1		21	16	G1	-	-
	INT10_2		112	-	-	-	-
	INT11_0	External interrupt request 11 input pin	37	32	L6	22	K5
	INT11_1		22	17	G2	-	-
	INT11_2		110	-	-	-	-

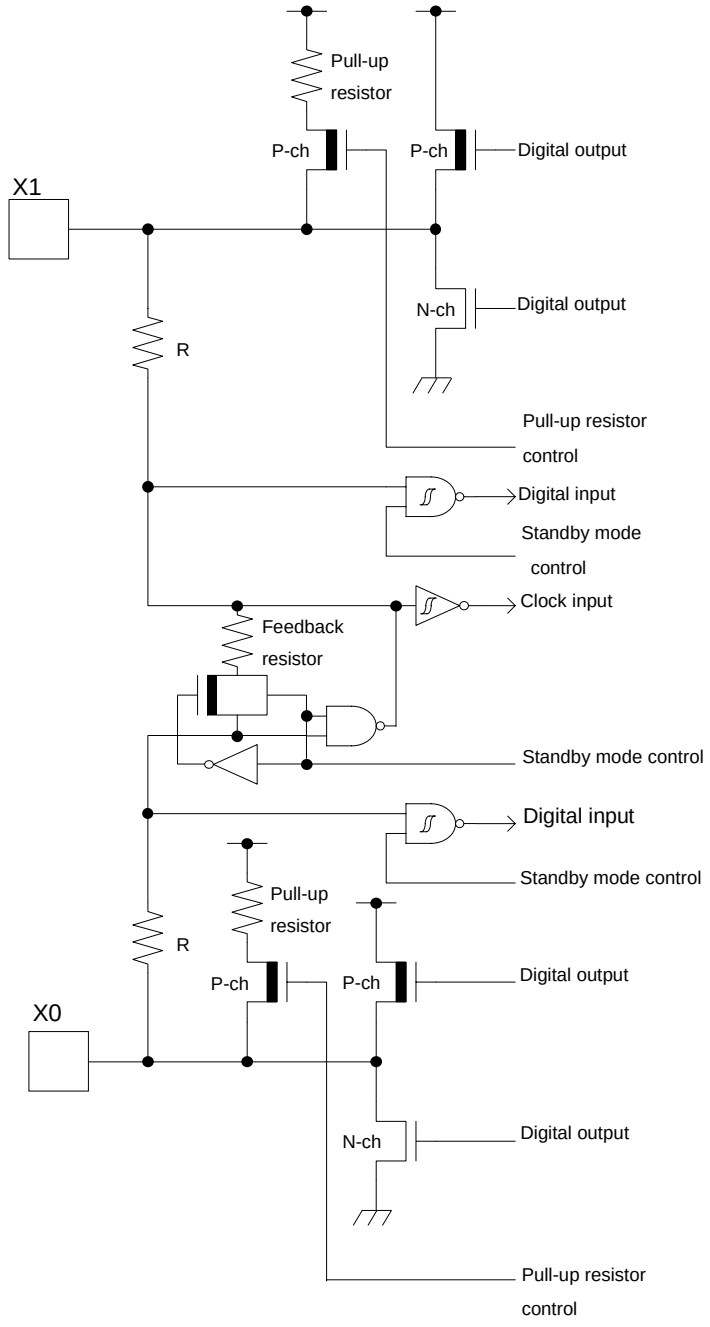
Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Multi- function Serial 10	SIN10_0	Multi-function serial interface ch.10 input pin	23	18	F4	13	G3
	SOT10_0 (SDA10_0)	Multi-function serial interface ch.10 output pin. This pin operates as SOT10 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA10 when it is used in an I^2C (operation mode 4).	24	19	G3	14	H1
	SCK10_0 (SCL10_0)	Multi-function serial interface ch.10 clock I/O pin. This pin operates as SCK10 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL10 when it is used in an I^2C (operation mode 4).	25	20	H1	15	H2
Multi- function Serial 11	SIN11_0	Multi-function serial interface ch.11 input pin	26	21	H2	16	H3
	SOT11_0 (SDA11_0)	Multi-function serial interface ch.11 output pin. This pin operates as SOT11 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA11 when it is used in an I^2C (operation mode 4).	27	22	G4	17	J1
	SCK11_0 (SCL11_0)	Multi-function serial interface ch.11 clock I/O pin. This pin operates as SCK11 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL11 when it is used in an I^2C (operation mode 4).	28	23	H3	18	J2

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Multi- function Serial 12	SIN12_0	Multi-function serial interface ch.12 input pin	32	27	J4	-	-
	SOT12_0 (SDA12_0)	Multi-function serial interface ch.12 output pin. This pin operates as SOT12 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA12 when it is used in an I^2C (operation mode 4).	33	28	L5	-	-
	SCK12_0 (SCL12_0)	Multi-function serial interface ch.12 clock I/O pin. This pin operates as SCK12 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL12 when it is used in an I^2C (operation mode 4).	34	29	K5	-	-
Multi- function Serial 13	SIN13_0	Multi-function serial interface ch.13 input pin	35	30	J5	-	-
	SOT13_0 (SDA13_0)	Multi-function serial interface ch.13 output pin. This pin operates as SOT13 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA13 when it is used in an I^2C (operation mode 4).	36	31	H5	-	-
	SCK13_0 (SCL13_0)	Multi-function serial interface ch.13 clock I/O pin. This pin operates as SCK13 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL13 when it is used in an I^2C (operation mode 4).	37	32	L6	-	-

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Multi- function Timer 0	RTO00_0 (PPG00_0)	Waveform generator output pin of multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	24	19	G3	14	H1
	RTO00_1 (PPG00_1)		86	71	D10	57	D10
	RTO01_0 (PPG00_0)	Waveform generator output pin of multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	25	20	H1	15	H2
	RTO01_1 (PPG00_1)		85	-	-	-	-
	RTO02_0 (PPG02_0)	Waveform generator output pin of multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	26	21	H2	16	H3
	RTO02_1 (PPG02_1)		84	-	-	-	-
	RTO03_0 (PPG02_0)	Waveform generator output pin of multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	27	22	G4	17	J1
	RTO03_1 (PPG02_1)		83	-	-	-	-
	RTO04_0 (PPG04_0)	Waveform generator output pin of multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	28	23	H3	18	J2
	RTO04_1 (PPG04_1)		82	-	-	-	-
	RTO05_0 (PPG04_0)	Waveform generator output pin of multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	29	24	J2	19	J4
	RTO05_1 (PPG04_1)		81	-	-	-	-
	IGTRG_0	PPG IGMT mode external trigger input pin	46	41	L7	31	J6
	IGTRG_1		116	96	C4	76	C4

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin	14	9	E1	9	E2
	AIN0_1		45	40	J6	30	K6
	AIN0_2		2	2	C1	2	C1
	BIN0_0	QPRC ch.0 BIN input pin	15	10	E2	10	E3
	BIN0_1		46	41	L7	31	J6
	BIN0_2		3	3	C2	3	C2
	ZIN0_0	QPRC ch.0 ZIN input pin	16	11	E3	11	G1
	ZIN0_1		47	42	K7	32	L7
	ZIN0_2		4	4	B3	4	B3
Quadrature Position/ Revolution Counter 1	AIN1_1	QPRC ch.1 AIN input pin	89	74	C10	60	C10
	AIN1_2		48	43	H6	33	K7
	BIN1_1	QPRC ch.1 BIN input pin	88	73	C11	59	C11
	BIN1_2		49	44	J7	34	J7
	ZIN1_1	QPRC ch.1 ZIN input pin	87	72	E8	58	D9
	ZIN1_2		50	45	K8	35	K8
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	107	92	B5	72	A6
	RTCCO_1		65	55	H10	45	H10
	RTCCO_2		24	19	G3	14	H1
	SUBOUT_0	Sub clock output pin	107	92	B5	72	A6
	SUBOUT_1		65	55	H10	45	H10
	SUBOUT_2		24	19	G3	14	H1
Low-Power Consumption Mode	WKUP0	Deep standby mode return signal input pin 0	107	92	B5	72	A6
	WKUP1	Deep standby mode return signal input pin 1	63	53	J10	43	J10
	WKUP2	Deep standby mode return signal input pin 2	88	73	C11	59	C11
	WKUP3	Deep standby mode return signal input pin 3	116	96	C4	76	C4
	WKUP4	Deep standby mode return signal input pin 4	14	9	E1	9	E2
	WKUP5	Deep standby mode return signal input pin 5	102	87	D7	67	C8
HDMI-CEC/ Remote Control Reception	CEC0_0	HDMI-CEC/Remote Control Reception ch.0 input/output pin	48	43	H6	33	K7
	CEC0_1		103	88	A6	68	C7
	CEC1_0	HDMI-CEC/Remote Control Reception ch.1 input/output pin	116	96	C4	76	C4
	CEC1_1		8	8	D5	8	E1

5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. ■ Oscillation feedback resistor: Approximately 1 MΩ ■ With standby mode control When the GPIO is selected. ■ CMOS level output. ■ CMOS level hysteresis input ■ With pull-up resistor control ■ With standby mode control ■ Pull-up resistor: Approximately 33 kΩ ■ I_{OH}= -4 mA, I_{OL}= 4 mA

■ Lead-Free Packaging

CAUTION:

When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■ Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C. When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■ Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

■ Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame

CAUTION:

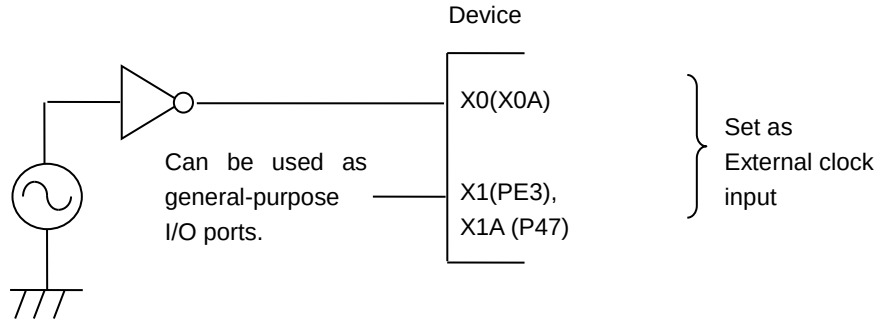
Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

7.5 Using an external clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port. Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

Example of Using an External Clock

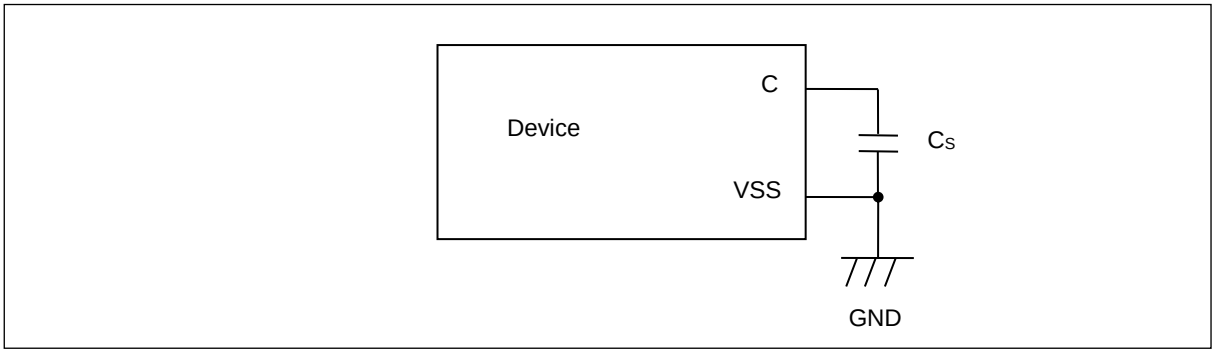


7.6 Handling when using Multi-function serial pin as I²C pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

7.7 C pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor. However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor. A smoothing capacitor of about 4.7 µF would be recommended for this series.



7.8 Mode pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistor stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep standby Rtc mode or Deep standby Stop mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
S	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected							GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									

[1]. Oscillation is stopped at Sub Timer mode, Low-speed CR Timer mode, RTC mode, Stop mode, Deep Standby RTC mode, and Deep Standby Stop mode.

[2]. Oscillation is stopped at Stop mode and Deep Standby Stop mode.

12.3.2 *Pin Characteristics*

(V_{CC} = AV_{CC} = 1.65V to 3.6V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input Voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	$V_{CC} \geq 2.7$ V	$V_{CC} \times 0.8$	-	$V_{CC} + 0.3$	V	
			$V_{CC} < 2.7$ V	$V_{CC} \times 0.7$				
		5V tolerant input pin	$V_{CC} \geq 2.7$ V	$V_{CC} \times 0.8$	-	$V_{SS} + 5.5$	V	
			$V_{CC} < 2.7$ V	$V_{CC} \times 0.7$				
L level input Voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	$V_{CC} \geq 2.7$ V	V_{SS} - 0.3	-	$V_{CC} \times 0.2$	V	
			$V_{CC} < 2.7$ V			$V_{CC} \times 0.3$		
		5 V tolerant input pin	$V_{CC} \geq 2.7$ V	V_{SS} - 0.3	-	$V_{CC} \times 0.2$	V	
			$V_{CC} < 2.7$ V			$V_{CC} \times 0.3$		
H level output voltage	V_{OH}	4mA type	$V_{CC} \geq 2.7$ V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			$V_{CC} < 2.7$ V, I_{OH} = - 2 mA	V_{CC} - 0.45				
L level output voltage	V_{OL}	4mA type	$V_{CC} \geq 2.7$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 2.7$ V, I_{OL} = 2 mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
		CEC0_0, CEC0_1, CEC1_0, CEC1_1	V_{CC} = AV_{CC} = AVRH = V_{SS} = AV_{SS} = 0.0 V	-	-	+1.8	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	$V_{CC} \geq 2.7$ V	21	33	66	kΩ	
			$V_{CC} < 2.7$ V	-	-	134		
Input capacitance	C_{IN}	Other than VCC, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

12.4.7 *External Bus Timing*

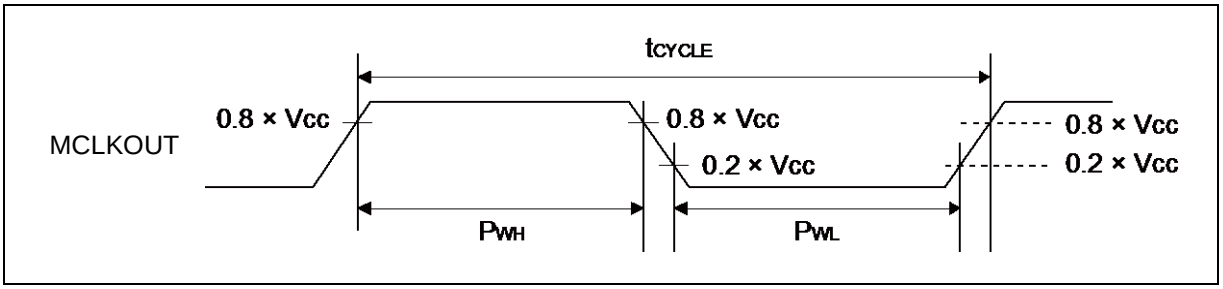
12.4.7.1 External bus clock output characteristics

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{CYCLE}	MCLKOUT[1]	$V_{CC} \geq 2.7$ V	-	40	MHz
			$V_{CC} < 2.7$ V	-	20	MHz

The external bus clock (MCLKOUT) is a divided clock of HCLK. For more information about setting of clock divider, see Chapter 12: External Bus Interface in FM3 Family Peripheral Manual..

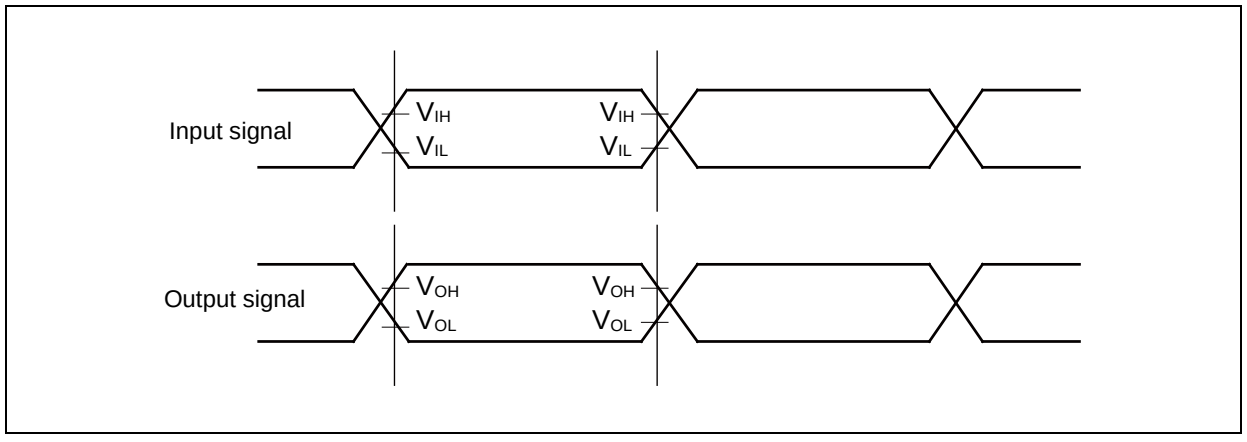
When external bus clock is not output, this characteristic does not give any effect on external bus operation.



12.4.7.2 External bus signal input/output characteristics

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	



12.4.7.4 Separate Bus Access Synchronous SRAM Mode

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Address delay time	t_{AV}	MCLK, MAD[24:0]	$V_{CC} \geq 2.7$ V	1	9	ns
			$V_{CC} < 2.7$ V		12	
MCSX delay time	t_{CSL}	MCLK, MCSX[7:0]	$V_{CC} \geq 2.7$ V	1	9	ns
			$V_{CC} < 2.7$ V		12	
	t_{CSH}		$V_{CC} \geq 2.7$ V	1	9	ns
			$V_{CC} < 2.7$ V		12	
MOEX delay time	t_{REL}	MCLK, MOEX	$V_{CC} \geq 2.7$ V	1	9	ns
			$V_{CC} < 2.7$ V		12	
	t_{REH}		$V_{CC} \geq 2.7$ V	1	9	ns
			$V_{CC} < 2.7$ V		12	
Data set up →MCLK ↑ time	t_{DS}	MCLK, MADATA[15:0]	$V_{CC} \geq 2.7$ V	19	-	ns
			$V_{CC} < 2.7$ V	37		
MCLK ↑ → Data hold time	t_{DH}	MCLK, MADATA[15:0]	$V_{CC} \geq 2.7$ V	0	-	ns
			$V_{CC} < 2.7$ V			
MWEX delay time	t_{WEL}	MCLK, MWEX	$V_{CC} \geq 2.7$ V	1	9	ns
			$V_{CC} < 2.7$ V		12	
	t_{WEH}		$V_{CC} \geq 2.7$ V	1	9	ns
			$V_{CC} < 2.7$ V		12	
MDQM[1:0] delay time	t_{DQML}	MCLK, MDQM[1:0]	$V_{CC} \geq 2.7$ V	1	9	ns
			$V_{CC} < 2.7$ V		12	
	t_{DQMH}		$V_{CC} \geq 2.7$ V	1	9	ns
			$V_{CC} < 2.7$ V		12	
MCLK ↑ → Data output time	t_{ODS}	MCLK, MADATA[15:0]	$V_{CC} \geq 2.7$ V	MCLK+1	MCLK+18	ns
			$V_{CC} < 2.7$ V		MCLK+24	
MCLK ↑ → Data hold time	t_{OD}	MCLK, MADATA[15:0]	$V_{CC} \geq 2.7$ V	1	18	ns
			$V_{CC} < 2.7$ V		24	

Note:

- *When the external load capacitance C_L = 30 pF.*

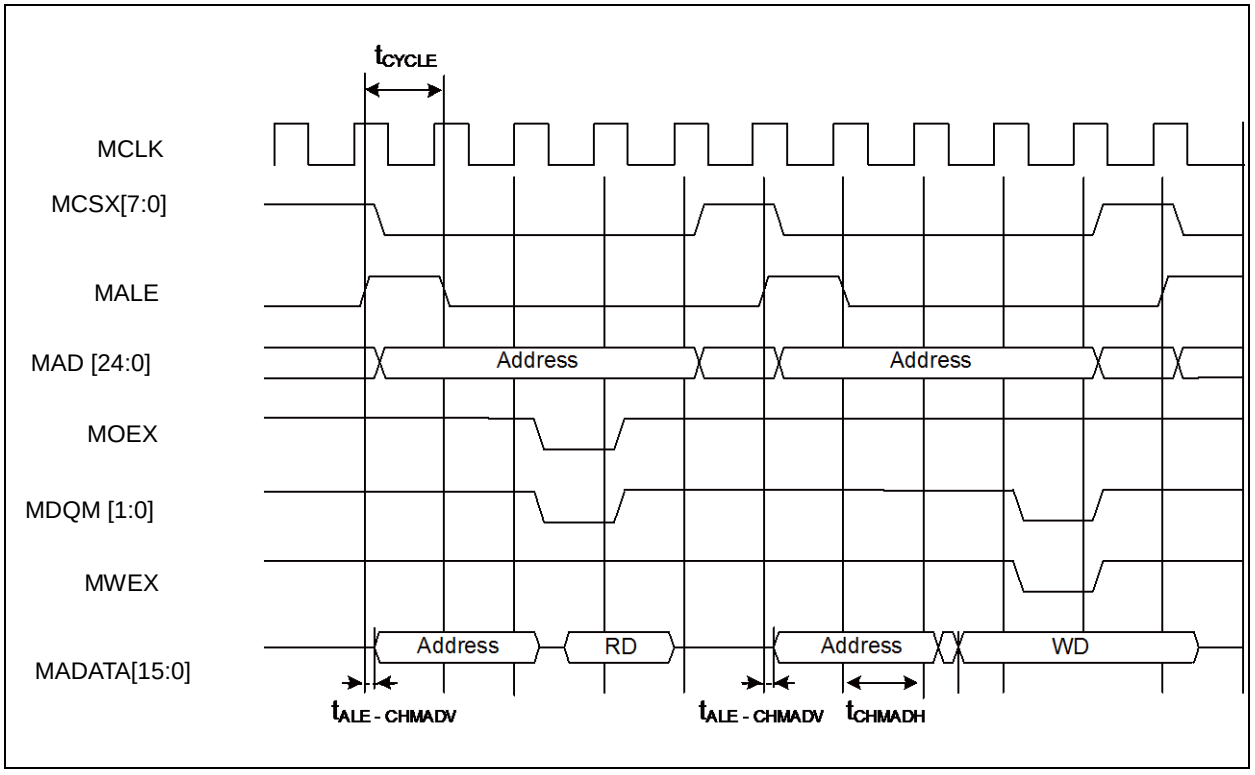
12.4.7.5 Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE, MADATA[15:0]	$V_{CC} \geq 2.7$ V	0	+10	ns
			$V_{CC} < 2.7$ V		+20	
Multiplexed address hold time	t_{CHMADH}		$V_{CC} \geq 2.7$ V	MCLK×n+0	MCLK×n+10	ns
			$V_{CC} < 2.7$ V	MCLK×n+0	MCLK×n+20	

Note:

- *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16).*



12.4.7.7 NAND Flash Memory Mode

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
MNREX Min pulse width	t_{NREW}	MNREX	$V_{CC} \geq 2.7$ V	MCLK×n-3	-	ns
			$V_{CC} < 2.7$ V			
Data setup → MNREX↑time	t_{DS-NRE}	MNREX, MADATA[15:0]	$V_{CC} \geq 2.7$ V	20	-	ns
			$V_{CC} < 2.7$ V	38	-	
MNREX↑→ Data hold time	t_{DH-NRE}	MNREX, MADATA[15:0]	$V_{CC} \geq 2.7$ V	0	-	ns
			$V_{CC} < 2.7$ V			
MNALE↑→MNWEX delay time	$t_{ALEH-NWEL}$	MNALE, MNWEX	$V_{CC} \geq 2.7$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 2.7$ V	MCLK×m-12	MCLK×m+12	
MNALE↓→MNWEX delay time	$t_{ALEL-NWEL}$	MNALE, MNWEX	$V_{CC} \geq 2.7$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 2.7$ V	MCLK×m-12	MCLK×m+12	
MNCLE↑→MNWEX delay time	$t_{CLEH-NWEL}$	MNCLE, MNWEX	$V_{CC} \geq 2.7$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 2.7$ V	MCLK×m-12	MCLK×m+12	
MNWEX↑→MNCLE delay time	$t_{NWEH-CLEL}$	MNCLE, MNWEX	$V_{CC} \geq 2.7$ V	0	MCLK×m+9	ns
			$V_{CC} < 2.7$ V		MCLK×m+12	
MNWEX Min pulse width	t_{NWEW}	MNWEX	$V_{CC} \geq 2.7$ V	MCLK×n-3	-	ns
			$V_{CC} < 2.7$ V			
MNWEX↓→Data output time	$t_{NWEL-DV}$	MNWEX, MADATA[15:0]	$V_{CC} \geq 2.7$ V	- 9	+ 9	ns
			$V_{CC} < 2.7$ V	-12	+12	
MNWEX↑→Data hold time	$t_{NWEH-DX}$	MNWEX, MADATA[15:0]	$V_{CC} \geq 2.7$ V	0	MCLK×m+9	ns
			$V_{CC} < 2.7$ V		MCLK×m+12	

Note:

- *When the external load capacitance C_L = 30 pF (m=0 to 15, n=1 to 16).*

Figure 1. NAND Flash Memory Read

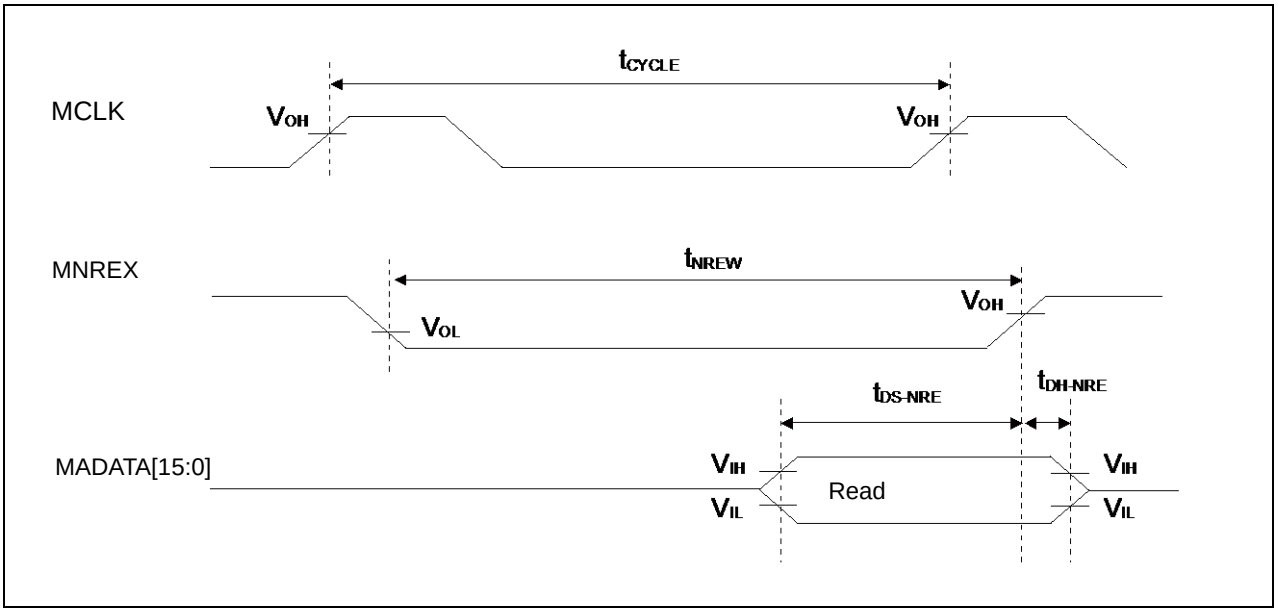
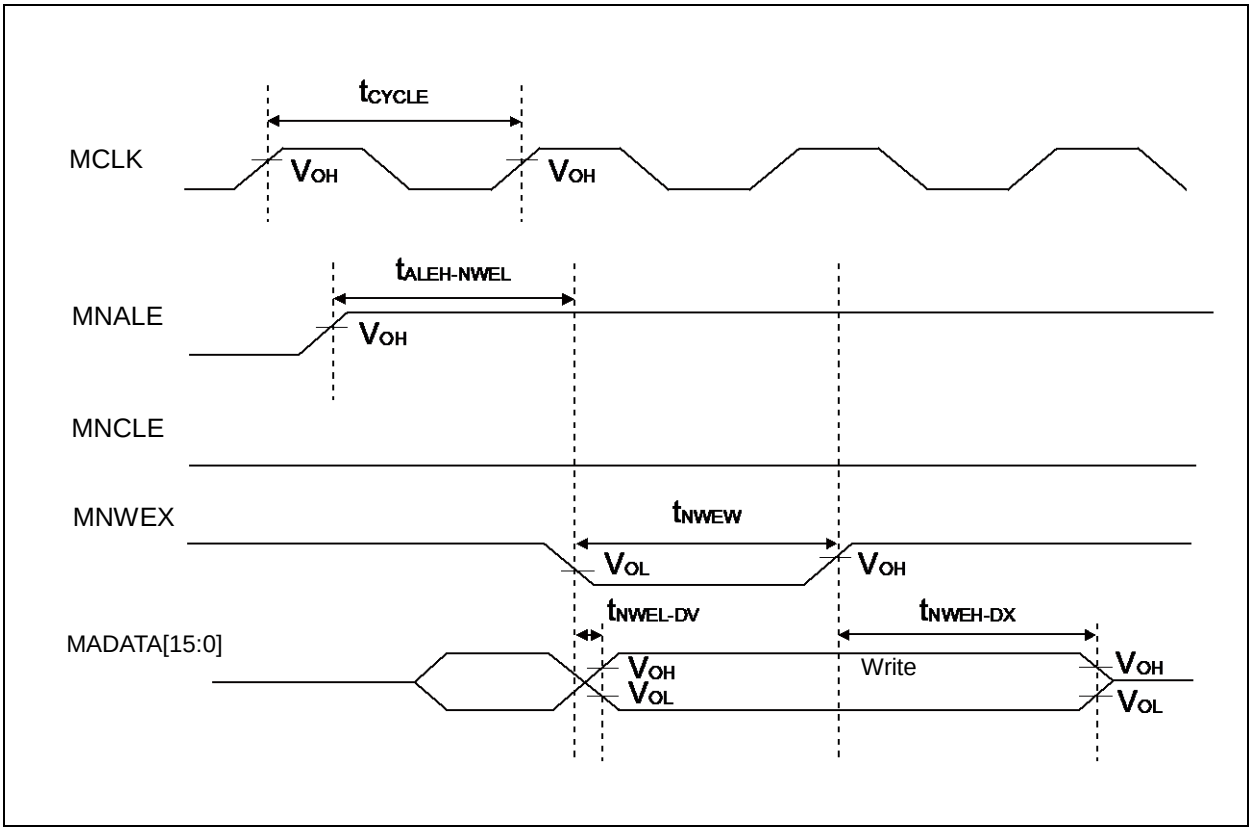
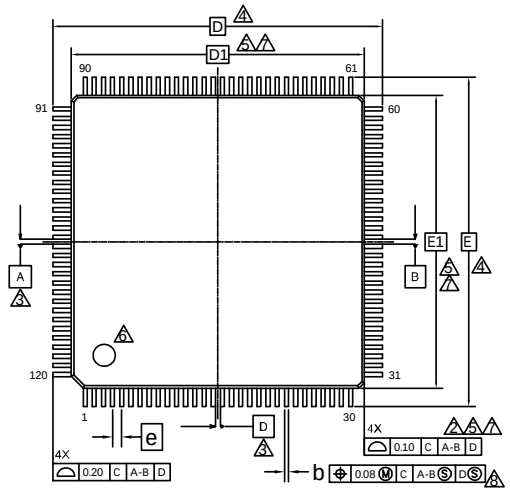


Figure 2. NAND Flash Memory Address Write

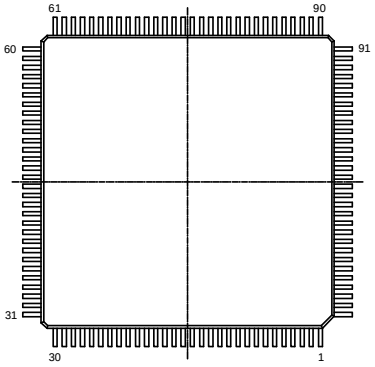


14. Package Dimensions

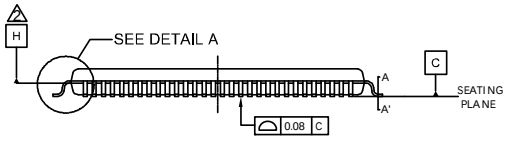
Package Type	Package Code
LQFP 120	LQM120



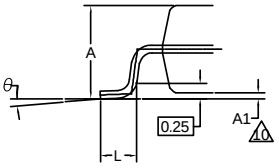
TOP VIEW



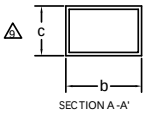
BOTTOM VIEW



SIDE VIEW



DETAIL A



SECTION A-A'

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.115	—	0.195
D	18.00 BSC		
D1	16.00 BSC		
e	0.50 BSC		
E	18.00 BSC		
E1	16.00 BSC		
L	0.45	0.60	0.75
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
11. JEDEC SPECIFICATION NO. REF: N/A.

002-16172 **

PACKAGE OUTLINE, 120 LEAD LQFP
18.0X18.0X1.7 MM LQM120 REV**