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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ACE1202
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	8
Program Memory Size	2KB (2K x 8)
Program Memory Type	EEPROM
EEPROM Size	64 x 8
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/ace1202emx

Figure 2: ACEx Application Example (Remote Keyless Entry)

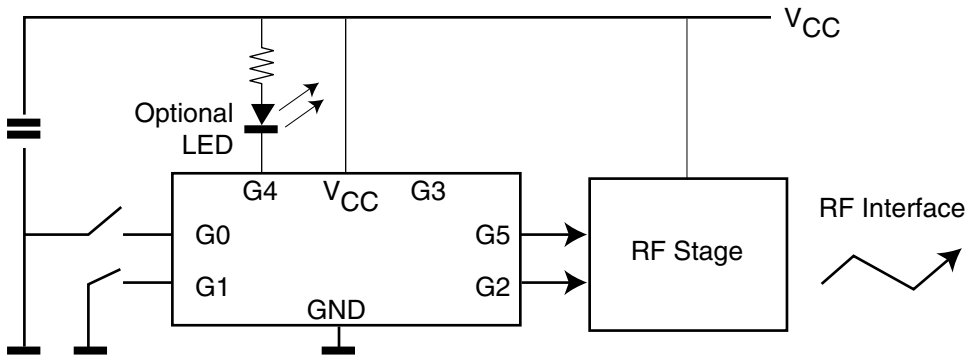
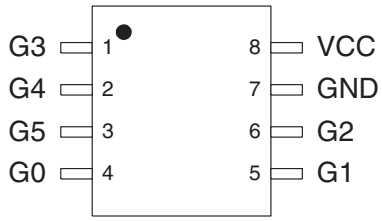


Figure 3: ACE1202/ACE1202-2 8-pin Device Pinout

a) Normal Mode Operation



b) Programming Mode Operation

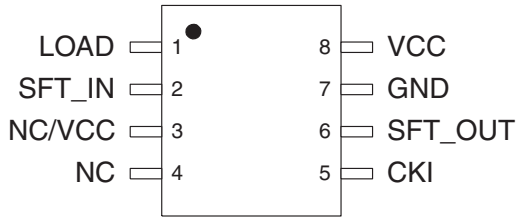
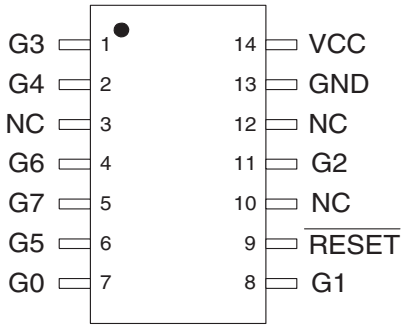
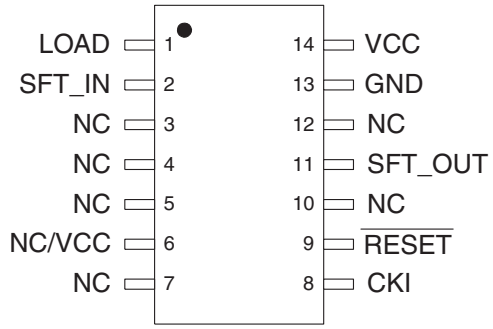


Figure 4: ACE1202/ACE1202-2 14-pin Device Pinout

a) Normal Mode Operation



b) Programming Mode Operation



2.0 Electrical Characteristics

Absolute Maximum Ratings

Ambient Storage Temperature	-65°C to +150°C
Input Voltage not including G3	-0.3V to V_{CC}+0.3V
G3 Input Voltage	0.3V to 13V
Lead Temperature (10s max)	+300°C
Electrostatic Discharge on all pins	2000V min

Operating Conditions

Relative Humidity (non-condensing)	95%
EEPROM write limits	See DC Electrical Characteristics

Part Number	Operating Voltage	Ambient Operating Temperature
ACE1202	2.2 to 5.5V	0°C to 70°C
ACE12022	2.2 to 5.5V	0°C to 70°C
ACE1202E	2.2 to 5.5V	-40°C to +85°C
ACE12022E	2.2 to 5.5V	-40°C to +85°C
ACE1202V	2.2 to 5.5V	-40°C to +125°C
ACE1202B	2.7 to 5.5V	0°C to 70°C
ACE12022B	2.7 to 5.5V	0°C to 70°C
ACE1202BE	2.7 to 5.5V	-40°C to +85°C
ACE12022BE	2.7 to 5.5V	-40°C to +85°C
ACE1202BV	2.7 to 5.5V	-40°C to +125°C
ACE12022BV	2.7 to 5.5V	-40°C to +125°C
ACE1202L	1.8 to 5.5V	0°C to 70°C

Preliminary ACE1202/ACE1202-2 AC Electrical Characteristics

V_{CC} = 1.8/2.2/2.7 to 5.5V

All measurements valid for ambient operating temperature range unless otherwise stated.

Parameter	Conditions	MIN	TYP	MAX	Units
Instruction cycle time from internal clock - setpoint	5.0V at +25°C	0.9	1.0	1.1	µs
Internal clock voltage dependent frequency variation	3.0V to 5.5V, constant temperature			+5	%
Internal clock temperature dependent frequency variation	3.0V to 5.5V, full temperature range			+10	%
Internal clock frequency deviation for 0.5V drop	3.0V to 4.5V, constant temperature			+2	%
Crystal oscillator frequency	(Note 6)			4	MHz
External clock frequency	(Note 7)			4	MHz
EEPROM write time			3	10	ms
Internal clock start up time	(Note 7)			2	ms
Oscillator start up time	(Note 7)			2400	cycles

[6] The maximum permissible frequency is guaranteed by design but not 100% tested.

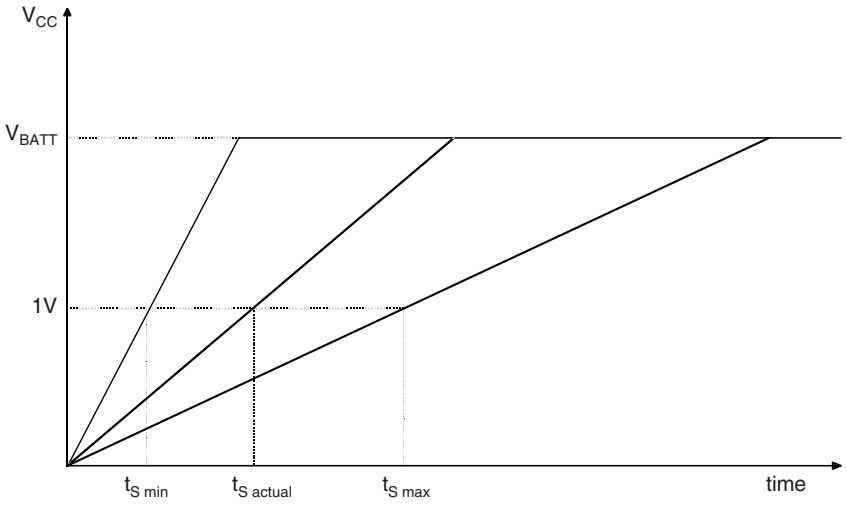
[7] The parameter is guaranteed by design but not 100% tested.

Preliminary ACE1202/ACE1202-2 Electrical Characteristics for programming

All data following is valid between 4.5V and 5.5V at ambient temperature. The following characteristics are guaranteed by design but are not 100% tested. See "EEPROM write time" in the AC Electrical Characteristics for definition of the programming ready time.

Parameter	Description	MIN	MAX	Units
t_{HI}	CLOCK high time	500	DC	ns
t_{LO}	CLOCK low time	500	DC	ns
t_{DIS}	SHIFT_IN setup time	100		ns
t_{DIH}	SHIFT_IN hold time	100		ns
t_{DOS}	SHIFT_OUT setup time	100		ns
t_{DOH}	SHIFT_OUT hold time	900		ns
t_{SV1}, t_{SV2}	LOAD supervoltage timing	50		µs
t_{LOAD1}, t_{LOAD2}, t_{LOAD3}, t_{LOAD4}	LOAD timing	5		µs
$V_{SUPERVOLTAGE}$	Supervoltage level	11.5	12.5	V

Figure 8: Power Supply Rise Time



Name	Parameter	Unit
V_{CC}	Supply Voltage	[V]
V_{BATT}	Battery Voltage (Nominal Operating Voltage)	[V]
$t_{S\ min}$	Minimum Time for V_{CC} to Rise by 1V	[ms]
$t_{S\ actual}$	Actual Time for V_{CC} to Rise by 1V	[ms]
$t_{S\ max}$	Maximum Time for V_{CC} to Rise by 1V	[ms]
S_{VCC}	Power Supply Slope	[ms/V]

6.0 Timer 0

Timer 0 is a 12-bit free running idle timer. Upon power-up or any reset, the timer is reset to 0x000 and then counts up continuously based on the instruction clock of 1MHz (1 s). Software cannot read from or write to this timer. However, software can monitor the timer's pending (T0PND) bit that is set every 8192 cycles (initially 4096 cycles after a reset). The T0PND flag is set every other time the timer overflows (transitions from 0xFFF to 0x000) through a divide-by-2 circuit. After an overflow, the timer will reset and restart its counting sequence.

Software can either poll the T0PND bit or vector to an interrupt subroutine. In order to interrupt on a T0PND, software must be sure to enable the Timer 0 interrupt enable (T0INTEN) bit in the Timer 0 control (T0CNTRL) register and also make sure the G bit is set in SR. Once the timer interrupt is serviced, software should reset the T0PND bit before exiting the routine. Timer 0 supports the following functions:

1. Exiting from IDLE mode (See Section 17.0 for details.)
2. Start up delay from HALT mode
3. Watchdog pre-scaler (See Section 7.0 for details.)

The T0INTEN bit is a read/write bit. If set to 0, interrupt requests from the Timer 0 are ignored. If set to 1, interrupt requests are accepted. Upon reset, the T0INTEN bit is reset to 0.

The T0PND bit is a read/write bit. If set to 1, it indicates that a Timer 0 interrupt is pending. This bit is set by a Timer 0 overflow and is reset by software or system reset.

The WKINTEN bit is used in the Multi-input Wakeup/Interrupt block. See Section 8 for details.

7.0 Watchdog timer

The Watchdog timer is used to reset the device and safely recover in the rare event of a processor "runaway condition." The 12-bit Timer 0 is used as a pre-scaler for Watchdog timer. The Watchdog timer must be serviced before every 61,440 cycles but no sooner than 4096 cycles since the last Watchdog reset. The Watchdog is serviced through software by writing the value 0x1B to the Watchdog Service (WDSVR) register (see Figure 20). The part resets automatically if the Watchdog is serviced too frequent, or not frequent enough.

The Watchdog timer must be enabled through the Watchdog enable bit (WDEN) in the initialization register. The WDEN bit can only be set while the device is in programming mode. Once set, the Watchdog will always be powered-up enabled. Software cannot disable the Watchdog. The Watchdog timer can only be disabled in programming mode by resetting the WDEN bit as long as the memory write protect (WDIS) feature is not enabled.

WARNING

Ensure that the Watchdog timer has been serviced before entering IDLE mode because it remains operational during this time.

Figure 19: Timer 0 Control Register (T0CNTRL)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WKINTEN	x	x	x	x	x	T0PND	T0INTEN

Figure 20: Watchdog Server Register (WDSVR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	1	1	0	1	1

8.0 Hardware Bit-Coder (ACE1202-2 only)

The ACE1202-2 contains a dedicated hardware bit-encoding peripheral block, Hardware Bit-Coder (HBC), for IR/RF data transmission (see Figure 21.) The HBC is completely software programmable and can be configured to emulate various bit-encoding formats. The software developer has the freedom to encode each bit of data into a desired pattern and output the encoded data at the desired frequency through either the G2 or G5 output (TX) ports.

The HBC contains six 8-bit memory-mapped configuration registers PSCALE, HPATTERN, LPATTERN, BPSEL, HBCNTRL, and DAT0. The registers are used to select the transmission frequency, store the data bit-encoding patterns, configure the data bit-pattern/frame lengths, and control the data transmission flow.

To select the IR/RF transmission frequency, an 8-bit divide constant must be written into the IR/RF Pre-scalar (PSCALE) register. The IR/RF transmission frequency generator divides the 1MHz instruction clock down by 4 and the PSCALE register is used to select the desired IR/RF frequency shift. Together, the transmission frequency range can be configured between 976Hz (PSCALE = 0xFF) and 125kHz (PSCALE = 0x01). Upon a reset, the PSCALE register is initialized to zero disabling the IR/RF transmission frequency generator. However, once the PSCALE register is programmed, the desired IR/RF frequency is maintained as long as the device is powered.

Once the transmission frequency is selected, the data bit-encoding patterns must be stored in the appropriate registers. The HBC contains two 8-bit bit-encoding pattern registers, High-pattern (HPATTERN) and Low-pattern (LPATTERN). The encoding pattern stored in the HPATTERN register is transmitted when the data bit value to be encoded is a 1. Similarly, the pattern stored in the LPATTERN register is transmitted when the data bit value to be encoded is a 0. The HBC transmits each encoded pattern MSB first.

The number of bits transmitted from the HPATTERN and LPATTERN registers is software programmable through the Bit Period Configuration (BPSEL) register (see Figure 22). During the transmission of HPATTERN, the number of bits transmitted is configured by BPH[2:0] (BPSEL[2:0]) while BPL[2:0] (BPSEL[5:3]) configures the number of transmitted bits for the LPATTERN. The HBC allows from 2 (0x1) to 8 (0x7) encoding pattern bits to be transmitted from each register. Upon a reset, BPSEL is initially 0 disabling the HBC from transmitting pattern bits from either register.

The Data (DAT0) register is used to store up to 8 bits of data to be encoded and transmitted by the HBC. This data is shifted, bit by bit, MSB to LSB into a 1-bit decision register. If the active bit shifted into the decision register is 1, the pattern in the HPATTERN register is shifted out of the output port. Similarly, if the active bit is 0 the pattern in the LPATTERN register is shifted out.

The HBC control (HBCNTRL) register is used to configure and control the data transmission. HBCNTRL is divided in 5 different controlling signal FRAME[2:0], IOSEL, TXBUSY, START/$\overline{\text{STOP}}$, and OCFLAG (see Figure 23.)

FRAME[2:0] selects the number of bits of DAT0 to encode and transmit. The HBC allows from 2 (0x1) to 8 (0x7) DAT0 bits to be encoded and transmitted. Upon a reset, FRAME is initialized to zero disabling the DAT0's decision register transmitting no data.

The IOSEL signal selects the transmission to output (TX) through either port G2 or G5. If IOSEL is 1, G5 is selected as the output port otherwise G2 is selected.

The TXBUSY signal is read only and is used to inform software that a transmission is in progress. TXBUSY goes high when the encoded data begins to shift out of the output port and will remains high during each consecutive DAT0 frame bit transmission (see Figure 25). The HBC will clear the TXBUSY signal when the last DAT0 encoded bit of the frame is transmitted and the STOP signal is 0.

The START / $\overline{\text{STOP}}$ signal controls the encoding and transmission process for each data frame. When software sets the START / $\overline{\text{STOP}}$ bit the DAT0 frame transmission process begins. The START signal will remain high until the beginning of the last encoded DAT0 frame bit transmission. The HBC then clears the START / $\overline{\text{STOP}}$ bit allowing software to either continue with a new DAT0 frame transmission or stop the transmission all together (see Figure 25). If TXBUSY is 0 when the START signal is enabled, a synchronization period occurs before any data is transmitted lasting the amount of time to transmit a 0 encoded bit (see Figure 24).

The OCFLAG signal is read only and goes high when the last encoded bit of the DAT0 frame is transmitting. The OCFLAG signal is used to inform software that the DAT0 frame transmission operation is completing (see Figure 25). If multiple DAT0 frames are to be transmitted consecutively, software should poll the OCFLAG signal for a 1. Once OCFLAG is 1, DAT0 must be reload and the START / $\overline{\text{STOP}}$ bit must be restored to 1 in order to begin the new frame transmission without interruptions (the synchronization period). Since OCFLAG remains high during the entire last encoded DAT0 frame bit transmission, software should wait for the HBC to clear the OCFLAG signal before polling for the new OCFLAG high pulse. If new data is not reloaded into DAT0 and the START signal ($\overline{\text{STOP}}$ is active) is not set before the OCFLAG is 0, the transmission process will end (TXBUSY is cleared) and a new process will begin starting with the synchronization period.

Figure 24 and 25 shows how the HBC performs its data encoding. In the example, two frames are encoded and transmitted consecutively with the following bit encoding format specification:

1. Transmission frequency = 62.5KHz
2. Data to be encoded = 0x52, 0x92 (all 8-bits)
3. Each bit should be encoded as a 3-bit binary value, '1' = 110b and '0' = 100b
4. Transmission output port : G2

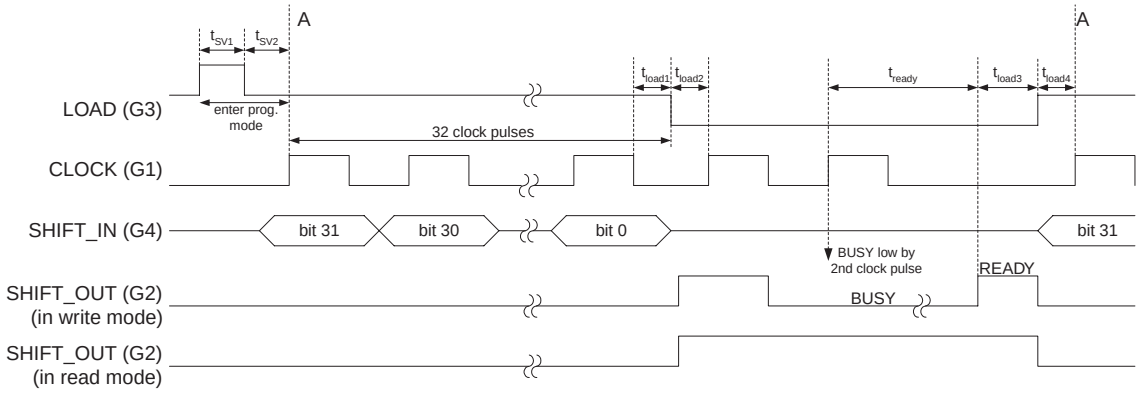
To perform the data transmission, software must first initialize the PSCALE, BPSEL, HPATTERN, LPATTERN, and DAT0 registers with the appropriate values.

```
LD  PSCALE, #03H        ; (1MHz   4)   4 = 62.5KHz
LD  BPSEL, #012H        ; BPH = 2, BPL = 2 (3 bits each)
LD  HPATTERN, #0C0H     ; HPATTERN = 0xC0
LD  LPATTERN, #090H     ; LPATTERN = 0x90
LD  DAT0, #052H         ; DAT0 = 0x52
```

Once the basic registers are initialized, the HBC can be started. (At the same time, software must set the number of data bits per data frame and select the desired output port.)

```
LD  HBCNTRL, #27H       ; START / STOP = 1,
                          FRAME = 7, IOSEL = 0
```

Figure 30: Programming Protocol[16]



A: start of programming cycle

Figure 31: Serial Data Timing