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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ACE1202
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	6
Program Memory Size	2KB (2K x 8)
Program Memory Type	EEPROM
EEPROM Size	64 x 8
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/ace1202lem8x

Preliminary ACE1202/ACE1202-2 DC Electrical Characteristics

V_{CC} = 1.8/2.2/2.7 to 5.5V

All measurements valid for ambient operating temperature range unless otherwise stated.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
I_{CC}[4]	Supply Current – no data EEPROM write in progress	1.8V 2.2V 2.7V 3.3V 5.5V		0.2 0.4 0.7 1.2 3.7	0.5 1.0 1.2 2.0 5.5	mA mA mA mA mA
I_{CCH}	HALT Mode current	3.3V @ -40°C to +25°C 5.5V @ -40°C to +25°C 3.3V @ +85°C 5.5V @ +85°C 3.3V @ +125°C 5.5V @+125°C		10 60 75 400 600 1550	100 1000 1000 2500 5000 8000	nA nA nA nA nA nA
I_{CCL}[5]	IDLE Mode Current	3.3V 5.5V		150 200	200 300	µA µA
V_{CCW}	EEPROM Write Voltage	Code EEPROM in Programming Mode	4.5	5.0	5.5	V
		Data EEPROM in Operating Mode	2.4		5.5	V
S_{VCC}	Power Supply Slope		1µs/V		10ms/V	
V_{IL}	Input Low with Schmitt Trigger Buffer	V_{CC} = 1.8 -5.5V			$0.2V_{CC}$	V
V_{IH}	Input High with Schmitt Trigger Buffer	V_{CC} = 1.8 - 5.5V	$0.8V_{CC}$			V
I_{IP}	Input Pull-up Current	V_{CC} =5.5V, V_{IN} =0V	30	65	350	µA
I_{TL}	TRI-STATE Leakage	V_{CC} =5.5V		2	200	nA
V_{OL}	Output Low Voltage	V_{CC} = 1.8 - 2.2V				
	G0, G1, G2, G4, G6, G7	0.8 mA sink			$0.2V_{CC}$	V
	G5	1.0 mA sink			$0.2V_{CC}$	V
	Output Low Voltage	V_{CC} = 2.2V – 3.3V				
	G0, G1, G2, G4, G6, G7	3.0 mA sink			$0.2V_{CC}$	V
	G5	5.0 mA sink			$0.2V_{CC}$	V
	Output Low Voltage	V_{CC} = 3.3V – 5.5V				
	G0, G1, G2, G4, G6, G7	5.0 mA sink			$0.2V_{CC}$	V
	G5	10.0 mA sink			$0.2V_{CC}$	V
V_{OH}	Output High Voltage	V_{CC} = 1.8 - 2.2V				
	G0, G1, G2, G4, G6, G7	0.1 mA source	$0.8V_{CC}$			V
	G5	0.2 mA source	$0.8V_{CC}$			V
	Output High Voltage	V_{CC} = 3.3V – 5.5V				
	G0, G1, G2, G4, G6, G7	0.4 mA source	$0.8V_{CC}$			V
	G5	0.8 mA source	$0.8V_{CC}$			V
	Output High Voltage	V_{CC} = 3.3V – 5.5V				
	G0, G1, G2, G4, G6, G7	0.4 mA source	$0.8V_{CC}$			V
	G5	1.0 mA source	$0.8V_{CC}$			V

[4] I_{CC} active current is dependent on the program code.

[5] Based on a continuous IDLE looping program.

Preliminary ACE1202/ACE1202-2 Low Battery Detect (LBD) Characteristics

V_{CC} = 2.2/1.8 to 5.5V

The following characteristics are guaranteed by design but are not 100% tested.

Parameter	Conditions	MIN	TYP	MAX	Units
LBD Voltage Threshold	Level 1 @ -40°C		2.84		V
	Level 8 @ -40°C		2.02		V
	Level 1 @ 0°C		2.98		V
	Level 8 @ 0°C		2.05		V
	Level 1 @ -25°C		3.08		V
	Level 8 @ +25°C		2.12		V
	Level 1 @ +85°C		3.31		V
	Level 8 @ +85°C		2.27		V
	Level 1 @ +125°C		3.36		V
	Level 8 @ +125°C		2.40		V

Preliminary ACE1202/ACE1202-2 Brown-out Reset (BOR) Characteristics

V_{CC} = 2.2 to 5.5V

The following characteristics are guaranteed by design but are not 100% tested.

Parameter	Conditions	MIN	TYP	MAX	Units
BOR Trigger Threshold	-40°C		1.98		V
	0°C		2.06		V
	+25°C		2.12		V
	+85°C		2.27		V
	+125°C		2.37		V

Preliminary ACE1202L Brown-out Reset (BOR) Characteristics

V_{CC} = 1.8 to 5.5V

The following characteristics are guaranteed by design but are not 100% tested.

Parameter	Conditions	MIN	TYP	MAX	Units
BOR Trigger Threshold	0°C		1.78		V
	+25°C		1.82		V
	+70°C		1.96		V

3.0 AC & DC Electrical Characteristic Graphs

Figure 5: RC Oscillator Frequency vs. Temperature (V_{CC}=5.0V)

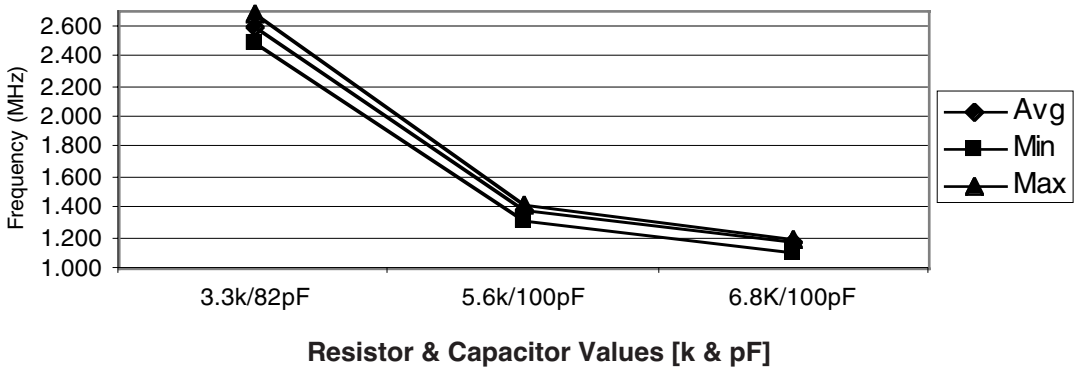


Figure 6: RC Oscillator Frequency vs. Temperature(V_{CC}=2.5V)

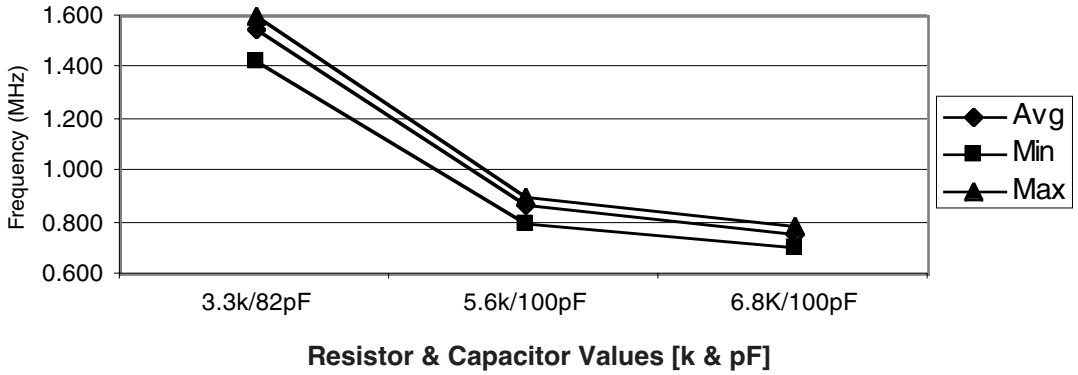


Figure 7: Internal Oscillator Frequency

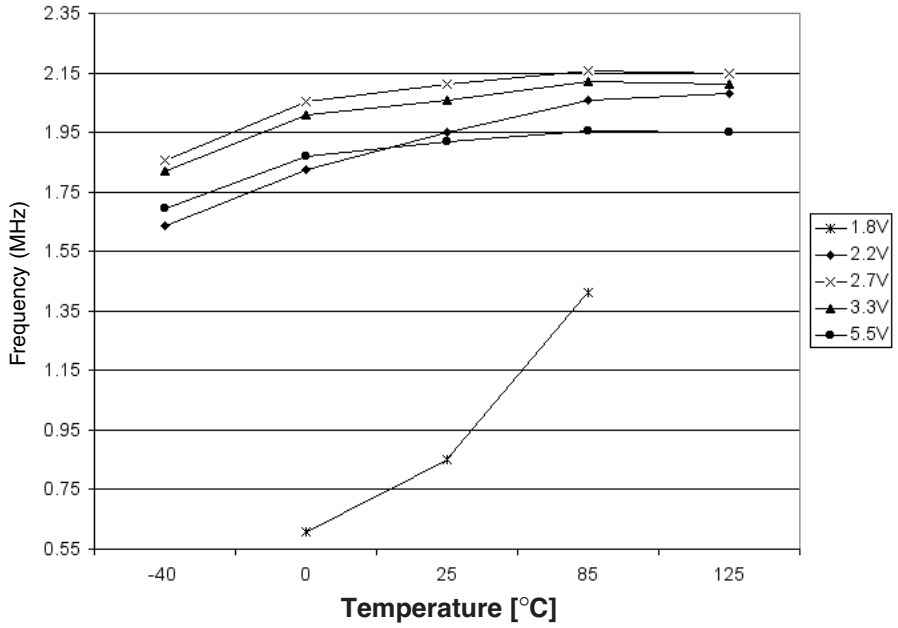
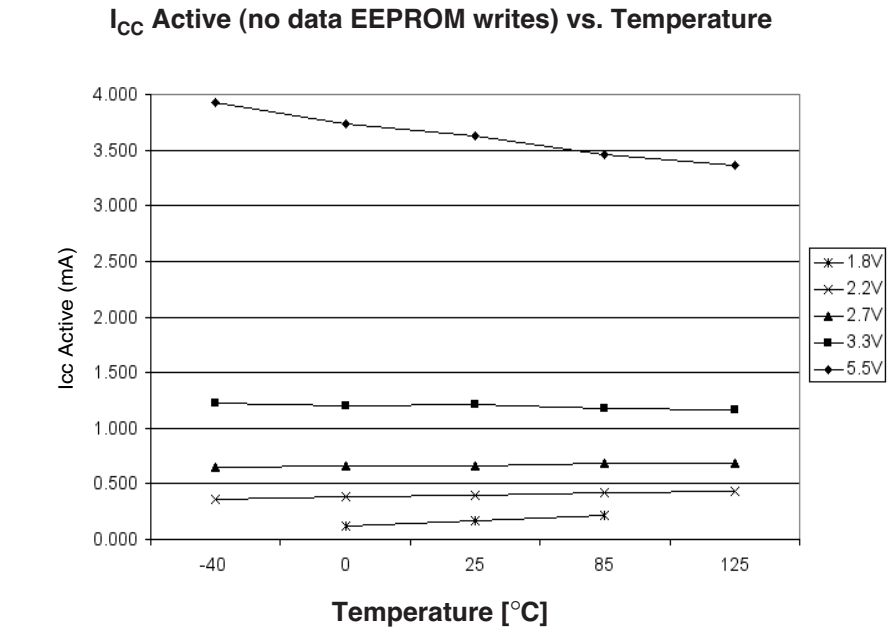


Figure 9: I_{CC} Active



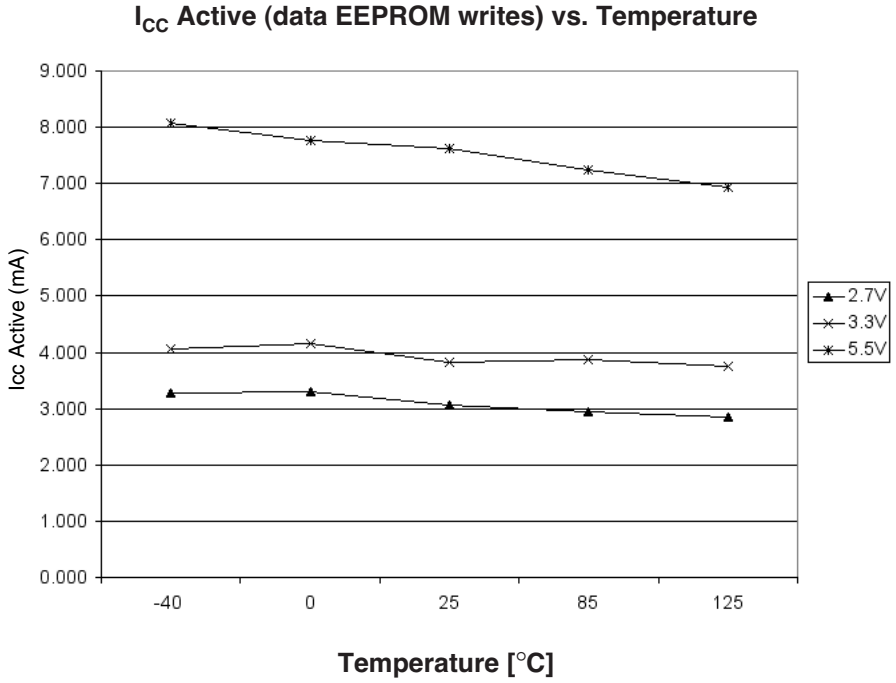


Figure 10: HALT Mode Currents

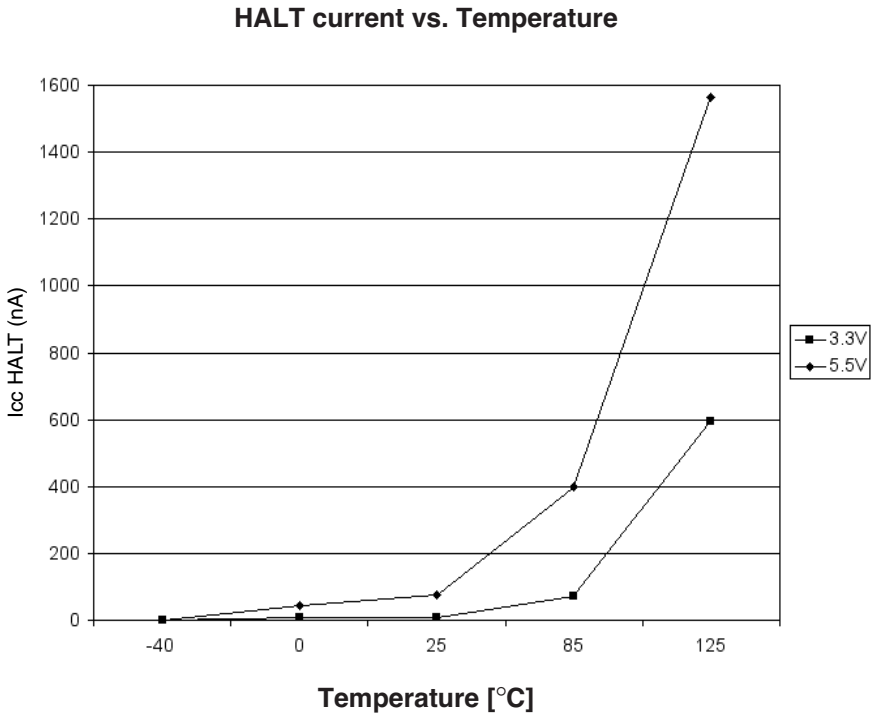
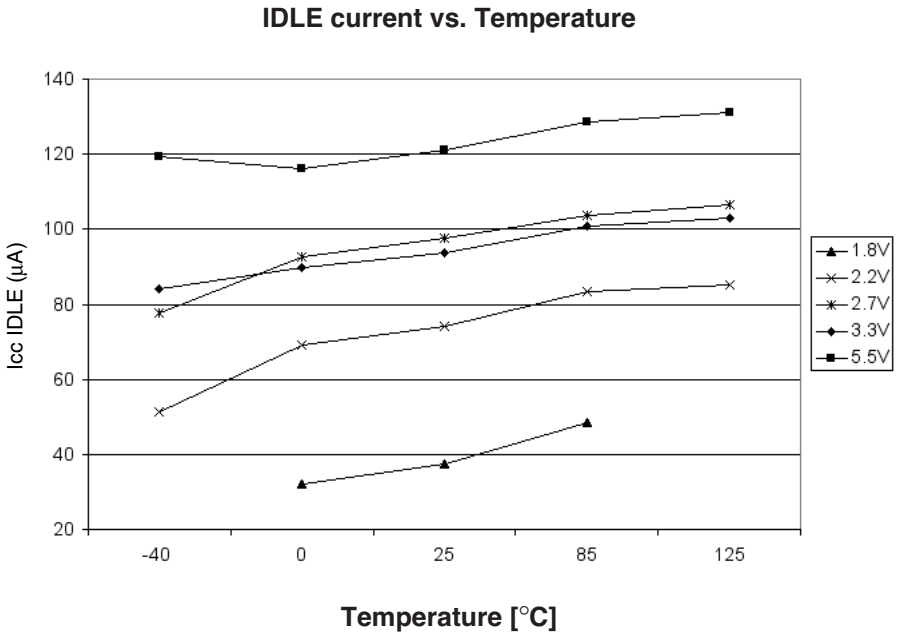


Figure 11: IDLE Mode Currents



4.1.1 Accumulator (A)

The Accumulator is a general-purpose 8-bit register that is used to hold data and results of arithmetic calculations or data manipulations.

4.1.2 X-Pointer (X)

The X-Pointer register allows for a 12-bit indexing value to be added to an 8-bit offset creating an effective address used for reading and writing between the entire memory space. (Software can only read from code EEPROM.) This provides software with the flexibility of storing lookup tables in the code EEPROM memory space for the core's accessibility during normal operation.

The ACEx core allows software to access the entire 12-bit X-Pointer register using the special X-pointer instructions (e.g. LD X, #000H). (See Table 9) However, software may also access the register through any of the memory-mapped instructions using the XHI (X[11:8]) and XLO (X[7:0]) variables located at 0xBE and 0xBF, respectively. (See Table 11)

The X register is divided into two sections. The 11 least significant bits (LSBs) of the register is the address of the program or data memory space. The most significant bit (MSB) of the register is write only and selects between the data (0x000 to 0x0FF) or program (0x800 to 0xFFF) memory space.

Example: If Bit 11 = 0, then the LD A, [00,X] instruction will take a value from address range 0x000 to 0x0FF and load it into A. If Bit 11 = 1, then the LD A, [00,X] instruction will take a value from address range 0x800 to 0xFFF and load it into A.

The X register can also serve as a counter or temporary storage register. However, this is true only for the 11-LSBs since the 12th bit is dedicated for memory space selection.

4.1.3 Program Counter (PC)

The 10-bit program counter register contains the address of the next instruction to be executed. After a reset, if in normal mode the program counter is initialized to 0x800.

4.1.4 Stack Pointer (SP)

The ACEx microcontroller has an automatic program stack with a 4-bit stack pointer. The stack can be initialized to any location between addresses 0x30-0x3F. Normally, the stack pointer is initialized by one of the first instructions in an application program. After a reset, the stack pointer is defaulted to 0xF pointing to address 0x3F.

The stack is configured as a data structure which decrements from high to low memory. Each time a new address is pushed onto the stack, the core decrements the stack pointer by two. Each time an address is pulled from the stack, the core increments the stack pointer is by two. At any given time, the stack pointer points to the next free location in the stack.

When a subroutine is called by a jump to subroutine (JSR) instruction, the address of the instruction is automatically pushed onto the stack least significant byte first. When the subroutine is finished, a return from subroutine (RET) instruction is executed. The RET instruction pulls the previously stacked return address from the stack and loads it into the program counter. Execution then continues at the recovered return address.

4.1.5 Status Register (SR)

The 8-bit Status register (SR) contains four condition code indicators (C, H, Z, and N), one interrupt masking bit (G), and an EEPROM write flag (R). The condition codes are automatically updated by most instructions. (See Table 10)

Carry/Borrow (C)

The carry flag is set if the arithmetic logic unit (ALU) performs a carry or borrow during an arithmetic operation and by its dedicated instructions. The rotate instruction operates with and through the carry bit to facilitate multiple-word shift operations. The LDC and INVC instructions facilitate direct bit manipulation using the carry flag.

Half Carry (H)

The half carry flag indicates whether an overflow has taken place on the boundary between the two nibbles in the accumulator. It is primarily used for Binary Coded Decimal (BCD) arithmetic calculation.

Zero (Z)

The zero flag is set if the result of an arithmetic, logic, or data manipulation operation is zero. Otherwise, it is cleared.

Negative (N)

The negative flag is set if the MSB of the result from an arithmetic, logic, or data manipulation operation is set to one. Otherwise, the flag is cleared. A result is said to be negative if its MSB is a one.

Interrupt Mask (G)

The interrupt request mask (G) is a global mask that disables all maskable interrupt sources. If the G Bit is cleared, interrupts can become pending, but the operation of the core continues uninterrupted. However, if the G Bit is set an interrupt is recognized. After any reset, the G bit is cleared by default and can only be set by a software instruction. When an interrupt is recognized, the G bit is cleared after the PC is stacked and the interrupt vector is fetched. Once the interrupt is serviced, a return from interrupt instruction is normally executed to restore the PC to the value that was present before the interrupt occurred. The G bit is reset to one after a return from interrupt is executed. Although the G bit can be set within an interrupt service routine, "nesting" interrupts in this way should only be done when there is a clear understanding of latency and of the arbitration mechanism.

4.2 Interrupt handling

When an interrupt is recognized, the current instruction completes its execution. The return address (the current value in the program counter) is pushed onto the stack and execution continues at the address specified by the unique interrupt vector (see Table 11). This process takes five instruction cycles. At the end of the interrupt service routine, a return from interrupt (RETI) instruction is executed. The RETI instruction causes the saved address to be pulled off the stack in reverse order. The G bit is set and instruction execution resumes at the return address.

Table 8: Interrupt Priority Sequence

Priority (4 highest, 1 lowest)	Interrupt
4	MIW (EDGEI)
3	Timer0 (TMRI0)
2	Timer1 (TMRI1)
1	Software (INTR)

Table 10: Instruction Cycles and Bytes

Mnemonic	Operand	Bytes	Cycles	Flags affected
ADC	A, [X]	1	1	C,H,Z,N
ADC	A, M	2	2	C,H,Z,N
ADC	A, #	2	2	C,H,Z,N
ADD	A, [X]	1	1	Z,N
ADD	A, M	2	2	Z,N
ADD	A, #	2	2	Z,N
AND	A, #	2	2	Z,N
AND	A, M	2	2	Z,N
AND	A, [X]	1	1	Z,N
CLR	X	1	1	Z
CLR	A	1	1	C,H,Z,N
CLR	M	2	2	C,H,Z,N
DEC	A	1	1	Z,N
DEC	M	2	2	Z,N
DEC	X	1	1	Z
IFBIT	#, A	1	1	None
IFBIT	#, M	2	2	None
IFC		1	1	None
IFEQ	A, [00,X]	2	3	None
IFEQ	A, [X]	1	1	None
IFEQ	A, #	2	2	None
IFEQ	A, M	2	2	None
IFEQ	M, #	3	3	None
IFEQ	X, #	3	3	None
IFGT	A, #	2	2	None
IFGT	A, [00,X]	2	3	None
IFGT	A, [X]	1	1	None
IFGT	A, M	2	2	None
IFGT	X, #	3	3	None
IFNE	A, #	2	2	None
IFNE	A, [00,X]	2	3	None
IFNE	A, [X]	1	1	None
IFNE	A, M	2	2	None
IFLT	X, #	3	3	None
IFNC		1	1	None
INC	A	1	1	Z,N
INC	M	2	2	Z,N
INC	X	1	1	Z
INTR		1	5	None
INVC		1	1	C

Mnemonic	Operand	Bytes	Cycles	Flags affected
JMP	M	3	4	None
JMP	[00,X]	2	3	None
JP		1	1	None
JSR	M	3	5	None
JSR	[00,X]	2	5	None
LD	A, #	2	2	None
LD	A, [00,X]	2	3	None
LD	A, [X]	1	1	None
LD	A, M	2	2	None
LD	M, #	3	3	None
LD	X, #	3	3	None
LDC	#, M	2	2	C
LD	M, M	3	3	None
NOP		1	1	None
OR	A, #	2	2	Z,N
OR	A, [X]	1	1	Z,N
OR	A, M	2	2	Z,N
RBIT	#, [X]	1	2	Z,N
RBIT	#, M	2	2	Z,N
RC		1	1	C,H
RET		1	5	None
RETI		1	5	None
RLC	A	1	1	C,Z,N
RLC	M	2	2	C,Z,N
RRC	A	1	1	C,Z,N
RRC	M	2	2	C,Z,N
SBIT	#, [X]	1	2	Z,N
SBIT	#, M	2	2	Z,N
SC		1	1	C,H
ST	A, [00,X]	2	3	None
ST	A, [X]	1	1	None
ST	A, M	2	2	None
STC	#, M	2	2	Z,N
SUBC	A, #	2	2	C,H,Z,N
SUBC	A, [X]	1	1	C,H,Z,N
SUBC	A, M	2	2	C,H,Z,N
XOR	A, #	2	2	Z,N
XOR	A, [X]	1	1	Z,N
XOR	A, M	2	2	Z,N

4.4 Memory Map

All I/O ports, peripheral registers and core registers, except the accumulator and the program counter are mapped into memory space.

Table 11: Memory Map

Address	Memory Space	Block	Contents
0x00 - 0x3F	Data	SRAM	Data RAM
0x40 - 0x7F	Data	EEPROM	Data EEPROM
0xA0	Data	HBC	HBCNTRL register (ACE1202-2 only)
0xA1	Data	HBC	PSCALE register (ACE1202-2 only)
0xA2	Data	HBC	HPATTERN register (ACE1202-2 only)
0xA3	Data	HBC	LPATTERN register (ACE1202-2 only)
0xA4	Data	HBC	BPSEL register (ACE1202-2 only)
0xA9	Data	HBC	DAT0 register (ACE1202-2 only)
0xAA	Data	Timer1	T1RALO register
0xAB	Data	Timer1	T1RAHI register
0xAC	Data	Timer1	TMR1LO register
0xAD	Data	Timer1	TMR1HI register
0xAE	Data	Timer1	T1CNTRL register
0xAF	Data	MIW	WKEDG register
0xB0	Data	MIW	WKPND register
0xB1	Data	MIW	WKEN register
0xB2	Data	I/O	PORTGD register
0xB3	Data	I/O	PORTGC register
0xB4	Data	I/O	PORTGP register
0xB5	Data	Timer0	WDSVR register
0xB6	Data	Timer0	T0CNTRL register
0xB7	Data	Clock	HALT mode register
0xB8 - 0xBC			Reserved
0xBD	Data	LBD	LBD register
0xBE	Data	Core	XHI register
0xBF	Data	Core	XLO register
0xC0	Data	Core	Power mode clear (PMC) register
0xCE	Data	Core	SP register
0xCF	Data	Core	Status register (SR)
0x800 - 0xFF5	Program	EEPROM	Code EEPROM
0xFF6 - 0xFF7	Program	Core	Timer0 Interrupt vector
0xFF8 - 0xFF9	Program	Core	Timer1 Interrupt vector
0xFFA - 0xFFB	Program	Core	MIW Interrupt vector
0xFFC - 0xFFD	Program	Core	Software Interrupt vector
0xFFE - 0xFFF			Reserved

5.4 Mode 3: Input Capture Mode

In the Input Capture mode, the timer is used to measure elapsed time between edges of an input signal. Once the timer is configured for this mode, the timer starts counting down immediately at the instruction clock rate. The Timer 1 will then transfer the current value of the TMR1 register into the T1RA register as soon as the selected edge of T1 is sensed. The input signal on T1 must have a pulse width equal to or greater than one instruction clock cycle. At every T1RA capture, software can then store the values into RAM to calculate the elapsed time between edges on T1. At any given time (with proper consideration of the state of T1) the timer can be configured to capture on positive-going or negative-going edges. A block diagram of the timer's Input Capture mode of operation is shown in Figure 17.

The timer has one interrupt (TMRI1) that is maskable through the T1EN bit of the T1CNTRL register. However, the core is only interrupted if the T1EN bit and the G (Global Interrupt enable) bit of the SR is set. The Input Capture mode contains two interrupt pending flags 1) the TMR1 register capture in T1RA (T1PND) and 2) timer underflow (T1C0). If interrupts are enabled, the timer will generate an interrupt each time a pending flag is set (provided that the pending flag was previously cleared.) The interrupt service routine is responsible for proper handling of the T1PND flag, T1C0 flag, and the T1EN bit.

For this operating mode, the T1C0 control bit serves as the timer underflow interrupt pending flag. The Timer 1 interrupt service routine must read both the T1PND and T1C0 flags to determine the cause of the interrupt. A set T1C0 flag means that a timer underflow occurred whereas a set T1PND flag means that a capture occurred in T1RA. It is possible that both flags will be found set, meaning that both events occurred at the same time. The interrupt service routine should take this possibility into consideration.

Because the T1C0 bit is used as the underflow interrupt pending flag, it is not available for use as a start/stop bit as in the other modes.

The TMR1 register counts down continuously at the instruction clock rate starting from the time that the input capture mode is selected. (See Table 12 and 13) To stop the timer from running, you must change the mode to an alternate mode (PWM or External Event Counter) while resetting the T1C0 bit.

The input pins can be independently configured to sense positive-going or negative-going transitions. The edge sensitivity of pin T1 is controlled by bit T1C1 as indicated in Table 13.

The edge sensitivity of a pin can be changed without leaving the input capture mode even while the timer is running. This feature allows you to measure the width of a pulse received on an input pin.

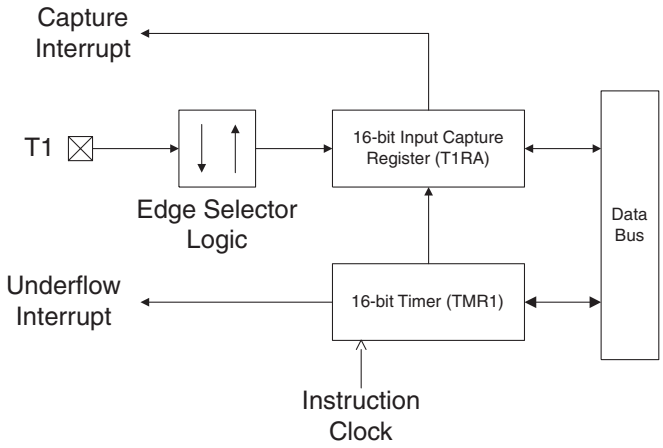
For example, the T1 pin can be programmed to be sensitive to a positive-going edge. When the positive edge is sensed, the TMR1 register contents is transferred to the T1RA register and a Timer 1 interrupt is generated. The Timer 1 interrupt service routine records the contents of the T1RA register, changes the edge sensitivity from positive to negative-going edge, and clears the T1PND flag. When the negative-going edge is sensed another Timer 1 interrupt is generated. The interrupt service routine reads the T1RA register again. The difference between the previous reading and the current reading reflects the elapsed time between the positive edge and negative edge of the T1 input signal i.e. the width of the positive-going pulse.

Remember that the Timer1 interrupt service routine must test the T1C0 and T1PND flags to determine the cause of the interrupt. If the T1C0 flag caused the interrupt, the interrupt service routine should record the occurrence of an underflow by incrementing a counter in memory or by some other means. The software that calculates the elapsed time between captures should take into account the number of underflow that occurred when making its calculation.

The following steps show how to properly configure Timer 1 to operate in the Input Capture mode.

1. Configure T1 as an input by clearing bit 2 of PORTGC.
   - RBIT 2, PORTGC ; Configure G2 as an input
2. Initialize T1 to input with pull-up by setting bit 2 of PORTGD.
   - SBIT 2, PORTGD ; Set G2 high
3. Enable the global interrupt enable bit.
   - SBIT 4, STATUS
4. With the timer stopped, load the initial time into the TMR1 register (typically the value is 0xFFFF.)
   - LD TMR1LO, #0FFH
   - LD TMR1HI, #00H
5. Write the appropriate control value to the T1CNTRL register to select Input Capture mode, to sense the appropriate edge, to set the enable bit, and to clear the pending flags. (See Table 12 and 13)
   - LD T1CNTRL, #64H ; T1C1 is the edge select bit
6. As soon as the input capture mode is enabled, the timer starts counting. When the selected edge is sensed on T1, the T1RA register is loaded and a Timer 1 interrupt is triggered.

Figure 17: Input Capture Mode



8.0 Hardware Bit-Coder (ACE1202-2 only)

The ACE1202-2 contains a dedicated hardware bit-encoding peripheral block, Hardware Bit-Coder (HBC), for IR/RF data transmission (see Figure 21.) The HBC is completely software programmable and can be configured to emulate various bit-encoding formats. The software developer has the freedom to encode each bit of data into a desired pattern and output the encoded data at the desired frequency through either the G2 or G5 output (TX) ports.

The HBC contains six 8-bit memory-mapped configuration registers PSCALE, HPATTERN, LPATTERN, BPSEL, HBCNTRL, and DAT0. The registers are used to select the transmission frequency, store the data bit-encoding patterns, configure the data bit-pattern/frame lengths, and control the data transmission flow.

To select the IR/RF transmission frequency, an 8-bit divide constant must be written into the IR/RF Pre-scalar (PSCALE) register. The IR/RF transmission frequency generator divides the 1MHz instruction clock down by 4 and the PSCALE register is used to select the desired IR/RF frequency shift. Together, the transmission frequency range can be configured between 976Hz (PSCALE = 0xFF) and 125kHz (PSCALE = 0x01). Upon a reset, the PSCALE register is initialized to zero disabling the IR/RF transmission frequency generator. However, once the PSCALE register is programmed, the desired IR/RF frequency is maintained as long as the device is powered.

Once the transmission frequency is selected, the data bit-encoding patterns must be stored in the appropriate registers. The HBC contains two 8-bit bit-encoding pattern registers, High-pattern (HPATTERN) and Low-pattern (LPATTERN). The encoding pattern stored in the HPATTERN register is transmitted when the data bit value to be encoded is a 1. Similarly, the pattern stored in the LPATTERN register is transmitted when the data bit value to be encoded is a 0. The HBC transmits each encoded pattern MSB first.

The number of bits transmitted from the HPATTERN and LPATTERN registers is software programmable through the Bit Period Configuration (BPSEL) register (see Figure 22). During the transmission of HPATTERN, the number of bits transmitted is configured by BPH[2:0] (BPSEL[2:0]) while BPL[2:0] (BPSEL[5:3]) configures the number of transmitted bits for the LPATTERN. The HBC allows from 2 (0x1) to 8 (0x7) encoding pattern bits to be transmitted from each register. Upon a reset, BPSEL is initially 0 disabling the HBC from transmitting pattern bits from either register.

The Data (DAT0) register is used to store up to 8 bits of data to be encoded and transmitted by the HBC. This data is shifted, bit by bit, MSB to LSB into a 1-bit decision register. If the active bit shifted into the decision register is 1, the pattern in the HPATTERN register is shifted out of the output port. Similarly, if the active bit is 0 the pattern in the LPATTERN register is shifted out.

The HBC control (HBCNTRL) register is used to configure and control the data transmission. HBCNTRL is divided in 5 different controlling signal FRAME[2:0], IOSEL, TXBUSY, START/$\overline{\text{STOP}}$, and OCFLAG (see Figure 23.)

FRAME[2:0] selects the number of bits of DAT0 to encode and transmit. The HBC allows from 2 (0x1) to 8 (0x7) DAT0 bits to be encoded and transmitted. Upon a reset, FRAME is initialized to zero disabling the DAT0's decision register transmitting no data.

The IOSEL signal selects the transmission to output (TX) through either port G2 or G5. If IOSEL is 1, G5 is selected as the output port otherwise G2 is selected.

The TXBUSY signal is read only and is used to inform software that a transmission is in progress. TXBUSY goes high when the encoded data begins to shift out of the output port and will remains high during each consecutive DAT0 frame bit transmission (see Figure 25). The HBC will clear the TXBUSY signal when the last DAT0 encoded bit of the frame is transmitted and the STOP signal is 0.

The START / $\overline{\text{STOP}}$ signal controls the encoding and transmission process for each data frame. When software sets the START / $\overline{\text{STOP}}$ bit the DAT0 frame transmission process begins. The START signal will remain high until the beginning of the last encoded DAT0 frame bit transmission. The HBC then clears the START / $\overline{\text{STOP}}$ bit allowing software to either continue with a new DAT0 frame transmission or stop the transmission all together (see Figure 25). If TXBUSY is 0 when the START signal is enabled, a synchronization period occurs before any data is transmitted lasting the amount of time to transmit a 0 encoded bit (see Figure 24).

The OCFLAG signal is read only and goes high when the last encoded bit of the DAT0 frame is transmitting. The OCFLAG signal is used to inform software that the DAT0 frame transmission operation is completing (see Figure 25). If multiple DAT0 frames are to be transmitted consecutively, software should poll the OCFLAG signal for a 1. Once OCFLAG is 1, DAT0 must be reload and the START / $\overline{\text{STOP}}$ bit must be restored to 1 in order to begin the new frame transmission without interruptions (the synchronization period). Since OCFLAG remains high during the entire last encoded DAT0 frame bit transmission, software should wait for the HBC to clear the OCFLAG signal before polling for the new OCFLAG high pulse. If new data is not reloaded into DAT0 and the START signal ($\overline{\text{STOP}}$ is active) is not set before the OCFLAG is 0, the transmission process will end (TXBUSY is cleared) and a new process will begin starting with the synchronization period.

Figure 24 and 25 shows how the HBC performs its data encoding. In the example, two frames are encoded and transmitted consecutively with the following bit encoding format specification:

1. Transmission frequency = 62.5KHz
2. Data to be encoded = 0x52, 0x92 (all 8-bits)
3. Each bit should be encoded as a 3-bit binary value, '1' = 110b and '0' = 100b
4. Transmission output port : G2

To perform the data transmission, software must first initialize the PSCALE, BPSEL, HPATTERN, LPATTERN, and DAT0 registers with the appropriate values.

```
LD  PSCALE, #03H        ; (1MHz ÷ 4) ÷ 4 = 62.5KHz
LD  BPSEL, #012H        ; BPH = 2, BPL = 2 (3 bits each)
LD  HPATTERN, #0C0H     ; HPATTERN = 0xC0
LD  LPATTERN, #090H     ; LPATTERN = 0x90
LD  DAT0, #052H         ; DAT0 = 0x52
```

Once the basic registers are initialized, the HBC can be started. (At the same time, software must set the number of data bits per data frame and select the desired output port.)

```
LD  HBCNTRL, #27H       ; START / STOP = 1,
                          FRAME = 7, IOSEL = 0
```

10.0 I/O Port

The eight I/O pins (six on 8-pin package option) are bi-directional (see Figure 28) with the exception of G3 which is always an input with weak pull-up. The bi-directional I/O pins can be individually configured by software to operate as high-impedance inputs, as inputs with weak pull-up, or as push-pull outputs. The operating state is determined by the contents of the corresponding bits in the data and configuration registers. Each bi-directional I/O pin can be used for general purpose I/O, or in some cases, for a specific alternate function determined by the on-chip hardware.

10.1 I/O registers

The I/O pins (G0-G7) have three memory-mapped port registers associated with the I/O circuitry: a port configuration register (PORTGC), a port data register (PORTGD), and a port input register (PORTGP). PORTGC is used to configure the pins as inputs or outputs. A pin may be configured as an input by writing a 0 or as an output by writing a 1 to its corresponding PORTGC bit. If a pin is configured as an output, its PORTGD bit represents the state of the pin (1 = logic high, 0 = logic low). If the pin is configured as an input, its PORTGD bit selects whether the pin is a weak pull-up or a high-impedence input. Table 14 provides details of the port configuration options. The port configuration and data registers can both be read from or written to. Reading PORTGP returns the value of the port pins regardless of how the pins are configured. Since this device supports MIW, PORTG inputs have Schmitt triggers.

Figure 28: PORTG Logic Diagram

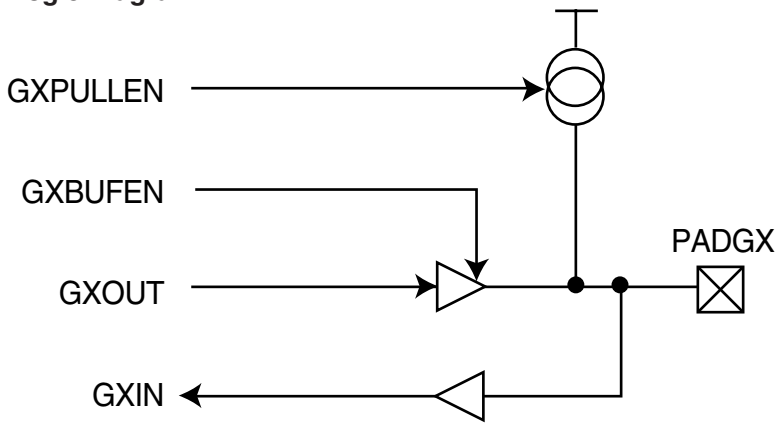


Figure 29: I/O Register bit assignments (PORTGC,PORTGD, PORTGD)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
[13]G7	[13]G6	G5	G4	[14]G3	G2	G1	G0

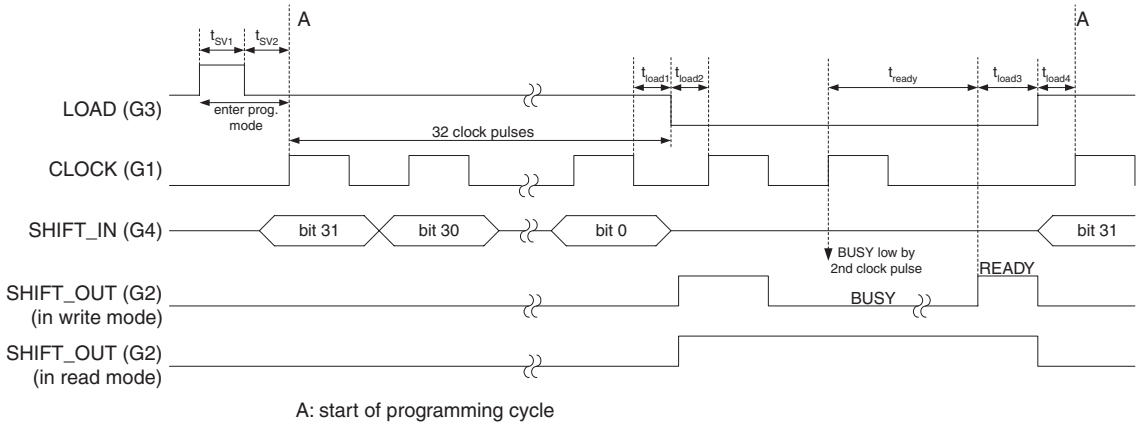
[13] Available only on the 14-pin package option

[14] G3 is always an input with weak pull-up

Table 14: I/O configuration options

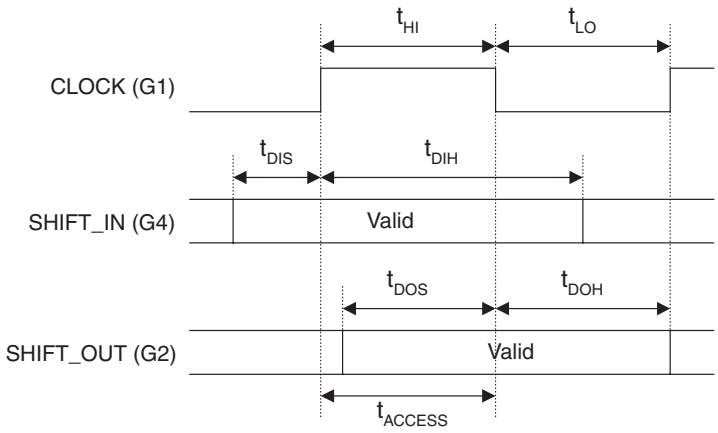
Configuration Bit	Data Bit	Port Pin Configuration
0	0	High-impedence input (TRI-STATE input)
0	1	Input with pull-up (weak one input)
1	0	Push-pull zero output
1	1	Push-pull one output

Figure 30: Programming Protocol[16]



A: start of programming cycle

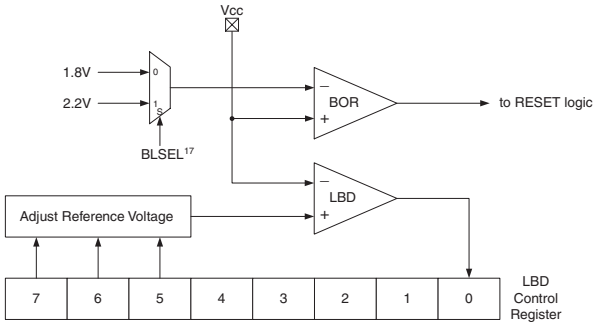
Figure 31: Serial Data Timing



12.0 Brown-out/Low Battery Detect Circuit

The Brown-out Reset (BOR) and Low Battery Detect (LBD) circuits on the ACEx microcontroller have been designed to offer two types of voltage reference comparators. The sections below will describe the functionality of both circuits.

Figure 32: BOR/LBD Block Diagram



[17] See Figure 14 for information on BLSEL.

12.1 Brown Out Reset [18]

The Brown-out Reset (BOR) function is used to hold the device in reset when V_{CC} drops below a fixed threshold. (See BOR Electrical Characteristics for threshold voltage.) While in reset, the device is held in its initial condition until V_{CC} rises above the threshold value. Shortly after V_{CC} rises above the threshold value, an internal reset sequence is started. After the reset sequence, the core fetches the first instruction and starts normal operation.

On the devices, the BOR should be used in situations when V_{CC} rises and falls slowly and in situations when V_{CC} does not fall to zero before rising back to operating range. The Brown-out Reset can be thought of as a supplement function to the Power-on Reset when V_{CC} does not fall below ~1.5V. The Power-on Reset circuit works best when V_{CC} starts from zero and rises sharply. So in applications where V_{CC} is not constant, the BOR will give added device stability.

The BOR circuit must be enabled through the BOR enable bit (BOREN) in the initialization register. The BOREN bit can only be set while the device is in programming mode. Once set, the BOR will always be powered-up enabled. Software cannot disable the BOR. The BOR can only be disabled in programming mode by resetting the BOREN bit as long as the global write protect (WDIS) feature is not enabled.

[18] BOR is not available on the P.N. ACE1202B/ACE12022B device

12.2 Low Battery Detect

The Low Battery Detect (LBD) circuit allows software to monitor the V_{CC} level at the lower voltage ranges. LBD has an eight level software programmable voltage reference threshold that can be changed on the fly. Once V_{CC} falls below the selected threshold, the LBD flag in the LBD control register is set. The LBD flag will hold its value until V_{CC} rises above the threshold. (See Table 16)

The LBD bit is read only. If LBD is 0, it indicates that the V_{CC} level is higher than the selected threshold. If LBD is 1, it indicates that the V_{CC} level is below the selected threshold. The threshold level can be adjusted up to eight levels using the three trim bits (Bat_trim[2:0]) of the LBD control register. The LBD flag does not cause any hardware actions or an interruption of the processor. It is for software monitoring only.

The LBD function is disabled during HALT/IDLE mode. After exiting HALT/IDLE, software must wait at least 10 µs before reading the LBD bit to ensure that the internal circuit has stabilized.

Table 16: LBD Control Register Definition

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bat_trim[2:0]			0	X	X	X	LBD

Level	Bat_trim[2]	Bat_trim[1]	Bat_trim[0]	Voltage Reference Range (±20%)
1	0	0	0	2.9 - 3.0
2	0	0	1	2.8 - 2.9
3	0	1	0	2.7 - 2.8
4	0	1	1	2.6 - 2.7
5	1	0	0	2.5 - 2.6
6	1	0	1	2.4 - 2.5
7	1	1	0	2.3 - 2.4
8	1	1	1	2.2 - 2.3

13.0 RESET block

When a RESET sequence is initiated, all I/O registers will be reset setting all I/Os to high-impedence inputs. The system clock is restarted after the required clock start-up delay. A reset is generated by any one of the following three conditions:

- Power-on Reset (as described in Section 14.0)
- Brown-out Reset (as described in Section 12.1)
- Watchdog Reset (as described in Section 7.0)
- External Reset[18] (as described in Section 14.0)

[18] Available only on the 14-pin package option.

14.0 Power-On-Reset

The Power-On Reset (POR) circuit is guaranteed to work if the rate of rise of V_{CC} is no slower than 10ms/1volt. The POR circuit was designed to respond to fast low to high transitions between 0V and V_{CC}. The circuit will not work if V_{CC} does not drop to 0V before the next power-up sequence. In applications where 1) the V_{CC} rise is slower than 10ms/1 volt or 2) V_{CC} does not drop to 0v before the next power-up sequence the external reset option should be used.

The external reset provides a way to properly reset the ACEx microcontroller if POR cannot be used in the application. The external reset pin contains an internal pull-up resistor. Therefore, to reset the device the reset pin should be held low for at least 2ms so that the internal clock has enough time to stabilize.

15.0 CLOCK

The ACEx microcontroller has an on-board oscillator trimmed to a frequency of 2MHz who is divided down by two yielding a 1MHz frequency. (See AC Electrical Characteristics.) Upon power-up, the on-chip oscillator runs continuously unless entering HALT mode or using an external clock source.

If required, an external oscillator circuit may be used depending on the states of the CMODE bits of the initialization register. (See Table 17) When the device is driven using an external clock, the clock input to the device (G1/CKI) can range between DC to 4MHz. For external crystal configuration, the output clock (CKO) is on the G0 pin. (See Figure 34) If an external crystal or RC is used, internally the input frequency (CKI) is divided-down by four to yield the corresponding instruction clock. If the device is configured for an external square clock, it will not be divided.

Table 17: CMODEx Bit Definition

CMODE[1]	CMODE[0]	Clock Type
0	0	Internal 1 MHz clock
0	1	External square clock
1	0	External crystal/resonator
1	1	External RC clock

Figure 33: BOR and POR Circuit Relationship Diagram

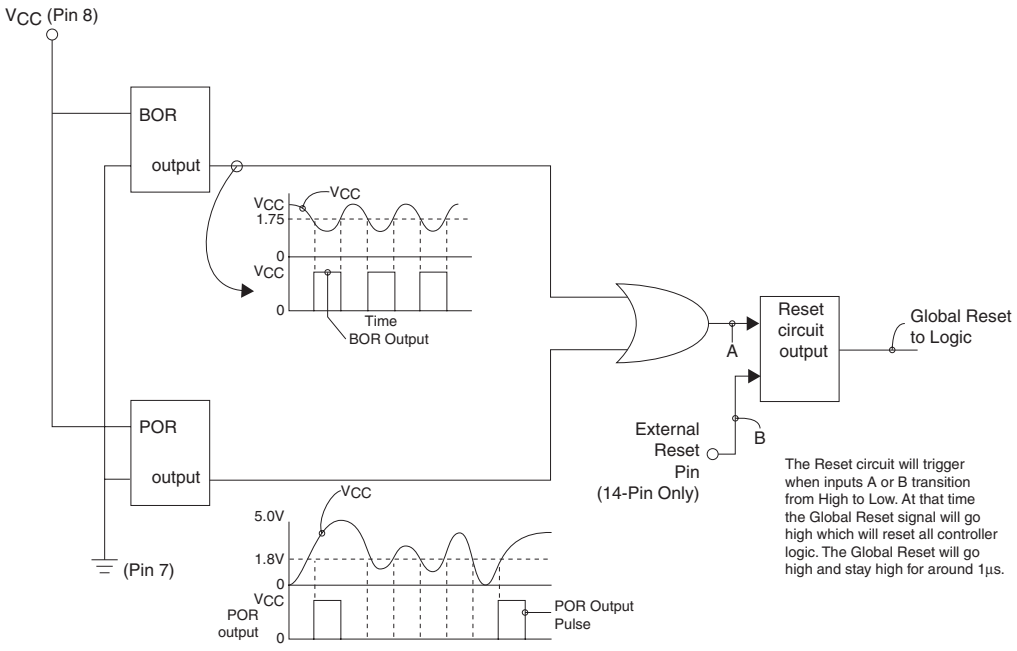
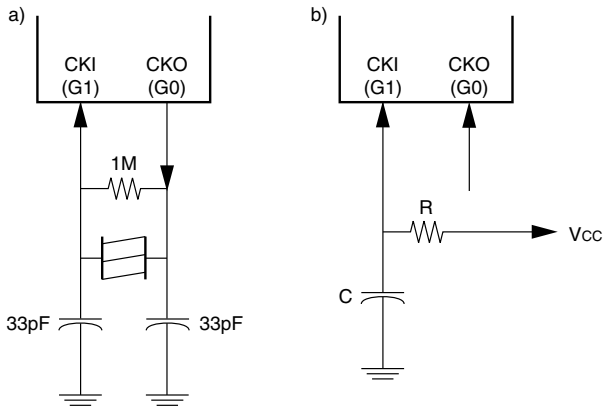


Figure 34: Crystal (a) and RC (b) Oscillator Diagrams



15.0 HALT Mode

The HALT mode is a power saving feature that almost completely shuts down the device for current conservation. The device is placed into HALT mode by setting the HALT enable bit (EHALT) of the HALT register through software using only the “LD M, #” instruction. EHALT is a write only bit and is automatically cleared upon exiting HALT. When entering HALT, the internal oscillator and all the on-chip systems including the LBD and the BOR circuits are shut down.

The device can exit HALT mode only by the MIW circuit. Therefore, prior to entering HALT mode, software must configure the MIW circuit accordingly. (See Section 9) After a wakeup from HALT, a 1ms start-up delay is initiated to allow the internal oscillator to stabilize before normal execution resumes. Immediately after exiting HALT, software must clear the Power Mode Clear (PMC) register by only using the “LD M, #” instruction. (See Figure 36)

17.0 IDLE Mode

In addition to the HALT mode power saving feature, the device also supports an IDLE mode operation. The device is placed into IDLE mode by setting the IDLE enable bit (EIDLE) of the HALT register through software using only the “LD M, #” instruction. EIDLE is a write only bit and is automatically cleared upon exiting IDLE. The IDLE mode operation is similar to HALT except the internal oscillator, the Watchdog, and the Timer 0 remain active while the other on-chip systems including the LBD and the BOR circuits are shut down.

The device automatically wakes from IDLE mode by the Timer 0 overflow every 8192 cycles (see Section 6). Before entering IDLE mode, software must clear the WKEN register to disable the MIW block. Once a wake from IDLE mode is triggered, the core will begin normal operation by the next clock cycle. Immediately after exiting IDLE mode, software must clear the Power Mode Clear (PMC) register by using only the "LD M, #" instruction. (See Figure 37)

Figure 35: HALT Register Definition

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
undefined	undefined	undefined	undefined	undefined	undefined	EIDLE	EHALT

Figure 36: Recommended HALT Flow

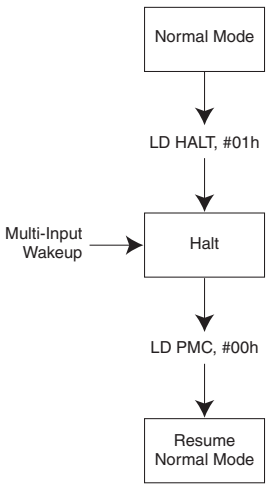
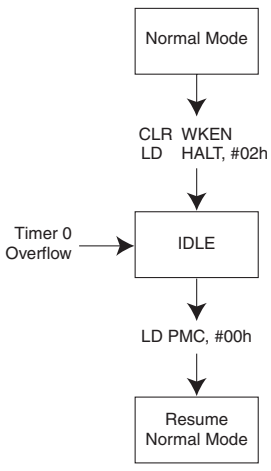


Figure 37: Recommended IDLE Flow



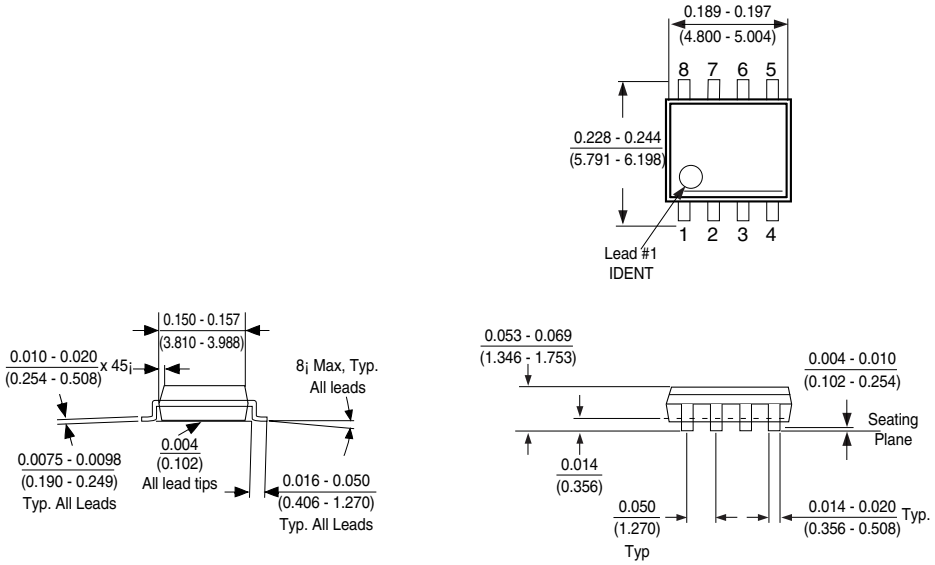
Ordering Information (ACE1202)

Part Number	Core Type			Max. # I/Os	Program Memory Size		Operating Voltage Range			Temperature Range			Package				Tape & Reel
	0	1	2	8	1K	2K	1.8 – 5.5V	2.2 – 5.5V	2.7 – 5.5V	0 to 70°C	-40 to +85C	-40 to +125°C	8-pin SOIC	14-pin SOIC	8-pin DIP	14-pin DIP	
ACE1202M8			X	X		X		X		X			X				
ACE1202M8X			X	X		X		X		X			X				X
ACE1202M			X	X		X		X		X				X			
ACE1202MX			X	X		X		X		X				X			X
ACE1202N			X	X		X		X		X					X		
ACE1202N14			X	X		X		X		X						X	
ACE1202EM8			X	X		X		X			X		X				
ACE1202EM8X			X	X		X		X			X		X				X
ACE1202EM			X	X		X		X			X			X			
ACE1202EMX			X	X		X		X			X			X			X
ACE1202EN			X	X		X		X			X				X		
ACE1202EN14			X	X		X		X			X					X	
ACE1202VM8			X	X		X		X				X	X				
ACE1202VM8X			X	X		X		X				X	X				X
ACE1202VM			X	X		X		X				X		X			
ACE1202VMX			X	X		X		X				X		X			X
ACE1202VN			X	X		X		X				X			X		
ACE1202VN14			X	X		X		X				X				X	
ACE1202BM8			X	X		X			X	X			X				
ACE1202BM8X			X	X		X			X	X			X				X
ACE1202BM			X	X		X			X	X				X			
ACE1202BMX			X	X		X			X	X				X			X
ACE1202BN			X	X		X			X	X					X		
ACE1202BN14			X	X		X			X	X						X	
ACE1202BEM8			X	X		X			X		X		X				
ACE1202BEM8X			X	X		X			X		X		X				X
ACE1202BEM			X	X		X			X		X			X			
ACE1202BEMX			X	X		X			X		X			X			X
ACE1202BEN			X	X		X			X		X				X		
ACE1202BEN14			X	X		X			X		X					X	
ACE1202BVM8			X	X		X			X			X	X				
ACE1202BVM8X			X	X		X			X			X	X				X
ACE1202BVM			X	X		X			X			X		X			
ACE1202BVMX			X	X		X			X			X		X			X
ACE1202BVN			X	X		X			X			X			X		
ACE1202BVN14			X	X		X			X			X				X	
ACE1202LM8			X	X		X	X			X			X				
ACE1202LM8X			X	X		X	X			X			X				X
ACE1202LM			X	X		X	X			X				X			
ACE1202LMX			X	X		X	X			X				X			X
ACE1202LN			X	X		X	X			X					X		
ACE1202LN14			X	X		X	X			X						X	

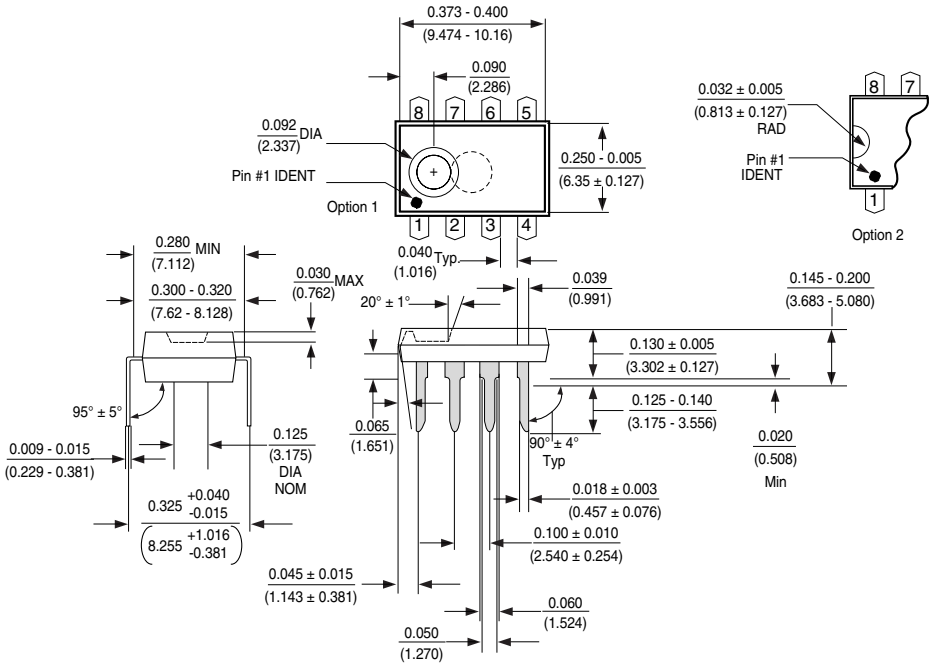
Ordering Information (ACE1202-2)

Part Number	Core Type			Max. # I/Os	Program Memory Size		Operating Voltage Range			Temperature Range			Package				Tape & Reel
	0	1	2	8	1K	2K	1.8 – 5.5V	2.2 – 5.5V	2.7 – 5.5V	0 to 70°C	-40 to +85C	-40 to +125°C	8-pin SOIC	14-pin SOIC	8-pin DIP	14-pin DIP	
ACE12022M8			X	X		X		X		X			X				
ACE12022M8X			X	X		X		X		X			X				X
ACE12022M			X	X		X		X		X				X			
ACE12022MX			X	X		X		X		X				X			X
ACE12022N			X	X		X		X		X					X		
ACE12022N14			X	X		X		X		X						X	
ACE12022EM8			X	X		X		X			X		X				
ACE12022EM8X			X	X		X		X			X		X				X
ACE12022EM			X	X		X		X			X			X			
ACE12022EMX			X	X		X		X			X			X			X
ACE12022EN			X	X		X		X			X				X		
ACE12022EN14			X	X		X		X			X					X	
ACE12022VM8			X	X		X		X				X	X				
ACE12022VM8X			X	X		X		X				X	X				X
ACE12022VM			X	X		X		X				X		X			
ACE12022VMX			X	X		X		X				X		X			X
ACE12022VN			X	X		X		X				X			X		
ACE12022VN14			X	X		X		X				X				X	
ACE12022BM8			X	X		X			X	X			X				
ACE12022BM8X			X	X		X			X	X			X				X
ACE12022BM			X	X		X			X	X				X			
ACE12022BMX			X	X		X			X	X				X			X
ACE12022BN			X	X		X			X	X					X		
ACE12022BN14			X	X		X			X	X						X	
ACE12022BEM8			X	X		X			X		X		X				
ACE12022BEM8X			X	X		X			X		X		X				X
ACE12022BEM			X	X		X			X		X			X			
ACE12022BEMX			X	X		X			X		X			X			X
ACE12022BEN			X	X		X			X		X				X		
ACE12022BEN14			X	X		X			X		X					X	
ACE12022BVM8			X	X		X			X			X	X				
ACE12022BVM8X			X	X		X			X			X	X				X
ACE12022BVM			X	X		X			X			X		X			
ACE12022BVMX			X	X		X			X			X		X			X
ACE12022BVN			X	X		X			X			X			X		
ACE12022BVN14			X	X		X			X			X				X	

Physical Dimensions inches (millimeters) unless otherwise noted

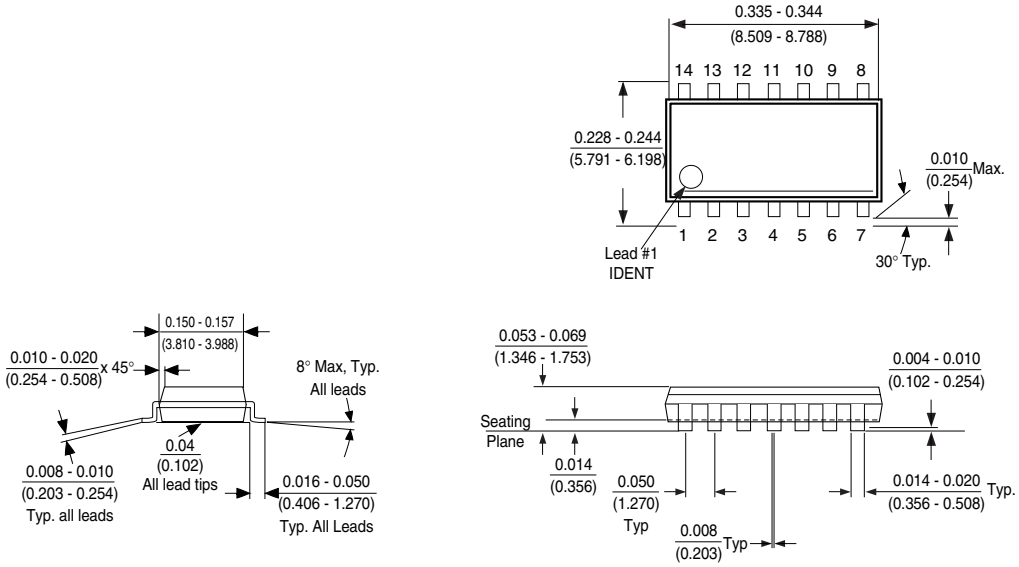


Molded Small Out-Line Package (M8)
Order Number ACE1202(12022, 1202L)M8/ACE1202(12022)EM8/ACE1202VM8
ACE1202(12022)BM8/ACE1202(12022)BEM8/ACE1202(12022)BVM8
Package Number M08A

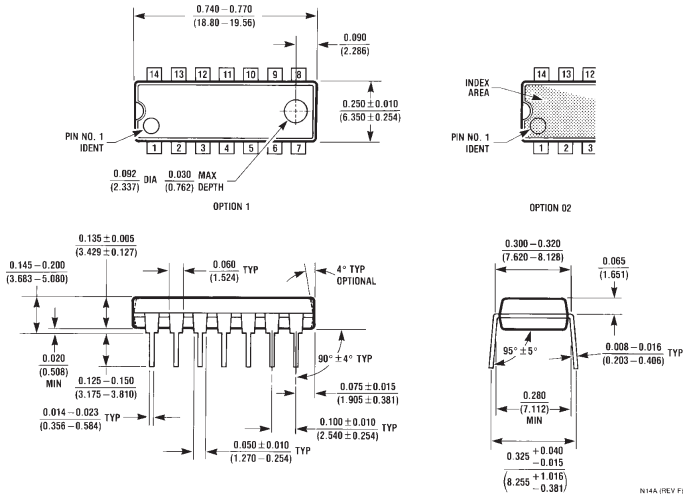


8-Pin DIP (N)
Order Number ACE1202(12022, 1202L)N/ACE1202(12022)EN/ACE1202VN
ACE1202(12022)BN/ACE1202(12022)BEN/ACE1202(12022)BVN
Package Number N08A

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Out-Line Package (M)
Order Number ACE1202(12022, 1202L)M/ACE1202(12022)EM/ACE1202VM
ACE1202(12022)BM/ACE1202(12022)BEM/ACE1202(12022)BVM
Package Number M14A



14-Pin DIP (N14)
Order Number ACE1202(12022, 1202L)N14/ACE1202(12022)EN14/ACE1202VN14
ACE1202(12022)BN14/ACE1202(12022)BEN14/ACE1202(12022)BVN14
Package Number N14A