Microchip Technology - ATMEGA8HVA-4CKU Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	4MHz
Connectivity	SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	7
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 9V
Data Converters	A/D 5x12b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-WFLGA
Supplier Device Package	36-LGA (6.5x3.5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atmega8hva-4cku

When an interrupt occurs, the Global Interrupt Enable I-bit is cleared and all interrupts are disabled. The user software can write logic one to the I-bit to enable nested interrupts. All enabled interrupts can then interrupt the current interrupt routine. The I-bit is automatically set when a Return from Interrupt instruction – RETI – is executed.

There are basically two types of interrupts. The first type is triggered by an event that sets the interrupt flag. For these interrupts, the Program Counter is vectored to the actual Interrupt Vector in order to execute the interrupt handling routine, and hardware clears the corresponding interrupt flag. Interrupt flags can also be cleared by writing a logic one to the flag bit position(s) to be cleared. If an interrupt condition occurs while the corresponding interrupt enable bit is cleared, the interrupt flag will be set and remembered until the interrupt is enabled, or the flag is cleared by software. Similarly, if one or more interrupt conditions occur while the Global Interrupt Enable bit is cleared, the corresponding interrupt flag(s) will be set and remembered until the Global Interrupt Enable bit is set, and will then be executed by order of priority.

The second type of interrupts will trigger as long as the interrupt condition is present. These interrupts do not necessarily have interrupt flags. If the interrupt condition disappears before the interrupt is enabled, the interrupt will not be triggered.

When the AVR exits from an interrupt, it will always return to the main program and execute one more instruction before any pending interrupt is served.

Note that the Status Register is not automatically stored when entering an interrupt routine, nor restored when returning from an interrupt routine. This must be handled by software.

When using the CLI instruction to disable interrupts, the interrupts will be immediately disabled. No interrupt will be executed after the CLI instruction, even if it occurs simultaneously with the CLI instruction. The following example shows how this can be used to avoid interrupts during the timed EEPROM write sequence.

Assembly Code Example

```
in  r16, SREG     ; store SREG value
cli    ; disable interrupts during timed sequence
sbi EECR, EEMPE   ; start EEPROM write
sbi EECR, EEPE
out SREG, r16     ; restore SREG value (I-bit)
```

C Code Example

```
char cSREG;
cSREG = SREG; /* store SREG value */
/* disable interrupts during timed sequence */
_CLI();
EECR |= (1<<EEMPE); /* start EEPROM write */
EECR |= (1<<EEPE);
SREG = cSREG; /* restore SREG value (I-bit) */
```

- **Bits 7:6 – Res: Reserved Bits**

These bits are reserved bits in the ATmega8HVA/16HVA and will always read as zero.

- **Bits 5, 4 – EEPM1 and EEPM0: EEPROM Programming Mode Bits**

The EEPROM Programming mode bit setting defines which programming action that will be triggered when writing EEPE. It is possible to program data in one atomic operation (erase the old value and program the new value) or to split the Erase and Write operations in two different operations. The Programming times for the different modes are shown in Table 8-1. While EEPE is set, any write to EEPMn will be ignored. During reset, the EEPMn bits will be reset to 0b00 unless the EEPROM is busy programming.

Table 8-1. EEPROM Mode Bits

EEPM1	EEPM0	Typ Programming Time, f_{OSC} = 4.0 MHz	Operation
0	0	3.4 ms	Erase and Write in one operation (Atomic Operation)
0	1	1.8 ms	Erase Only
1	0	1.8 ms	Write Only
1	1	–	Reserved for future use

- **Bit 3 – EERIE: EEPROM Ready Interrupt Enable**

Writing EERIE to one enables the EEPROM Ready Interrupt if the I bit in SREG is set. Writing EERIE to zero disables the interrupt. The EEPROM Ready interrupt generates a constant interrupt when EEPE is cleared.

- **Bit 2 – EEMPE: EEPROM Master Write Enable**

The EEMPE bit determines whether setting EEPE to one causes the EEPROM to be written. When EEMPE is set, setting EEPE within four clock cycles will write data to the EEPROM at the selected address If EEMPE is zero, setting EEPE will have no effect. When EEMPE has been written to one by software, hardware clears the bit to zero after four clock cycles. See the description of the EEPE bit for an EEPROM write procedure.

- **Bit 1 – EEPE: EEPROM Write Enable**

The EEPROM Write Enable Signal EEPE is the write strobe to the EEPROM. When address and data are correctly set up, the EEPE bit must be written to one to write the value into the EEPROM. The EEMPE bit must be written to one before a logical one is written to EEPE, otherwise no EEPROM write takes place. The following procedure should be followed when writing the EEPROM (the order of steps 2 and 3 is not essential):

1. Wait until EEPE becomes zero.
2. Write new EEPROM address to EEAR (optional).
3. Write new EEPROM data to EEDR (optional).
4. Write a logical one to the EEMPE bit while writing a zero to EEPE in EECR.
5. Within four clock cycles after setting EEMPE, write a logical one to EEPE.

Caution:

An interrupt between step 4 and step 5 will make the write cycle fail, since the EEPROM Master Write Enable will time-out. If an interrupt routine accessing the EEPROM is interrupting another EEPROM access, the EEAR or EEDR Register will be modified, causing the interrupted

Assembly Code Example

```
EEPROM_read:
  ; Wait for completion of previous write
  sbic EECR,EEPE
  rjmp EEPROM_read
  ; Set up address (r17) in address register
  out  EEAR, r17
  ; Start eeprom read by writing EERE
  sbi  EECR,EERE
  ; Read data from data register
  in   r16,EEDR
  ret
```

C Code Example

```
unsigned char EEPROM_read(unsigned int uiAddress)
{
  /* Wait for completion of previous write */
  while(EECR & (1<<EEPE))
    ;
  /* Set up address register */
  EEAR = uiAddress;
  /* Start eeprom read by writing EERE */
  EECR |= (1<<EERE);
  /* Return data from data register */
  return EEDR;
}
```

8.6.4 GPIOR2 – General Purpose I/O Register 2

Bit	7	6	5	4	3	2	1	0	
0x2B (0x4B)	MSB							LSB	GPIOR2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

8.6.5 GPIOR1 – General Purpose I/O Register 1

Bit	7	6	5	4	3	2	1	0	
0x2A (0x4A)	MSB							LSB	GPIOR1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

8.6.6 GPIOR0 – General Purpose I/O Register 0

Bit	7	6	5	4	3	2	1	0	
0x1E (0x3E)	MSB							LSB	GPIOR0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 4 - OSISEL0: Oscillator Sampling Interface Select 0**

Table 9-5. OSISEL Bit Description

OSISEL0	Oscillator source
0	ULP Oscillator
1	Slow RC Oscillator

- **Bit 1 – OSIST: Oscillator Sampling Interface Status**

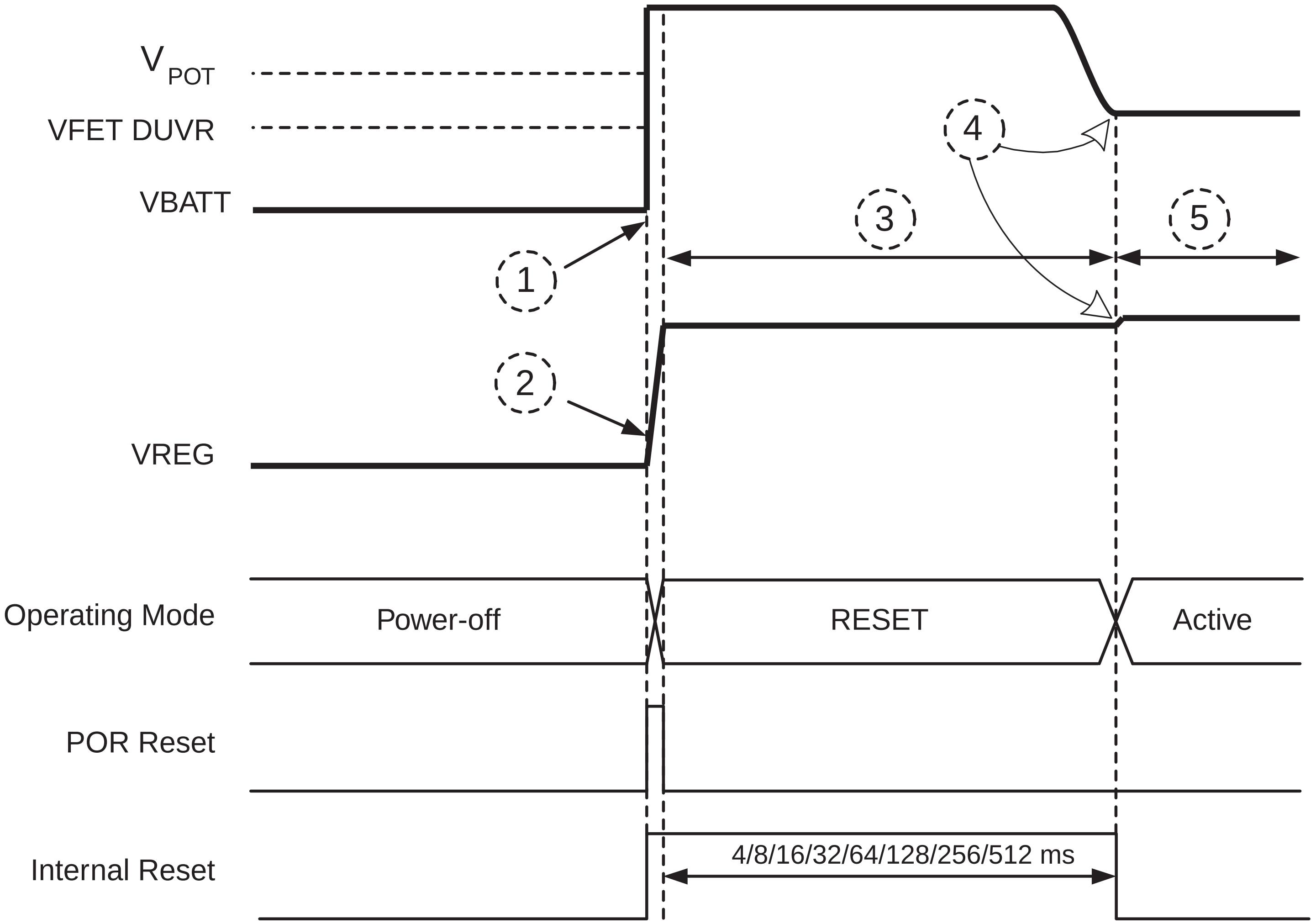
This bit continuously displays the phase of the prescaled clock. This bit can be polled by the CPU to determine the rising and falling edges of the prescaled clock.

- **Bit 0 – OSIEN: Oscillator Sampling Interface Enable**

Setting this bit enables the Oscillator Sampling Interface. When this bit is cleared, the Oscillator Sampling Interface is disabled.

Notes: 1. The prescaler is reset each time the OSICSR register is written, and hence each time a new oscillator source is selected.

Figure 11-2. Normal Start-up Sequence in Power-off.



1. The charger voltage pulls the BATT pin above the Power-on Threshold Voltage (V_{POT}).
2. When V_{BATT} rises above V_{POT}, ATmega8HVA/16HVA turns on the Voltage Regulator and VREG starts to rise. The POR reset will go high while VREG is rising and initiate the internal reset state of the chip. The external FETs are initially switched off.
3. The internal reset is held high after POR reset goes low for a time given by t_{TOUT}, see "System Control and Reset" on page 41. While the chip is in reset, VREF calibration registers will be reset to their default values. The VREG and BOD levels are both referenced to the VREF voltage. In reset all these voltage levels will therefore have default values. Both FETs are switched completely off in this state.
4. As soon as the internal reset goes low, the chip will start operating in DUVR mode (for details on DUVR mode, see "DUVR – Deep Under-Voltage Recovery Mode operation" on page 137 and application note AVR354). In DUVR mode the FET driver controls the gate voltage of the Charge FET to get a voltage at the VFET pin given by the VFET level specified in Table 29-5 on page 170. This causes the BATT voltage to decrease. Note that DUVR mode will only regulate the VFET voltage as long as the cell voltage is lower than the VFET_DUVR level. For high cell voltages, DUVR mode will not have any impact. DUVR mode may be disabled by SW as soon as the chip enters ACTIVE mode.

11.4 Register Description

11.4.1 MCUSR – MCU Status Register

The MCU Status Register provides information on which reset source caused an MCU reset.

Bit	7	6	5	4	3	2	1	0	
0x34 (0x54)	–	–	–	OCDRF	WDRF	BODRF	EXTRF	PORF	MCUSR
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	See Bit Description					

- **Bits 7:5 – Res: Reserved Bits**

These bits are reserved bits in the ATmega8HVA/16HVA, and will always read as zero.

- **Bit 4 – OCDRF: OCD Reset Flag**

This bit is set if a debugWIRE Reset occurs. The bit is reset by a Power-on Reset, or by writing a logic zero to the flag.

- **Bit 3 – WDRF: Watchdog Reset Flag**

This bit is set if a Watchdog Reset occurs. The bit is reset by a Power-on Reset, or by writing a logic zero to the flag.

- **Bit 2 – BODRF: Brown-out Reset Flag**

This bit is set if a Brown-out Reset occurs. This bit is reset by a Power-on Reset, or by writing a logic zero to the flag.

- **Bit 1 – EXTRF: External Reset Flag**

This bit is set if an External Reset occurs. The bit is reset by a Power-on Reset, or by writing a logic zero to the flag.

- **Bit 0 – PORF: Power-on Reset Flag**

This bit is set if a Power-on Reset occurs. The bit is reset only by writing a logic zero to the flag.

To make use of the Reset flags to identify a reset condition, the user should read and then reset the MCUSR as early as possible in the program. If the register is cleared before another reset occurs, the source of the reset can be found by examining the reset flags.

11.4.2 WDTCSR – Watchdog Timer Control Register

Bit	7	6	5	4	3	2	1	0	
	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	WDTCSR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	X	0	0	0	

- **Bit 7 - WDIF: Watchdog Interrupt Flag**

This bit is set when a time-out occurs in the Watchdog Timer and the Watchdog Timer is configured for interrupt. WDIF is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, WDIF is cleared by writing a logic one to the flag. When the I-bit in SREG and WDIE are set, the Watchdog Time-out Interrupt is executed.

Table 14-1. Generic Description of Overriding Signals for Alternate Functions

Signal Name	Full Name	Description
PVOE	Port Value Override Enable	If this signal is set and the Output Driver is enabled, the port value is controlled by the PVOV signal. If PVOE is cleared, and the Output Driver is enabled, the port Value is controlled by the PORTxn Register bit.
PVOV	Port Value Override Value	If PVOE is set, the port value is set to PVOV, regardless of the setting of the PORTxn Register bit.
DIEOE	Digital Input Enable Override Enable	If this bit is set, the Digital Input Enable is controlled by the DIEOV signal. If this signal is cleared, the Digital Input Enable is determined by MCU state (Normal mode, sleep mode).
DIEOV	Digital Input Enable Override Value	If DIEOE is set, the Digital Input is enabled/disabled when DIEOV is set/cleared, regardless of the MCU state (Normal mode, sleep mode).
DI	Digital Input	This is the Digital Input to alternate functions. In the figure, the signal is connected to the output of the schmitt trigger but before the synchronizer. Unless the Digital Input is used as a clock source, the module with the alternate function will use its own synchronizer.

14.4.1 Alternate Functions of Port C

The Port C pins with alternate functions are shown in Table 14-2.

Table 14-2. Port C Pins Alternate Functions

Port Pin	Alternate Function
PC0	INT0/ ICP0 (External Interrupt 0 or Timer/Counter0 Input Capture Trigger)

The alternate pin configuration is as follows:

- **INT0 - Port C, Bit 0**

INT0: External Interrupt Source 0. The PC0 pin can serve as external interrupt source. INT0 can be used as an interrupt pin regardless of whether another special function is enabled or not.

Table 14-3 relates the alternate functions of Port C to the overriding signals shown in Figure 14-3 on page 60.

Table 14-3. Overriding Signals for Alternate Functions in PC0

Signal Name	PC0/INT0
PVOE	0
DIEOE	INT Enable
DIEOV	1
DI	INT0 INPUT

14.5 Register Description

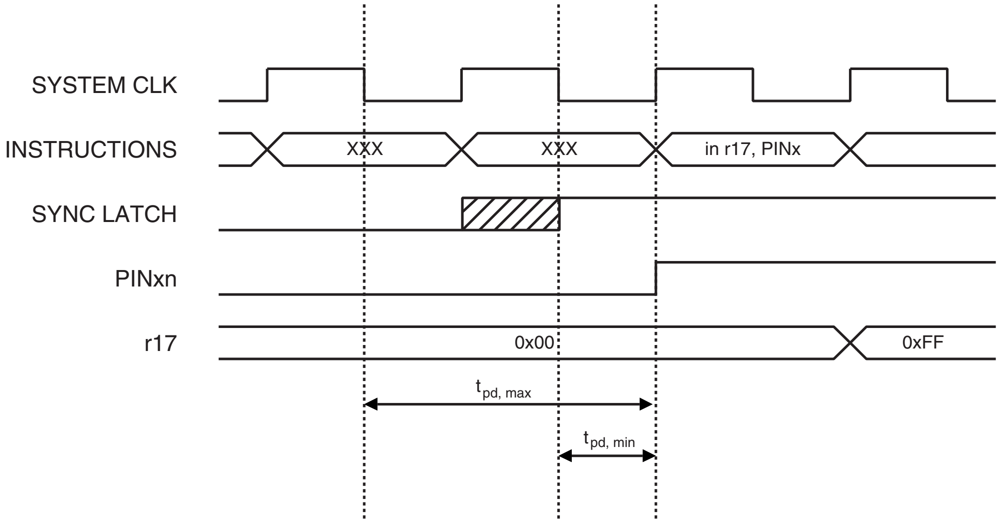
14.5.1 PORTC – Port C Data Register

Bit	7	6	5	4	3	2	1	0	
0x08 (0x28)	–	–	–	–	–	–	–	**PORTC0**	**PORTC**
Read/Write	R	R	R	R	R	R	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

14.5.2 PINC – Port C Input Pins Address

Bit	7	6	5	4	3	2	1	0	
0x06 (0x26)	–	–	–	–	–	–	–	**PINC0**	**PINC**
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

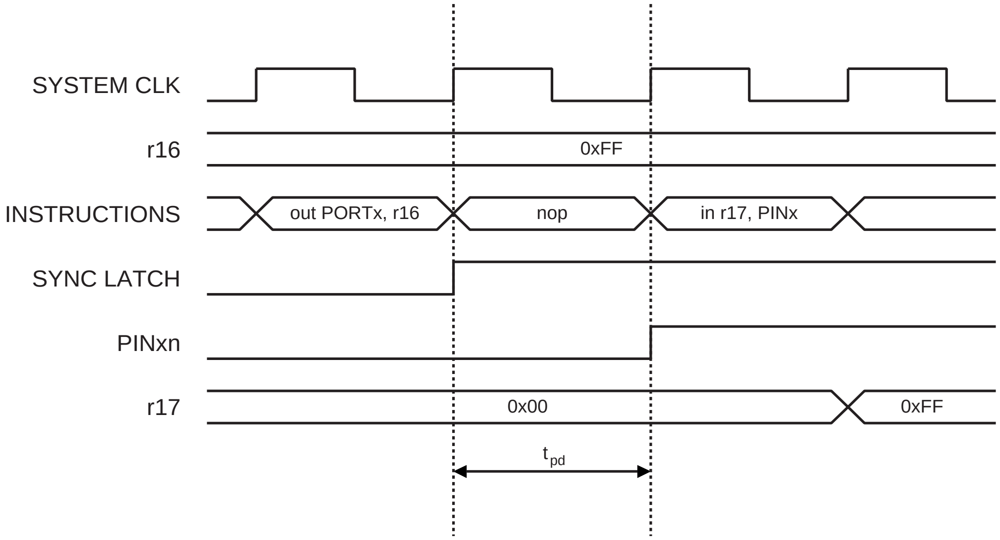
Figure 15-3. Synchronization when Reading an Externally Applied Pin value



Consider the clock period starting shortly after the first falling edge of the system clock. The latch is closed when the clock is low, and goes transparent when the clock is high, as indicated by the shaded region of the “SYNC LATCH” signal. The signal value is latched when the system clock goes low. It is clocked into the PINxn Register at the succeeding positive clock edge. As indicated by the two arrows tpd,max and tpd,min, a single signal transition on the pin will be delayed between ½ and 1½ system clock period depending upon the time of assertion.

When reading back a software assigned pin value, a nop instruction must be inserted as indicated in Figure 15-4. The out instruction sets the “SYNC LATCH” signal at the positive edge of the clock. In this case, the delay tpd through the synchronizer is 1 system clock period.

Figure 15-4. Synchronization when Reading a Software Assigned Pin Value



The following code example shows how to set port B pins 0 and 1 high, 2 and 3 low, and define the port pins from 4 to 7 as input with pull-ups assigned to port pins 6 and 7. The resulting pin values are read back again, but as previously discussed, a nop instruction is included to be able to read back the value recently assigned to some of the pins.

Assembly Code Example[1]

```
   ...
   ; Define pull-ups and set outputs high
   ; Define directions for port pins
   ldi  r16,(1<<PB7)|(1<<PB6)|(1<<PB1)|(1<<PB0)
   ldi  r17,(1<<DDB3)|(1<<DDB2)|(1<<DDB1)|(1<<DDB0)
   out  PORTB,r16
   out  DDRB,r17
   ; Insert nop for synchronization
   nop
   ; Read port pins
   in   r16,PINB
   ...
```

C Code Example

```
 unsigned char i;
   ...
   /* Define pull-ups and set outputs high */
   /* Define directions for port pins */
   PORTB = (1<<PB7)|(1<<PB6)|(1<<PB1)|(1<<PB0);
   DDRB = (1<<DDB3)|(1<<DDB2)|(1<<DDB1)|(1<<DDB0);
   /* Insert nop for synchronization*/
   _NOP();
   /* Read port pins */
   i = PINB;
   ...
```

Note: 1. For the assembly program, two temporary registers are used to minimize the time from pull-ups are set on pins 0, 1, 6, and 7, until the direction bits are correctly set, defining bit 2 and 3 as low and redefining bits 0 and 1 as strong high drivers.

15.2.5 Digital Input Enable and Sleep Modes

As shown in Figure 15-2 on page 64, the digital input signal can be clamped to ground at the input of the schmitt-trigger. The signal denoted SLEEP in the figure, is set by the MCU Sleep Controller in Power-save mode to avoid high power consumption if some input signals are left floating, or have an analog signal level close to $V_{REG}/2$.

SLEEP is overridden for port pins enabled as external interrupt pins. If the external interrupt request is not enabled, SLEEP is active also for these pins. SLEEP is also overridden by various other alternate functions as described in ”Alternate Port Functions” on page 68.

If a logic high level (“one”) is present on an asynchronous external interrupt pin configured as “Interrupt on Rising Edge, Falling Edge, or Any Logic Change on Pin” while the external interrupt is *not* enabled, the corresponding External Interrupt Flag will be set when resuming from the above mentioned Sleep mode, as the clamping in these sleep mode produces the requested logic change.

15.2.6 Unconnected Pins

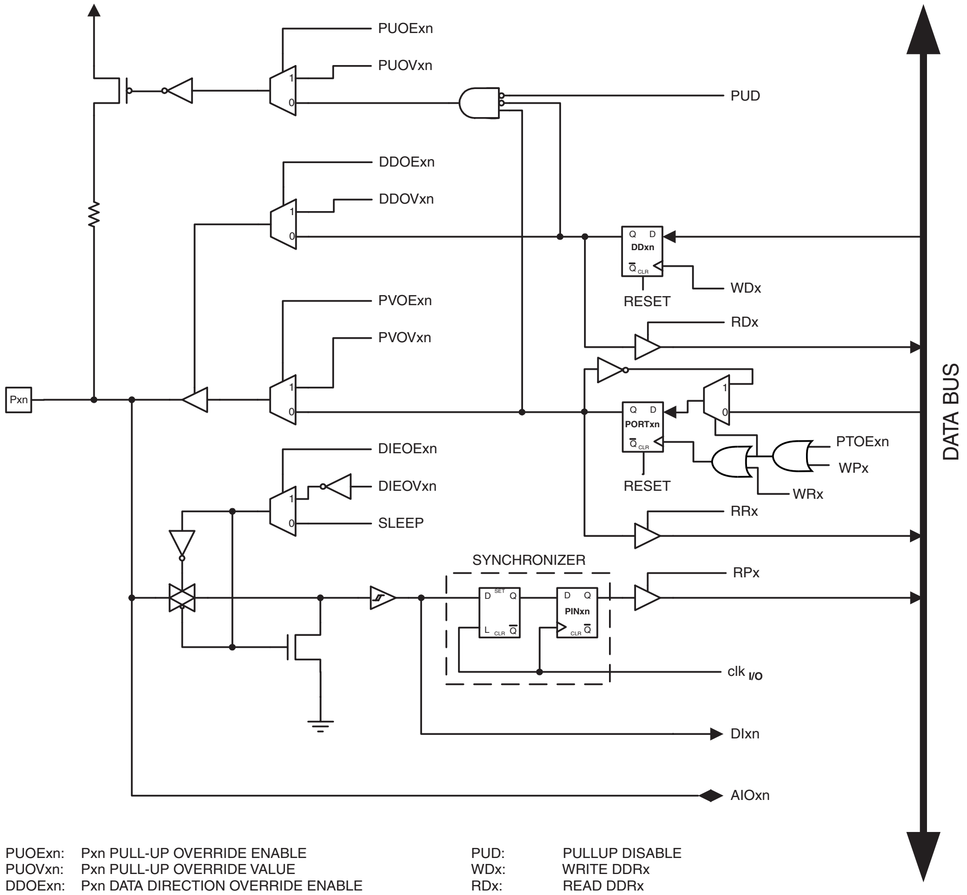
If some pins are unused, it is recommended to ensure that these pins have a defined level. Even though most of the digital inputs are disabled in the deep sleep modes as described above, floating inputs should be avoided to reduce current consumption in all other modes where the digital inputs are enabled (Reset, Active mode and Idle mode).

The simplest method to ensure a defined level of an unused pin, is to enable the internal pull-up. In this case, the pull-up will be disabled during reset. If low power consumption during reset is important, it is recommended to use an external pull-up or pull-down. Connecting unused pins directly to V_{CC} or GND is not recommended, since this may cause excessive currents if the pin is accidentally configured as an output.

15.3 Alternate Port Functions

Many low voltage port pins have alternate functions in addition to being general digital I/Os. Figure 15-5 shows how the port pin control signals from the simplified Figure 15-2 on page 64 can be overridden by alternate functions. The overriding signals may not be present in all port pins, but the figure serves as a generic description applicable to all port pins in the AVR microcontroller family.

Figure 15-5. Alternate Port Functions[1]



PUOExn:	Pxn PULL-UP OVERRIDE ENABLE	PUD:	PULLUP DISABLE
PUOVxn:	Pxn PULL-UP OVERRIDE VALUE	WDx:	WRITE DDRx
DDOExn:	Pxn DATA DIRECTION OVERRIDE ENABLE	RDx:	READ DDRx
DDOVxn:	Pxn DATA DIRECTION OVERRIDE VALUE	RRx:	READ PORTx REGISTER
PVOExn:	Pxn PORT VALUE OVERRIDE ENABLE	WRx:	WRITE PORTx
PVOVxn:	Pxn PORT VALUE OVERRIDE VALUE	RPx:	READ PORTx PIN
DIEOExn:	Pxn DIGITAL INPUT-ENABLE OVERRIDE ENABLE	WPx:	WRITE PINx
DIEOVxn:	Pxn DIGITAL INPUT-ENABLE OVERRIDE VALUE	$clk_{I/O}$:	I/O CLOCK
SLEEP:	SLEEP CONTROL	DIxn:	DIGITAL INPUT PIN n ON PORTx
PTOExn:	Pxn, PORT TOGGLE OVERRIDE ENABLE	AIOxn:	ANALOG INPUT/OUTPUT PIN n ON PORTx

17.10 Register Description

17.10.1 TCCRnA – Timer/Counter n Control Register A

Bit	7	6	5	4	3	2	1	0	
	TCWn	ICENn	ICNCn	ICESn	ICSn	–	–	WGMn0	TCCRnA
Read/Write	R/W	R/W	R/W	R/W	R/W	R	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7– TCWn: Timer/Counter Width**

When this bit is written to one 16-bit mode is selected. The Timer/Counter width is set to 16-bits and the Output Compare Registers OCRnA and OCRnB are combined to form one 16-bit Output Compare Register. Because the 16-bit registers TCNTnH/L and OCRnB/A are accessed by the AVR CPU via the 8-bit data bus, special procedures must be followed. These procedures are described in section ”Accessing Registers in 16-bit Mode” on page 86.

- **Bit 6– ICENn: Input Capture Mode Enable**

The Input Capture Mode is enabled when this bit is written to one.

- **Bit 5 – ICNCn: Input Capture Noise Canceler**

Setting this bit activates the Input Capture Noise Canceler. When the noise canceler is activated, the input from the Input Capture Source is filtered. The filter function requires four successive equal valued samples of the Input Capture Source for changing its output. The Input Capture is therefore delayed by four System Clock cycles when the noise canceler is enabled.

- **Bit 4 – ICESn: Input Capture Edge Select**

This bit selects which edge on the Input Capture Source that is used to trigger a capture event. When the ICESn bit is written to zero, a falling (negative) edge is used as trigger, and when the ICESn bit is written to one, a rising (positive) edge will trigger the capture. When a capture is triggered according to the ICESn setting, the counter value is copied into the Input Capture Register. The event will also set the Input Capture Flag (ICFn), and this can be used to cause an Input Capture Interrupt, if this interrupt is enabled.

- **Bit 3 - ICSn: Input Capture Select**

When written to a logic one, this bit selects the alternate Input Capture Source as trigger for the Timer/Counter input capture function. To trigger the Timer/Counter Input Capture interrupt, the ICIEn bit in the Timer Interrupt Mask Register (TIMSK) must be set. See Table 17-3 on page 84 and Table 17-4 on page 84.

- **Bits 2:0 – Res: Reserved Bits**

These bits are reserved bits in the ATmega8HVA/16HVA and will always read as zero.

- **Bit 0 – WGMn0: Waveform Generation Mode**

This bit controls the counting sequence of the counter, the source for maximum (TOP) counter value, see Figure 17-6 on page 85. Modes of operation supported by the Timer/Counter unit are: Normal mode (counter) and Clear Timer on Compare Match (CTC) mode (see ”Timer/Counter Timing Diagrams” on page 85).

Instantaneous Current Interrupt should be enabled as wake-up source by setting the CADICIE bit. The device will then wake-up from sleep after each single IC measurement. To check if Regular Current Detection has occurred the Regular Current Detection flag, CADRCIF, should be read.

19.5 Offset Canceling by Polarity Switching

The CC-ADC offers Polarity Switching for internal offset canceling. By switching the polarity of the sampled input signal at selected time intervals, the internal voltage offset of the CC-ADC will cancel at the output. This feature prevents the CC-ADC from accumulating an offset error over time.

19.6 Configuration and Usage

While the CC-ADC is converting, the CPU can enter sleep mode and wait for an interrupt. After adding the conversion data for the Coulomb Counting, the CPU can go back to sleep again. This reduces the CPU workload, and allows more time spent in low power modes, reducing power consumption.

To use the CC-ADC, the bandgap voltage reference must be enabled. See ”Voltage Reference and Temperature Sensor” on page 117.

The CC-ADC will not consume power when CADEN is cleared. It is therefore recommended to switch off the CC-ADC whenever the Coulomb Counter or Regular Current Detection functions are not used. The CC-ADC is automatically disabled in Power-off mode.

After the CC-ADC is enabled by setting the CADEN bit, the first three Instantaneous conversions do not contain useful data and should be ignored. This also applies after clearing the CADSE bit, or after changing the CADPOL or CADVSE bits.

The conversion times and sampling intervals are controlled by the Slow RC Oscillator, and will depend on its actual frequency. To obtain accurate coulomb counting results, the actual conversion time must be calculated. Refer to ”Slow RC Oscillator” on page 26 for details.

19.7 Register Description

19.7.1 CADCSRA - CC-ADC Control and Status Register A

Bit	7	6	5	4	3	2	1	0	
(0xE4)	CADEN	CADPOL	CADUB	CADAS1	CADAS0	CADSI1	CADSI0	CADSE	CADCSRA
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 - CADEN: CC-ADC Enable**

When the CADEN bit is cleared (zero), the CC-ADC is disabled, and any ongoing conversions will be terminated. When the CADEN bit is set (one), the CC-ADC will continuously measure the voltage drop over the external sense resistor R_{SENSE}. In Power-off, the CC-ADC is always disabled. Note that the bandgap voltage reference must be enabled, see ”Voltage Reference and Temperature Sensor” on page 117.

- **Bit 6 - CADPOL: CC-ADC Polarity**

The CADPOL bit is used to change input sampling polarity in the Sigma Delta Modulator. Writing this bit to one, the polarity will be negative. When the bit is zero, the polarity will be positive.

19.7.5 CADRC- CC-ADC Regular Current

Bit	7	6	5	4	3	2	1	0	
(0xE6)	CADRC[7:0]								CADRC
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The CC-ADC Regular Current Register determines the threshold level for the Regular Current detection. When the result of a CC-ADC Instantaneous Current conversion has an absolute value greater than, or equal to, the Regular Current level, the CC-ADC Regular Current Interrupt Flag is set.

The value in this register defines the eight least significant bits of the Regular Current level. The most significant bits of the Regular Current level are always zero. The programmable range for the Regular Current level is given in Table 19-3.

Table 19-3. Programmable Range for the Regular Current Level

		Minimum	Maximum	Step size
Voltage (µV)		0	6848	26.9
Current (mA)	R_{SENSE} = 1 mΩ	0	6848	26.9
	R_{SENSE} = 5 mΩ	0	1370	5.4
	R_{SENSE} = 10 mΩ	0	685	2.7

The CC-ADC Regular Current Register does not affect the setting of the CC-ADC Conversion Complete Interrupt Flag.

20. Voltage ADC – 5-channel General Purpose 12-bit Sigma-Delta ADC

20.1 Features

- **12-bit Resolution**
- **519µs Conversion Time @ 1 MHz clk$_{VADC}$**
- **Two Differential Input Channels for Cell Voltage Measurements**
- **Three Single Ended Input Channels**
- **0.2x Pre-scaling of Cell Voltages**
- **Interrupt on V-ADC Conversion Complete**

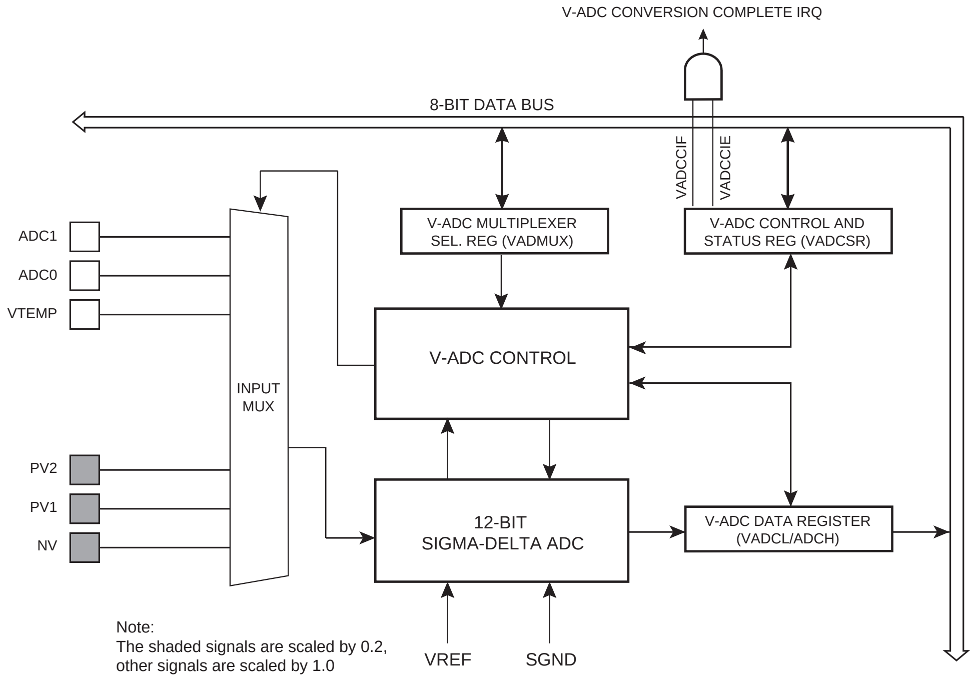
20.2 Overview

The ATmega8HVA/16HVA features a 12-bit Sigma-Delta ADC.

The Voltage ADC (V-ADC) is connected to five different sources through the Input Multiplexer. There are two differential channels for Cell Voltage measurements. These channels are scaled 0.2x to comply with the Full Scale range of the V-ADC. In addition there are three single ended channels referenced to SGND. One channel is for measuring the internal temperature sensor VPTAT and two channels for measuring the voltage at ADC0 and ADC1.

When the V-ADC is not used, power consumption can be minimized by writing the PRVADC bit in PRR0 to one. See "PRR0 – Power Reduction Register 0" on page 39 for details on how to use the PRVADC bit.

Figure 20-1. Voltage ADC Block Schematic


V-ADC CONVERSION COMPLETE IRQ
8-BIT DATA BUS
VADCCIF
VADCCIE
ADC1
ADC0
VTEMP
PV2
PV1
NV
INPUT MUX
V-ADC MULTIPLEXER SEL. REG (VADMUX)
V-ADC CONTROL AND STATUS REG (VADCSR)
V-ADC CONTROL
12-BIT SIGMA-DELTA ADC
V-ADC DATA REGISTER (VADCL/ADCH)
VREF
SGND

Note:
The shaded signals are scaled by 0.2,
other signals are scaled by 1.0

20.3 Operation

To enable V-ADC conversions, the V-ADC Enable bit, VADEN, in V-ADC Control and Status Register – VADCSR must be set. If this bit is cleared, the V-ADC will be switched off, and any ongoing conversions will be terminated. The V-ADC is automatically disabled in Power-save and

27.2.1 High Byte

Table 27-3. Fuse High Byte

Bit No	Fuse High Byte	Description	Default Value
7:2	–	–	1 (unprogrammed)
1	OSCSEL1	Oscillator Select 1	0 (programmed)
0	OSCSEL0	Oscillator Select 0	1 (unprogrammed)

Note: 1. The default OSCSEL1:0 setting should not be changed. OSCSEL1:0 = ‘00’ is reserved for test purposes. Other values are reserved for future use.

27.2.2 Low Byte

Table 27-4. Fuse Low Byte

Bit No	Fuse Low Byte	Description	Default Value
7	WDTON[3]	Watchdog Timer always on	1 (unprogrammed)
6	EESAVE	EEPROM memory is preserved through the Chip Erase	1 (unprogrammed, EEPROM not preserved)
5	SPIEN[2]	Enable SPI Programming Interface	0 (programmed, SPI prog. enabled)
4	DWEN	Enable debugWIRE	1 (unprogrammed)
3	SELFPRGEN	Self Programming enable	1 (unprogrammed)
2	SUT2[1]	Select start-up time	1 (unprogrammed)
1	SUT1[1]	Select start-up time	1 (unprogrammed)
0	SUT0[1]	Select start-up time	1 (unprogrammed)

Notes: 1. See Table 9-1 on page 25 for details about start-up time.
2. The SPIEN Fuse is not accessible in SPI programming mode.
3. See ”WDTCSR – Watchdog Timer Control Register” on page 49 for details.

The status of the Fuse bits is not affected by Chip Erase. Note that the Fuse bits are locked if Lock bit1 (LB1) is programmed. Program the Fuse bits before programming the Lock bits.

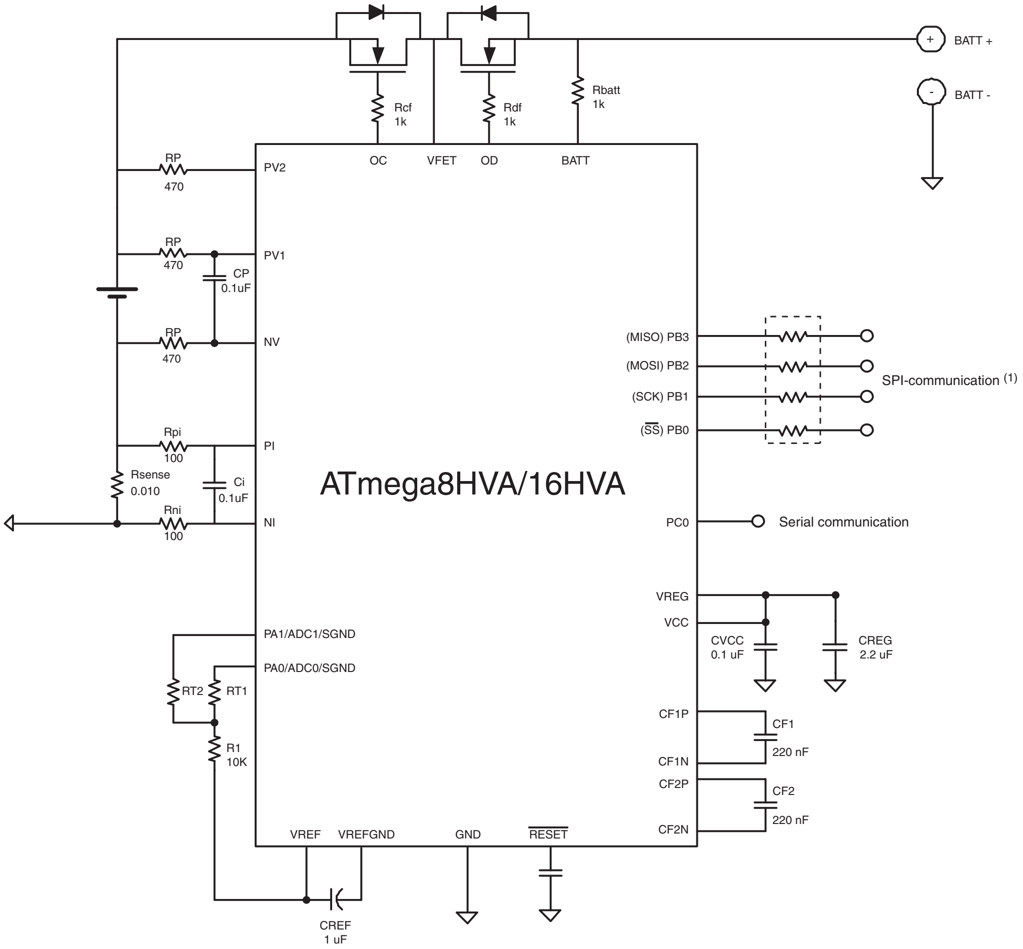
27.2.3 Latching of Fuses

The fuse values are latched when the device enters programming mode and changes of the fuse values will have no effect until the part leaves Programming mode. This does not apply to the EESAVE Fuse which will take effect once it is programmed. The fuses are also latched on Power-up in Normal mode.

Table 27-14. High-voltage Serial Programming Instruction Set for ATmega8HVA/16HVA

Instruction		Instruction Format				Operation Remarks
		Instr.1/5	Instr.2/6	Instr.3	Instr.4	
Chip Erase	SDI	0_1000_0000_00	0_0000_0000_00	0_0000_0000_00		
	SII	0_0100_1100_00	0_0110_0100_00	0_0110_1100_00		
	SDO	x_xxxx_xxxx_xx	x_xxxx_xxxx_xx	x_xxxx_xxxx_xx		
Load “Write Flash” Command	SDI	0_0001_0000_00				
	SII	0_0100_1100_00				
	SDO	x_xxxx_xxxx_xx				
Load Flash Page Buffer	SDI	0_ **bbbb_bbbb** _00	0_**eeee_eeee**_00	0_**dddd_dddd**_00	0_0000_0000_00	
	SII	0_0000_1100_00	0_0010_1100_00	0_0011_1100_00	0_0111_1101_00	
	SDO	x_xxxx_xxxx_xx	x_xxxx_xxxx_xx	x_xxxx_xxxx_xx	x_xxxx_xxxx_xx	
	SDI	0_0000_0000_00				
	SII	0_0111_1100_00				
	SDO	x_xxxx_xxxx_xx				
Load Flash High Address and Program Page	SDI	0_**aaaa_aaaa**_00	0_0000_0000_00	0_0000_0000_00		
	SII	0_0001_1100_00	0_0110_0100_00	0_0110_1100_00		
	SDO	x_xxxx_xxxx_xx	x_xxxx_xxxx_xx	x_xxxx_xxxx_xx		
Load “Read Flash” Command	SDI	0_0000_0010_00				
	SII	0_0100_1100_00				
	SDO	x_xxxx_xxxx_xx				
Read Flash Low and High Bytes	SDI	0_**bbbb_bbbb**_00	0_**aaaa_aaaa**_00	0_0000_0000_00	0_0000_0000_00	
	SII	0_0000_1100_00	0_0001_1100_00	0_0110_1000_00	0_0110_1100_00	
	SDO	x_xxxx_xxxx_xx	x_xxxx_xxxx_xx	x_xxxx_xxxx_xx	**q_qqqq_qqq**x_xx	
	SDI	0_0000_0000_00	0_0000_0000_00			
	SII	0_0111_1000_00	0_0111_1100_00			
	SDO	x_xxxx_xxxx_xx	**p_pppp_ppp**x_xx			
Load “Write EEPROM” Command	SDI	0_0001_0001_00				
	SII	0_0100_1100_00				
	SDO	x_xxxx_xxxx_xx				
Load EEPROM Page Buffer	SDI	0_**bbbb_bbbb**_00	0_**eeee_eeee**_00	0_0000_0000_00	0_0000_0000_00	
	SII	0_0000_1100_00	0_0010_1100_00	0_0110_1101_00	0_0110_1100_00	
	SDO	x_xxxx_xxxx_xx	x_xxxx_xxxx_xx	x_xxxx_xxxx_xx	x_xxxx_xxxx_xx	
Program EEPROM Page	SDI	0_0000_0000_00	0_0000_0000_00			
	SII	0_0110_0100_00	0_0110_1100_00			
	SDO	x_xxxx_xxxx_xx	x_xxxx_xxxx_xx			
Write EEPROM Byte	SDI	0_**bbbb_bbbb**_00	0_**eeee_eeee**_00	0_0000_0000_00	0_0000_0000_00	
	SII	0_0000_1100_00	0_0010_1100_00	0_0110_1101_00	0_0110_0100_00	
	SDO	x_xxxx_xxxx_xx	x_xxxx_xxxx_xx	x_xxxx_xxxx_xx	x_xxxx_xxxx_xx	
	SDI	0_0000_0000_00				
	SII	0_0110_1100_00				
	SDO	x_xxxx_xxxx_xx				
Load “Read EEPROM” Command	SDI	0_0000_0011_00				
	SII	0_0100_1100_00				
	SDO	x_xxxx_xxxx_xx				

Figure 28-2. Operating Circuit Diagram, 1-cell



Notes:
1. The series resistors on the SPI lines are required for In-System Programming and On-chip Debug support. The value of the series resistor depends on the application. A value of 10k will ensure that programming and debugging operates correctly, but it must be determined by the end user that this does not affect the normal operation of the SPI interface.
2. PA1 should be connected to SNGD when measuring V(RT_2).
PA0 should be connected to SNGD when measuring V(RT_1).

29.4 General I/O Lines characteristics

Table 29-3. [1]T_A = -10°C to 70°C, V_{CC} = 3.3V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage, Except RESET pin		-0.5		$0.3V_{CC}$[2]	V
V_{IL1}	Input Low Voltage, RESET pin				$0.3V_{CC}$[2]	
V_{IH}	Input High Voltage, Except RESET pin		$0.6V_{CC}$[3]		$V_{CC} + 0.5$	V
V_{IH1}	Input High Voltage, RESET pin		$0.9V_{CC}$[3]		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	I_{OL} = 5mA			0.5	V
V_{OH}	Output High Voltage	I_{OH} = 2 mA	2.3			V
I_{IL}	Input Leakage Current I/O Pin	Pin low (absolute value)			1	µA
I_{IH}	Input Leakage Current I/O Pin	Pin high (absolute value)			1	µA
R_{RST}	Reset Pull-up Resistor		30		60	kΩ
R_{PU}	I/O Pin Pull-up Resistor		20		50	kΩ

Notes:
1. Applicable for all except PC0.
2. "Max" means the highest value where the pin is guaranteed to be read as low
3. "Min" means the lowest value where the pin is guaranteed to be read as high
4. Although each I/O port can sink more than the test conditions (5 mA at V_{CC} = 3.3V) under steady state conditions (non-transient), the following must be observed:
   - The sum of all IOL should not exceed 20 mA.
   If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test condition.
5. Although each I/O port can source more than the test conditions (2 mA at V_{CC} = 3.3V) under steady state conditions (non-transient), the following must be observed:
   - The sum of all IOH should not exceed 2 mA.

Table 29-4. PC0 Characteristics (T_A = -10°C to 70°C unless otherwise specified)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage		-0.5	0.8[1]	V
V_{IH}	Input High-voltage		2.1[2]	5.5	V
V_{OL}	Output Low-voltage	350 µA sink current	0	0.4	V
t_r[3]	Rise Time			300	ns
t_{of}[3]	Output Fall Time from V_{IHmin} to V_{ILmax}	C_b < 400 pF[4]		250	ns
t_{SP}[3]	Spikes Suppressed by Input Filter		0	50	ns
I_i[3]	Input Current	$0.1V_{BUS} < V_i < 0.9V_{BUS}$	-5	5	µA
C_i[3]	Capacitance			10	pF

Notes:
1. "Max" means the highest value where the pin is guaranteed to be read as low
2. "Min" means the lowest value where the pin is guaranteed to be read as high
3. This value is not tested in production.
4. C_b = capacitance of one bus line in pF

33. Ordering Information

33.1 ATmega8HVA

Speed (MHz)	Power Supply	Ordering Code	Package[1]	Operation Range
1 - 4	1.8 - 9.0V	ATmega8HVA-4CKU ATmega8HVA-4TU	36CK1 28T	-20 to +85°C

Notes: 1. Pb-free packaging, complies with the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

Package Type	
36CK1	36-pad, (6.50 x 3.50 x 0.85 mm Body, 0.60 mm Pitch), Land Grid Array (LGA) Package.
28T	28-lead (8 x 13.4 mm) Plastic Thin Small Outline Package, Type I (TSOP)