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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	EBI/EMI, I ² C, IrDA, SCI, SPI, SSI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52305adfp-30

1.2 List of Products

Table 1.3 and Table 1.4 are a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products: D Version (T_a = –40 to +85°C) (1/2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature
RX231	R5F52318ADLA	R5F52318ADLA#20	PTLG0100KA-A	512 Kbytes	64 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Available	–40 to +85°C
	R5F52318BDLA	R5F52318BDLA#20						Available	Available	Available	
	R5F52318ADFP	R5F52318ADFP#30	PLQP0100KB-B					Not available	Not available	Available	
	R5F52318BDFP	R5F52318BDFP#30						Available	Available	Available	
	R5F52318ADND	R5F52318ADND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52318BDND	R5F52318BDND#U0						Available	Available	Available	
	R5F52318ADFM	R5F52318ADFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52318BDFM	R5F52318BDFM#30						Available	Available	Available	
	R5F52318ADNE	R5F52318ADNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52318BDNE	R5F52318BDNE#U0						Available	Not available	Available	
	R5F52318ADFL	R5F52318ADFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52318BDFL	R5F52318BDFL#30						Available	Not available	Available	
	R5F52317ADLA	R5F52317ADLA#20	PTLG0100KA-A	384 Kbytes				Not available	Not available	Available	
	R5F52317BDLA	R5F52317BDLA#20						Available	Available	Available	
	R5F52317ADFP	R5F52317ADFP#30	PLQP0100KB-B					Not available	Not available	Available	
	R5F52317BDFP	R5F52317BDFP#30						Available	Available	Available	
	R5F52317ADND	R5F52317ADND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52317BDND	R5F52317BDND#U0						Available	Available	Available	
	R5F52317ADFM	R5F52317ADFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52317BDFM	R5F52317BDFM#30						Available	Available	Available	
	R5F52317ADNE	R5F52317ADNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52317BDNE	R5F52317BDNE#U0						Available	Not available	Available	
	R5F52317ADFL	R5F52317ADFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52317BDFL	R5F52317BDFL#30						Available	Not available	Available	
	R5F52316ADLA	R5F52316ADLA#20	PTLG0100KA-A	256 Kbytes	32 Kbytes			Not available	Not available	Available	
	R5F52316CDLA	R5F52316CDLA#20						Not available	Not available	Not available	
	R5F52316ADFP	R5F52316ADFP#30	PLQP0100KB-B					Not available	Not available	Available	
	R5F52316CDFP	R5F52316CDFP#30						Not available	Not available	Not available	
	R5F52316CDLF	R5F52316CDLF#U0	PWL0064KA-A					Not available	Not available	Not available	
	R5F52316ADND	R5F52316ADND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52316CDND	R5F52316CDND#U0						Not available	Not available	Not available	
	R5F52316ADFM	R5F52316ADFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52316CDFM	R5F52316CDFM#30						Not available	Not available	Not available	
	R5F52316ADNE	R5F52316ADNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52316CDNE	R5F52316CDNE#U0						Not available	Not available	Not available	

Table 1.7 List of Pins and Pin Functions (100-Pin LFQFP) (2/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, IIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
42		P52	RD#				TS18	
43		P51	WR1#/BC1#/WAIT#				TS19	
44		P50	WR0#/WR#				TS20	
45	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA			CACREF
46		PC6	A22/CS1#	MTIOC3C/MTCLKA/TMC12	RXD8/SMISO8/SSCL8/MOSIA		TS22	
47		PC5	A21/CS2#/WAIT#	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA		TS23	
48		PC4	A20/CS3#	MTIOC3D/MTCLKC/TMC11/POE0#	SCK5/CTS8#/RTS8#/SS8#/SSLA0	SDHI_D1	TSCAP	
49		PC3	A19	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5/IRTXD5	SDHI_D0	TS27	
50		PC2	A18	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/SSLA3/IRRXD5	SDHI_D3	TS30	
51		PC1	A17	MTIOC3A/TCLKD	SCK5/SSLA2		TS33	
52		PC0	A16	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/SSLA1		TS35	
53		PB7	A15	MTIOC3B/TIOCB5	TXD9/SMOSI9/SSDA9	SDHI_D2		
54		PB6	A14	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9	SDHI_D1		
55		PB5	A13	MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOCB4	SCK9/USB0_VBUS	SDHI_CD		
56		PB4	A12	TIOCA4	CTS9#/RTS9#/SS9#			
57		PB3	A11	MTIOC0A/MTIOC4A/TMO0/POE3#/TIOC3D/TCLKD	SCK6	SDHI_W P		
58		PB2	A10	TIOCC3/TCLKC	CTS6#/RTS6#/SS6#			
59		PB1	A9	MTIOC0C/MTIOC4C/TMC10/TIOCB3	TXD6/SMOSI6/SSDA6	SDHI_CLK		IRQ4/CMPOB1
60	VCC							
61		PB0	A8	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/RSPCKA	SDHI_C MD		
62	VSS							
63		PA7	A7	TIOCB2	MISOA			
64		PA6	A6	MTIC5V/MTCLKB/TMC13/POE2#/TIOCA2	CTS5#/RTS5#/SS5#/MOSIA/SSIWS0			
65		PA5	A5	TIOCB1	RSPCKA			
66		PA4	A4	MTIC5U/MTCLKA/TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5			IRQ5 / CVREFB1
67		PA3	A3	MTIOC0D/MTCLKD/TIOC0D/TCLKB	RXD5/SMISO5/SSCL5/SSIRXD0/IRRXD5			IRQ6 /CMPB1
68		PA2	A2		RXD5/SMISO5/SSCL5/SSLA3/IRRXD5			
69		PA1	A1	MTIOC0B/MTCLKC/TIOCB0	SCK5/SSLA2/SSISCK0			
70		PA0	A0/BC0#	MTIOC4A/TIOCA0	SSLA1			CACREF
71		PE7	D15[A15/D15]					IRQ7/AN023
72		PE6	D14[A14/D14]					IRQ6/AN022
73		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B				IRQ5/AN021/CMPOB0
74		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A				AN020/ CMPA2/ CLKOUT
75		PE3	D11[A11/D11]	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/AUDIO_MCLK			AN019/ CLKOUT
76		PE2	D10[A10/D10]	MTIOC4A	RXD12/RXDX12/SMISO12/SSCL12			IRQ7/AN018/ CVREFB0
77		PE1	D9[A9/D9]	MTIOC4C	TXD12/TXDX12/SIOX12/SMOSI12/SSDA12			AN017/ CMPB0
78		PE0	D8[A8/D8]		SCK12			AN016

Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
79		PD7	D7[A7/D7]	MTIC5U/POE0#				IRQ7/AN031
80		PD6	D6[A6/D6]	MTIC5V/POE1#				IRQ6/AN030
81		PD5	D5[A5/D5]	MTIC5W/POE2#				IRQ5/AN029
82		PD4	D4[A4/D4]	POE3#				IRQ4/AN028
83		PD3	D3[A3/D3]	POE8#				IRQ3/AN027
84		PD2	D2[A2/D2]	MTIOC4D				IRQ2/AN026
85		PD1	D1[A1/D1]	MTIOC4B				IRQ1/AN025
86		PD0	D0[A0/D0]					IRQ0/AN024
87		P47						AN007
88		P46						AN006
89		P45						AN005
90		P44						AN004
91		P43						AN003
92		P42						AN002
93		P41						AN001
94	VREFL0							
95		P40						AN000
96	VREFH0							
97	AVCC0							
98		P07						ADTRG0#
99	AVSS0							
100		P05						DA1

Note 1. RX230: PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, PH3/TMCI0
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Table 1.9 List of Pins and Pin Functions (64-Pin LFQFP/HWQFN) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, IIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
42		PA4	MTIC5U/MTCLKA/TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5			IRQ5 /CVREFB1
43		PA3	MTIOC0D/MTCLKD/TIOCD0/TCLKB	RXD5/SMISO5/SSCL5/SSIRXD0/IRRXD5			IRQ6 /CMPB1
44		PA1	MTIOC0B/MTCLKC/TIOCB0	SCK5/SSLA2/SSISCK0			
45		PA0	MTIOC4A/TIOCA0	SSLA1			CACREF
46		PE5	MTIOC4C/MTIOC2B				IRQ5/AN021/CMPOB0
47		PE4	MTIOC4D/MTIOC1A				AN020/CMPA2/CLKOUT
48		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/AUDIO_MCLK			AN019/CLKOUT
49		PE2	MTIOC4A	RXD12/RXD12/SMISO12/SSCL12			IRQ7/AN018/CVREFB0
50		PE1	MTIOC4C	TXD12/TXD12/SIOX12/SMOSI12/SSDA12			AN017/CMPB0
51		PE0		SCK12			AN016
52	VREFL						
53		P46					AN006
54	VREFH						
55		P44					AN004
56		P43					AN003
57		P42					AN002
58		P41					AN001
59	VREFL0						
60		P40					AN000
61	VREFH0						
62	AVCC0						
63		P05					DA1
64	AVSS0						

Note 1. RX230: PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, PH3/TMCIO
 RX231: VSS_USB, USB_DP, USB_DM, VCC_USB

(9) Floating-point status word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.

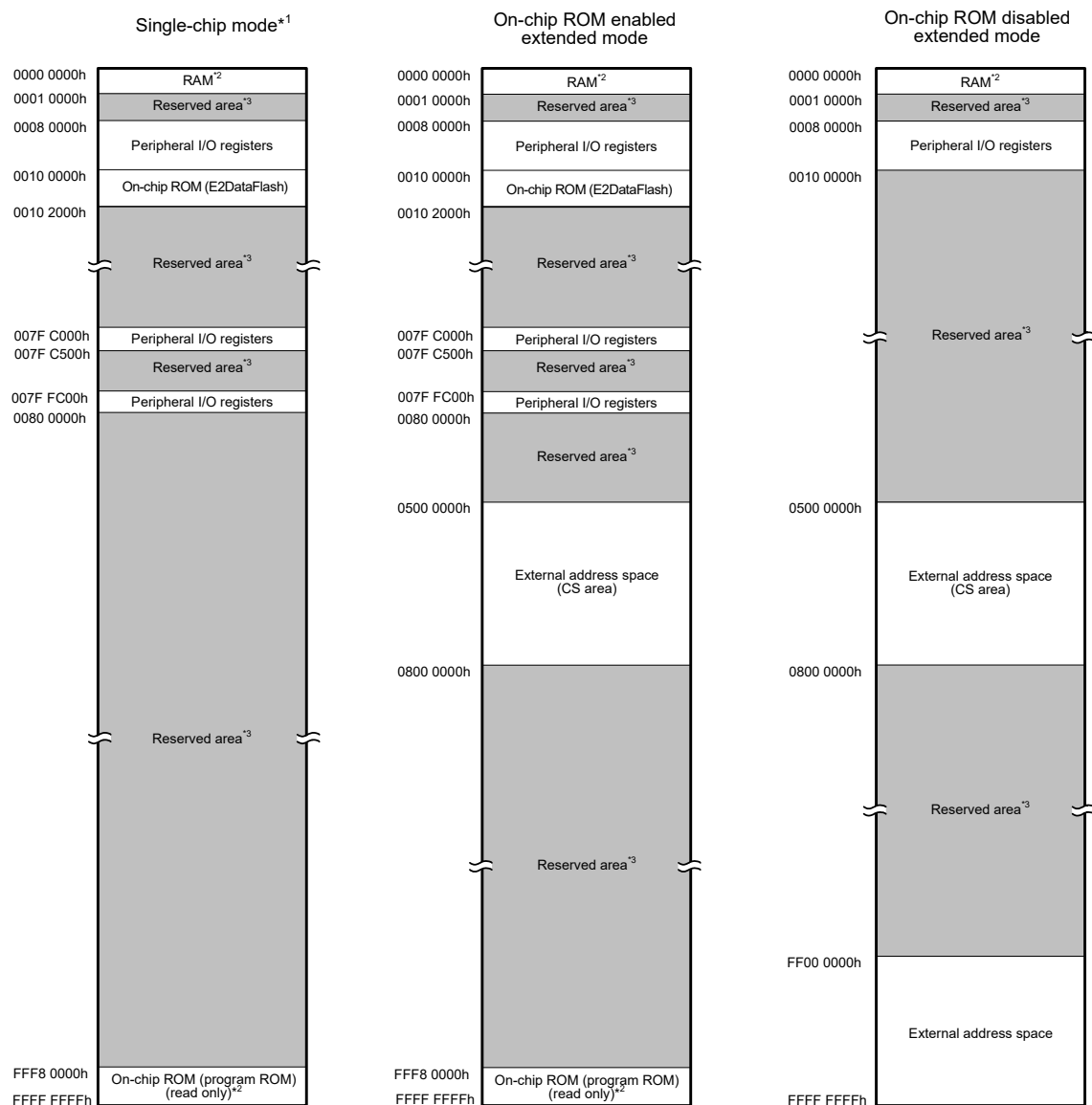
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

2.3 Accumulator

The accumulator (ACC0 or ACC1) is a 72-bit register used for DSP instructions. The accumulator is handled as a 96-bit register for reading and writing. At this time, when bits 95 to 72 of the accumulator are read, the value where the value of bit 71 is sign extended is read. Writing to bits 95 to 72 of the accumulator is ignored. ACC0 is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in ACC0 is modified by execution of the instruction.

Use the MVTACGU, MVTACHI, and MVTACLO instructions for writing to the accumulator. The MVTACGU, MVTACHI, and MVTACLO instructions write data to bits 95 to 64, the higher-order 32 bits (bits 63 to 32), and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions for reading data from the accumulator. The MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions read data from the guard bits (bits 95 to 64), higher-order 32 bits (bits 63 to 32), the middle 32 bits (bits 47 to 16), and the lower-order 32 bits (bits 31 to 0), respectively.



Note 1. The address space in boot mode and USB boot mode is the same as the address space in single-chip mode.

Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	Address	Capacity	Address
512 Kbytes	FFF8 0000h to FFFF FFFFh	64 Kbytes	0000 0000h to 0000 FFFFh
384 Kbytes	FFFA 0000h to FFFF FFFFh		
256 Kbytes	FFFC 0000h to FFFF FFFFh		
128 Kbytes	FFFE 0000h to FFFF FFFFh	32 Kbytes	0000 0000h to 0000 7FFFh

Note: See Table 1.3 and Table 1.4 List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map in Each Operating Mode

4. I/O Registers

This section provides information on the on-chip I/O register addresses and bit configuration. The information is given as shown below. Notes on writing to registers are also given below.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- Numbers of cycles for access indicate numbers of cycles of the given base clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.

As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERN of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

- Write to an I/O register.
- Read the value from the I/O register to a general register.
- Execute the operation using the value read.
- Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.B #SFR_DATA, [R1]
CMP [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.W #SFR_DATA, [R1]
CMP [R1].W, R1
;; Next process
```

Table 4.1 List of I/O Registers (Address Order) (7/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 or 3 PCLKB	2 ICLK
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 or 3 PCLKB	2 ICLK
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 or 3 PCLKB	2 ICLK
0008 8310h	RIIC0	I ² C-Bus Bit Rate Low-Level Register	ICBRL	8	8	2 or 3 PCLKB	2 ICLK
0008 8311h	RIIC0	I ² C-Bus Bit Rate High-Level Register	ICBRH	8	8	2 or 3 PCLKB	2 ICLK
0008 8312h	RIIC0	I ² C-Bus Transmit Data Register	ICDRT	8	8	2 or 3 PCLKB	2 ICLK
0008 8313h	RIIC0	I ² C-Bus Receive Data Register	ICDRR	8	8	2 or 3 PCLKB	2 ICLK
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2 or 3 PCLKB	2 ICLK
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2 or 3 PCLKB	2 ICLK
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2 or 3 PCLKB	2 ICLK
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2 or 3 PCLKB	2 ICLK
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2 or 3 PCLKB	2 ICLK
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2 or 3 PCLKB	2 ICLK
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 or 3 PCLKB	2 ICLK
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2 or 3 PCLKB	2 ICLK
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2 or 3 PCLKB	2 ICLK
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2 or 3 PCLKB	2 ICLK
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2 or 3 PCLKB	2 ICLK
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2 or 3 PCLKB	2 ICLK
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2 or 3 PCLKB	2 ICLK
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2 or 3 PCLKB	2 ICLK
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2 or 3 PCLKB	2 ICLK
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2 or 3 PCLKB	2 ICLK
0008 8410h	IRDA	IrDA Control Register	IRCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8900h	POE	Input Level Control/Status Register 1	ICSR1	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 8902h	POE	Output Level Control/Status Register 1	OCSR1	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 8908h	POE	Input Level Control/Status Register 2	ICSR2	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 890Ah	POE	Software Port Output Enable Register	SPOER	8	8	2 or 3 PCLKB	2 ICLK
0008 890Bh	POE	Port Output Enable Control Register 1	POECR1	8	8	2 or 3 PCLKB	2 ICLK
0008 890Ch	POE	Port Output Enable Control Register 2	POECR2	8	8	2 or 3 PCLKB	2 ICLK
0008 890Eh	POE	Input Level Control/Status Register 3	ICSR3	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB	2 ICLK
0008 9004h	S12AD	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB	2 ICLK
0008 9006h	S12AD	A/D Channel Select Register A1	ADANSA1	16	16	2 or 3 PCLKB	2 ICLK
0008 9008h	S12AD	A/D-Converted Value Addition/Average Function Select Register 0	ADADS0	16	16	2 or 3 PCLKB	2 ICLK
0008 900Ah	S12AD	A/D-Converted Value Addition/Average Function Select Register 1	ADADS1	16	16	2 or 3 PCLKB	2 ICLK
0008 900Ch	S12AD	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB	2 ICLK
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB	2 ICLK
0008 9010h	S12AD	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB	2 ICLK
0008 9012h	S12AD	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB	2 ICLK
0008 9014h	S12AD	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB	2 ICLK
0008 9016h	S12AD	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB	2 ICLK
0008 9018h	S12AD	A/D Data Duplication Register	ADBLDR	16	16	2 or 3 PCLKB	2 ICLK
0008 901Ah	S12AD	A/D Temperature Sensor Data Register	ADTSR	16	16	2 or 3 PCLKB	2 ICLK
0008 901Ch	S12AD	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (23/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 00B0h	USB0	BC Control Register 0	USBBCCTRL0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00CCh	USB0	USB Module Control Register	USBMC	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D0h	USB0	Device Address 0 Configuration Register	DEVADD0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D2h	USB0	Device Address 1 Configuration Register	DEVADD1	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D4h	USB0	Device Address 2 Configuration Register	DEVADD2	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D6h	USB0	Device Address 3 Configuration Register	DEVADD3	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D8h	USB0	Device Address 4 Configuration Register	DEVADD4	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00DAh	USB0	Device Address 5 Configuration Register	DEVADD5	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 0900h	CTSU	CTSU Control Register 0	CTSUCR0	8	8	2 or 3 PCLKB	2 ICLK
000A 0901h	CTSU	CTSU Control Register 1	CTSUCR1	8	8	2 or 3 PCLKB	2 ICLK
000A 0902h	CTSU	CTSU Synchronous Noise Reduction Setting Register	CTSUSDPRS	8	8	2 or 3 PCLKB	2 ICLK
000A 0903h	CTSU	CTSU Sensor Stabilization Wait Control Register	CTSUSST	8	8	2 or 3 PCLKB	2 ICLK
000A 0904h	CTSU	CTSU Measurement Channel Register 0	CTSUMCH0	8	8	2 or 3 PCLKB	2 ICLK
000A 0905h	CTSU	CTSU Measurement Channel Register 1	CTSUMCH1	8	8	2 or 3 PCLKB	2 ICLK
000A 0906h	CTSU	CTSU Channel Enable Control Register 0	CTSUCHAC0	8	8	2 or 3 PCLKB	2 ICLK
000A 0907h	CTSU	CTSU Channel Enable Control Register 1	CTSUCHAC1	8	8	2 or 3 PCLKB	2 ICLK
000A 0908h	CTSU	CTSU Channel Enable Control Register 2	CTSUCHAC2	8	8	2 or 3 PCLKB	2 ICLK
000A 0909h	CTSU	CTSU Channel Enable Control Register 3	CTSUCHAC3	8	8	2 or 3 PCLKB	2 ICLK
000A 090Ah	CTSU	CTSU Channel Enable Control Register 4	CTSUCHAC4	8	8	2 or 3 PCLKB	2 ICLK
000A 090Bh	CTSU	CTSU Channel Transmit/Receive Control Register 0	CTSUCHTRC0	8	8	2 or 3 PCLKB	2 ICLK
000A 090Ch	CTSU	CTSU Channel Transmit/Receive Control Register 1	CTSUCHTRC1	8	8	2 or 3 PCLKB	2 ICLK
000A 090Dh	CTSU	CTSU Channel Transmit/Receive Control Register 2	CTSUCHTRC2	8	8	2 or 3 PCLKB	2 ICLK
000A 090Eh	CTSU	CTSU Channel Transmit/Receive Control Register 3	CTSUCHTRC3	8	8	2 or 3 PCLKB	2 ICLK
000A 090Fh	CTSU	CTSU Channel Transmit/Receive Control Register 4	CTSUCHTRC4	8	8	2 or 3 PCLKB	2 ICLK
000A 0910h	CTSU	CTSU High-Pass Noise Reduction Control Register	CTSUDCLKC	8	8	2 or 3 PCLKB	2 ICLK
000A 0911h	CTSU	CTSU Status Register	CTSUST	8	8	2 or 3 PCLKB	2 ICLK
000A 0912h	CTSU	CTSU High-Pass Noise Reduction Spectrum Diffusion Control Register	CTSUSSC	16	16	2 or 3 PCLKB	2 ICLK
000A 0914h	CTSU	CTSU Sensor Offset Register 0	CTSUSO0	16	16	2 or 3 PCLKB	2 ICLK
000A 0916h	CTSU	CTSU Sensor Offset Register 1	CTSUSO1	16	16	2 or 3 PCLKB	2 ICLK
000A 0918h	CTSU	CTSU Sensor Counter	CTSUSC	16	16	2 or 3 PCLKB	2 ICLK
000A 091Ah	CTSU	CTSU Reference Counter	CTSURC	16	16	2 or 3 PCLKB	2 ICLK
000A 091Ch	CTSU	CTSU Error Status Register	CTSUERRS	16	16	2 or 3 PCLKB	2 ICLK
000A 8300h	RSCAN0	Bit Configuration Register L	CFGL	16	16	2 or 3 PCLKB	2 ICLK
000A 8302h	RSCAN0	Bit Configuration Register H	CFGH	16	16	2 or 3 PCLKB	2 ICLK
000A 8304h	RSCAN0	Control Register L	CTRL	16	16	2 or 3 PCLKB	2 ICLK
000A 8306h	RSCAN0	Control Register H	CTRH	16	16	2 or 3 PCLKB	2 ICLK
000A 8308h	RSCAN0	Status Register L	STSL	16	16	2 or 3 PCLKB	2 ICLK
000A 830Ah	RSCAN0	Status Register H	STSH	16	16	2 or 3 PCLKB	2 ICLK
000A 830Ch	RSCAN0	Error Flag Register L	ERFLL	16	16	2 or 3 PCLKB	2 ICLK
000A 830Eh	RSCAN0	Error Flag Register H	ERFLH	16	16	2 or 3 PCLKB	2 ICLK
000A 8322h	RSCAN	Global Configuration Register L	GCFGFL	16	16	2 or 3 PCLKB	2 ICLK
000A 8324h	RSCAN	Global Configuration Register H	GCFGH	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (29/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 8494h	RSCAN	Receive Buffer Register 15BL	RMTS15	16	16	2 or 3 PCLKB	2 ICLK
000A 8496h	RSCAN	Receive Buffer Register 15BH	RMPTR15	16	16	2 or 3 PCLKB	2 ICLK
000A 8498h	RSCAN	Receive Buffer Register 15CL	RMDF015	16	16	2 or 3 PCLKB	2 ICLK
000A 849Ah	RSCAN	Receive Buffer Register 15CH	RMDF115	16	16	2 or 3 PCLKB	2 ICLK
000A 849Ch	RSCAN	Receive Buffer Register 15DL	RMDF215	16	16	2 or 3 PCLKB	2 ICLK
000A 849Eh	RSCAN	Receive Buffer Register 15DH	RMDF315	16	16	2 or 3 PCLKB	2 ICLK
000A 8580h to 000A 859Fh	RSCAN	RAM Test Register 0 to RAM Test Register 15	RPGACC0 to RPGACC15	16	16	2 or 3 PCLKB	2 ICLK
000A 85A0h	RSCAN	Receive FIFO Access Register 0AL	RFIDL0	16	16	2 or 3 PCLKB	2 ICLK
000A 85A0h	RSCAN	RAM Test Register 16	RPGACC16	16	16	2 or 3 PCLKB	2 ICLK
000A 85A2h	RSCAN	Receive FIFO Access Register 0AH	RFIDH0	16	16	2 or 3 PCLKB	2 ICLK
000A 85A2h	RSCAN	RAM Test Register 17	RPGACC17	16	16	2 or 3 PCLKB	2 ICLK
000A 85A4h	RSCAN	Receive FIFO Access Register 0BL	RFTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 85A4h	RSCAN	RAM Test Register 18	RPGACC18	16	16	2 or 3 PCLKB	2 ICLK
000A 85A6h	RSCAN	Receive FIFO Access Register 0BH	RFPTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 85A6h	RSCAN	RAM Test Register 19	RPGACC19	16	16	2 or 3 PCLKB	2 ICLK
000A 85A8h	RSCAN	Receive FIFO Access Register 0CL	RFDF00	16	16	2 or 3 PCLKB	2 ICLK
000A 85A8h	RSCAN	RAM Test Register 20	RPGACC20	16	16	2 or 3 PCLKB	2 ICLK
000A 85AAh	RSCAN	Receive FIFO Access Register 0CH	RFDF10	16	16	2 or 3 PCLKB	2 ICLK
000A 85AAh	RSCAN	RAM Test Register 21	RPGACC21	16	16	2 or 3 PCLKB	2 ICLK
000A 85ACh	RSCAN	Receive FIFO Access Register 0DL	RFDF20	16	16	2 or 3 PCLKB	2 ICLK
000A 85ACh	RSCAN	RAM Test Register 22	RPGACC22	16	16	2 or 3 PCLKB	2 ICLK
000A 85AEh	RSCAN	Receive FIFO Access Register 0DH	RFDF30	16	16	2 or 3 PCLKB	2 ICLK
000A 85AEh	RSCAN	RAM Test Register 23	RPGACC23	16	16	2 or 3 PCLKB	2 ICLK
000A 85B0h	RSCAN	Receive FIFO Access Register 1AL	RFIDL1	16	16	2 or 3 PCLKB	2 ICLK
000A 85B0h	RSCAN	RAM Test Register 24	RPGACC24	16	16	2 or 3 PCLKB	2 ICLK
000A 85B2h	RSCAN	Receive FIFO Access Register 1AH	RFIDH1	16	16	2 or 3 PCLKB	2 ICLK
000A 85B2h	RSCAN	RAM Test Register 25	RPGACC25	16	16	2 or 3 PCLKB	2 ICLK
000A 85B4h	RSCAN	Receive FIFO Access Register 1BL	RFTS1	16	16	2 or 3 PCLKB	2 ICLK
000A 85B4h	RSCAN	RAM Test Register 26	RPGACC26	16	16	2 or 3 PCLKB	2 ICLK
000A 85B6h	RSCAN	Receive FIFO Access Register 1BH	RFPTR1	16	16	2 or 3 PCLKB	2 ICLK
000A 85B6h	RSCAN	RAM Test Register 27	RPGACC27	16	16	2 or 3 PCLKB	2 ICLK
000A 85B8h	RSCAN	Receive FIFO Access Register 1CL	RFDF01	16	16	2 or 3 PCLKB	2 ICLK
000A 85B8h	RSCAN	RAM Test Register 28	RPGACC28	16	16	2 or 3 PCLKB	2 ICLK
000A 85BAh	RSCAN	Receive FIFO Access Register 1CH	RFDF11	16	16	2 or 3 PCLKB	2 ICLK
000A 85BAh	RSCAN	RAM Test Register 29	RPGACC29	16	16	2 or 3 PCLKB	2 ICLK
000A 85BCh	RSCAN	Receive FIFO Access Register 1DL	RFDF21	16	16	2 or 3 PCLKB	2 ICLK
000A 85BCh	RSCAN	RAM Test Register 30	RPGACC30	16	16	2 or 3 PCLKB	2 ICLK
000A 85BEh	RSCAN	Receive FIFO Access Register 1DH	RFDF31	16	16	2 or 3 PCLKB	2 ICLK
000A 85BEh	RSCAN	RAM Test Register 31	RPGACC31	16	16	2 or 3 PCLKB	2 ICLK
000A 85C0h to 000A 85DEh	RSCAN	RAM Test Register 32 to RAM Test Register 47	RPGACC32 to RPGACC47	16	16	2 or 3 PCLKB	2 ICLK
000A 85E0h	RSCAN0	Transmit/Receive FIFO Access Register 0AL	CFIDL0	16	16	2 or 3 PCLKB	2 ICLK
000A 85E0h	RSCAN	RAM Test Register 48	RPGACC48	16	16	2 or 3 PCLKB	2 ICLK
000A 85E2h	RSCAN0	Transmit/Receive FIFO Access Register 0AH	CFIDH0	16	16	2 or 3 PCLKB	2 ICLK
000A 85E2h	RSCAN	RAM Test Register 49	RPGACC49	16	16	2 or 3 PCLKB	2 ICLK
000A 85E4h	RSCAN0	Transmit/Receive FIFO Access Register 0BL	CFTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 85E4h	RSCAN	RAM Test Register 50	RPGACC50	16	16	2 or 3 PCLKB	2 ICLK
000A 85E6h	RSCAN0	Transmit/Receive FIFO Access Register 0BH	CFPTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 85E6h	RSCAN	RAM Test Register 51	RPGACC51	16	16	2 or 3 PCLKB	2 ICLK
000A 85E8h	RSCAN0	Transmit/Receive FIFO Access Register 0CL	CFDF00	16	16	2 or 3 PCLKB	2 ICLK
000A 85E8h	RSCAN	RAM Test Register 52	RPGACC52	16	16	2 or 3 PCLKB	2 ICLK

5.2.3 Normal I/O Pin Output Characteristics (3)

Figure 5.18 to Figure 5.21 show the characteristics of the RIIC output pin.

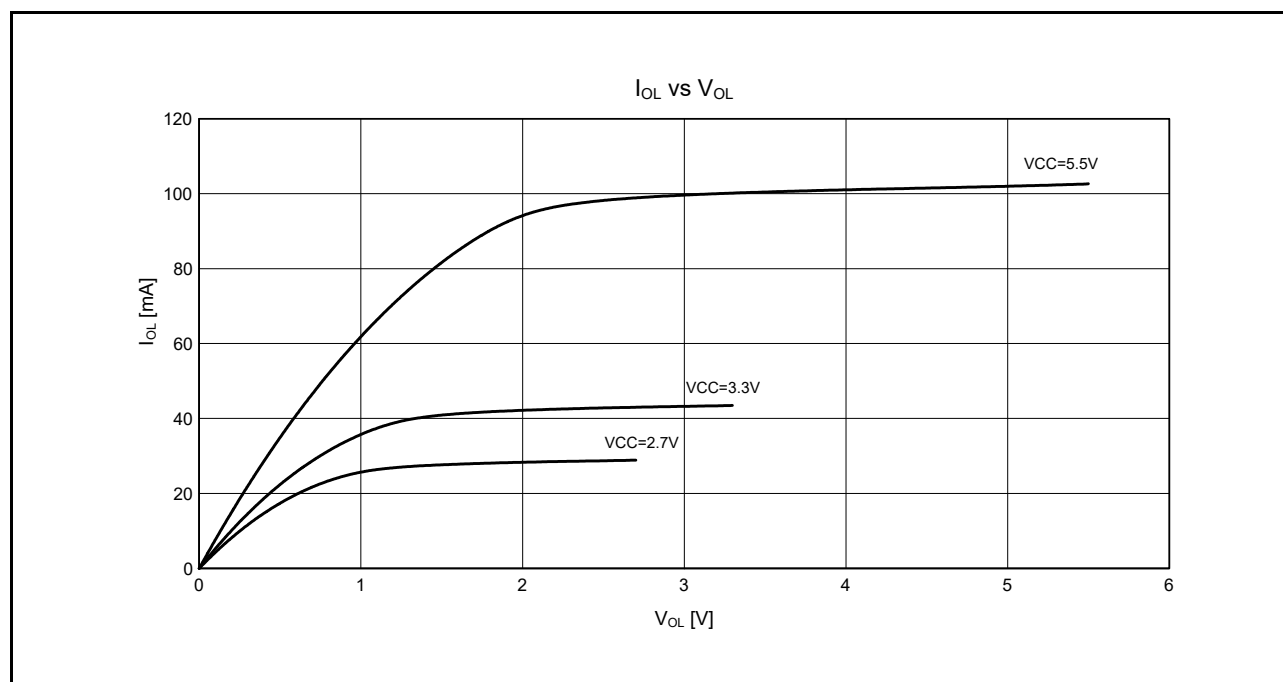


Figure 5.18 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at T_a = 25°C (Reference Data)

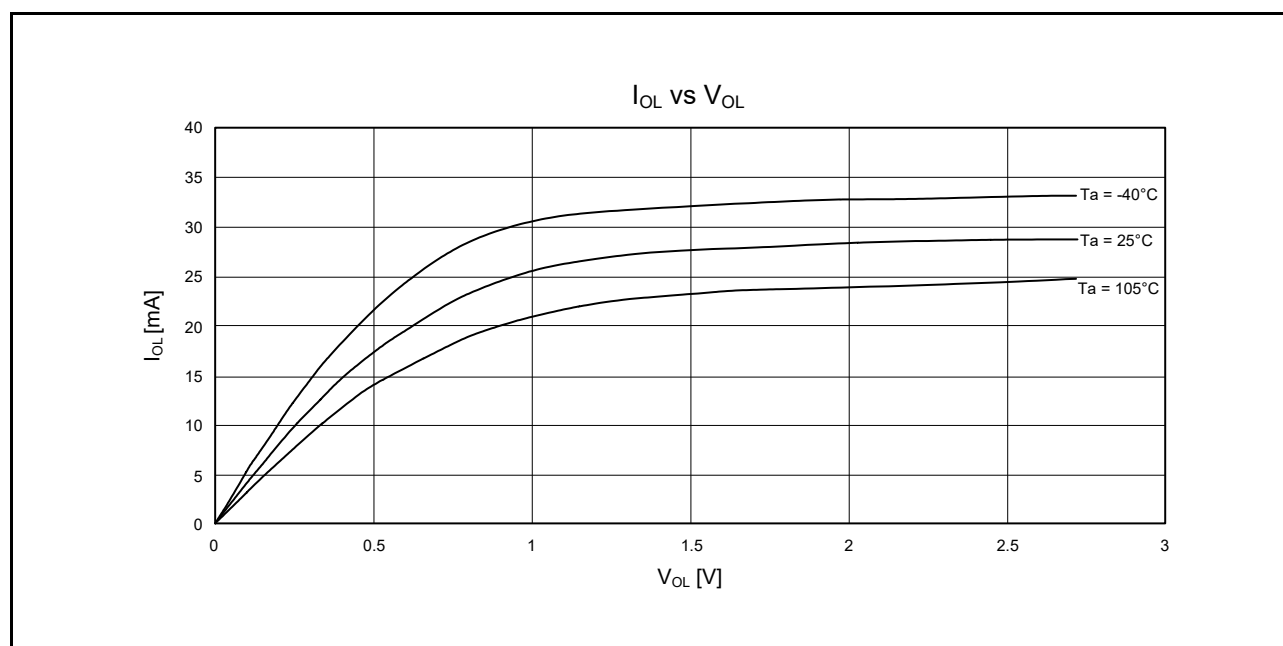


Figure 5.19 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)

5.3.2 Reset Timing

Table 5.27 Reset Timing

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VREFL0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

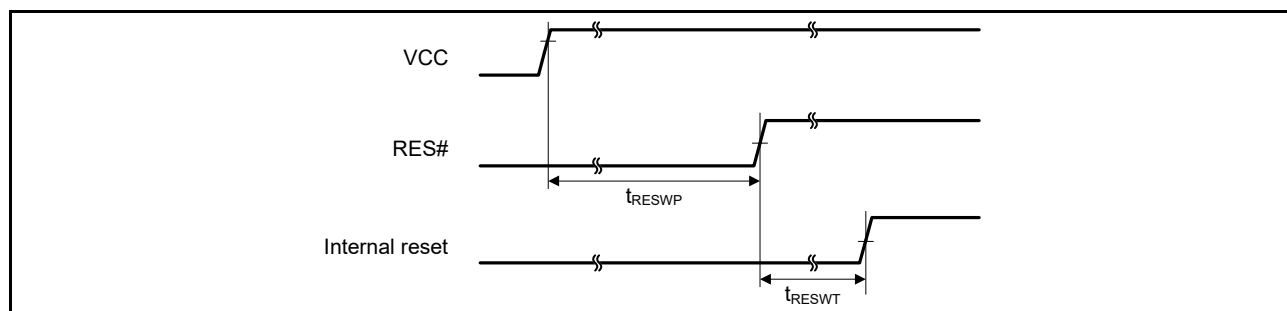
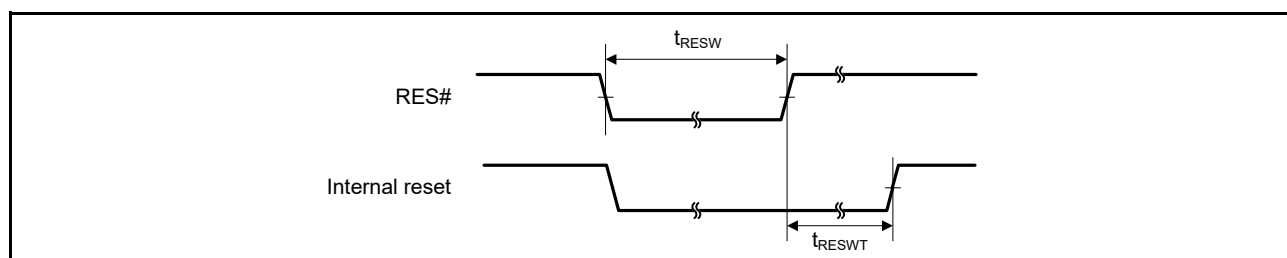
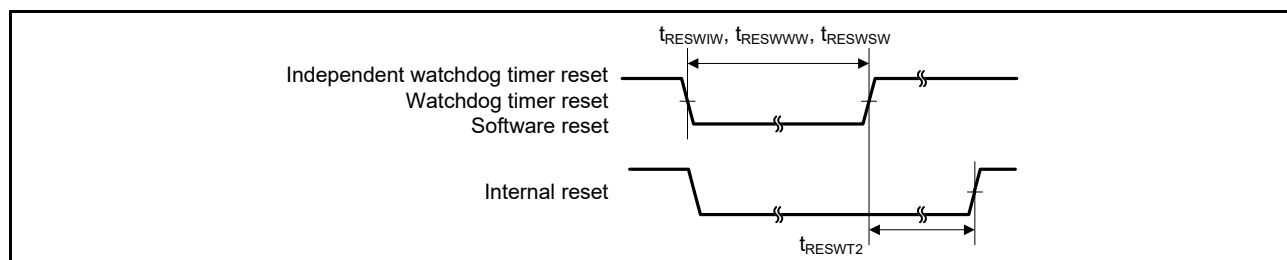
Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t_{RESWP}	3	—	—	ms	Figure 5.31
	Other than above	t_{RESW}	30	—	—	μs	Figure 5.32
Wait time after RES# cancellation (at power-on)	At normal startup*1	t_{RESWT}	—	8.5	—	ms	Figure 5.31
	During fast startup time*2	t_{RESWT}	—	560	—	μs	
Wait time after RES# cancellation (during powered-on state)		t_{RESWT}	—	120	—	μs	Figure 5.32
Independent watchdog timer reset period		t_{RESWIW}	—	1	—	IWDTC clock cycle	Figure 5.33
Watchdog timer reset period		t_{RESWWW}	—	4	—	PCLKB cycle	
Software reset period		t_{RESWSW}	—	1	—	ICLK cycle	
Wait time after independent watchdog timer reset cancellation*3		t_{RESWT2}	—	300	—	μs	
Wait time after watchdog timer reset cancellation*4		t_{RESWT2}	—	300	—	μs	
Wait time after software reset cancellation		t_{RESWT2}	—	170	—	μs	

Note 1. When OFS1.(LVDAS, FASTSTUP) bits are 11b.

Note 2. When OFS1.(LVDAS, FASTSTUP) bits are a value other than 11b.

Note 3. When IWDTCR.CKS[3:0] bits are 0000b.

Note 4. When WDTTCR.CKS[3:0] bits are 0001b.

**Figure 5.31 Reset Input Timing at Power-On****Figure 5.32 Reset Input Timing (1)****Figure 5.33 Reset Input Timing (2)**

5.3.4 Control Signal Timing

Table 5.33 Control Signal Timing

Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

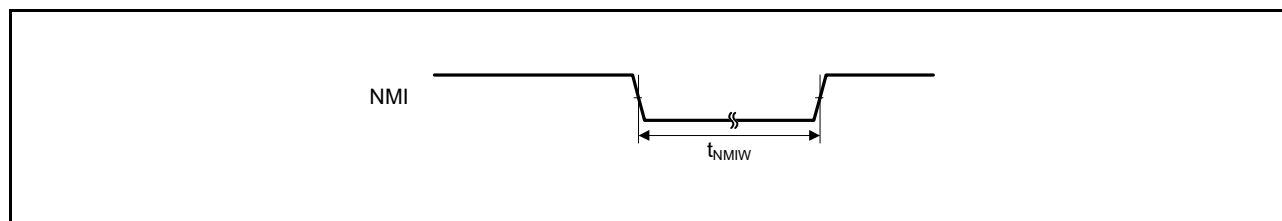
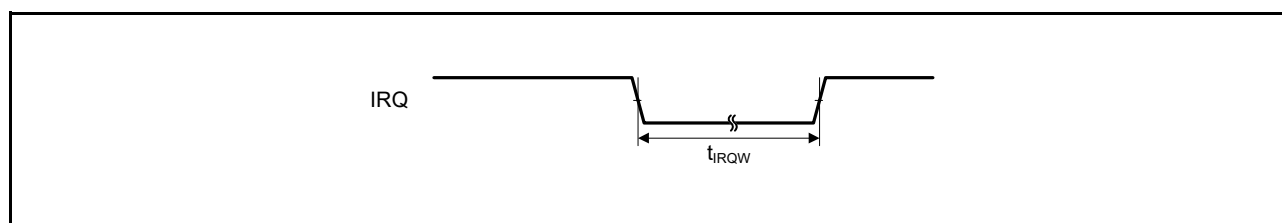
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter is disabled (NMIFLTE.NFLTEN = 0)	$t_{Pcyc} \times 2 \leq 200\text{ ns}$
		$t_{Pcyc} \times 2^{*1}$	—	—			$t_{Pcyc} \times 2 > 200\text{ ns}$
		200	—	—		NMI digital filter is enabled (NMIFLTE.NFLTEN = 1)	$t_{NMICK} \times 3 \leq 200\text{ ns}$
		$t_{NMICK} \times 3.5^{*2}$	—	—			$t_{NMICK} \times 3 > 200\text{ ns}$
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter is disabled (IRQFLTE0.FLTENi = 0)	$t_{Pcyc} \times 2 \leq 200\text{ ns}$
		$t_{Pcyc} \times 2^{*1}$	—	—			$t_{Pcyc} \times 2 > 200\text{ ns}$
		200	—	—		IRQ digital filter is enabled (IRQFLTE0.FLTENi = 1)	$t_{IRQCK} \times 3 \leq 200\text{ ns}$
		$t_{IRQCK} \times 3.5^{*3}$	—	—			$t_{IRQCK} \times 3 > 200\text{ ns}$

Note: 200 ns minimum in software standby mode.

Note 1. t_{Pcyc} indicates the cycle of PCLKB.

Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.

Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

**Figure 5.36 NMI Interrupt Input Timing****Figure 5.37 IRQ Interrupt Input Timing**

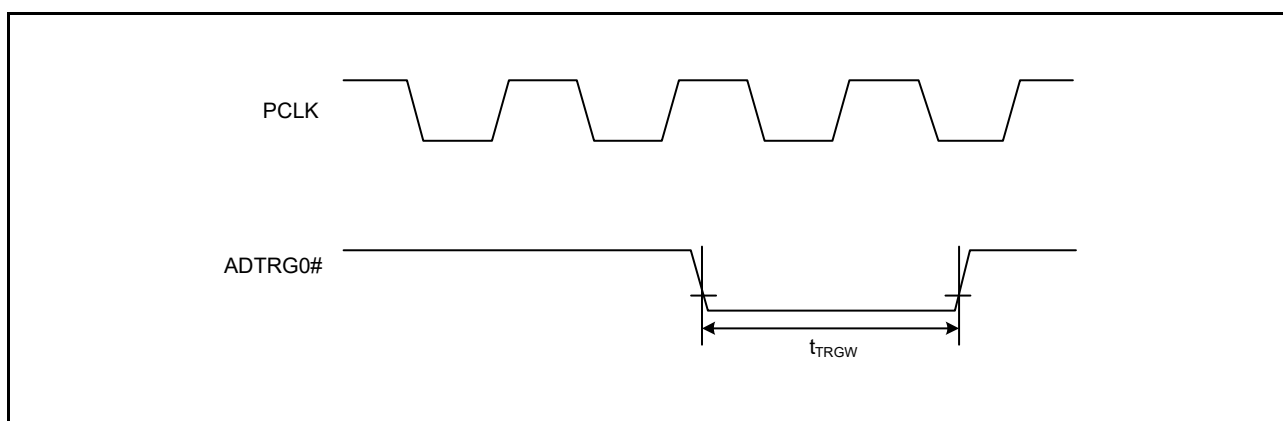


Figure 5.52 A/D Converter External Trigger Input Timing

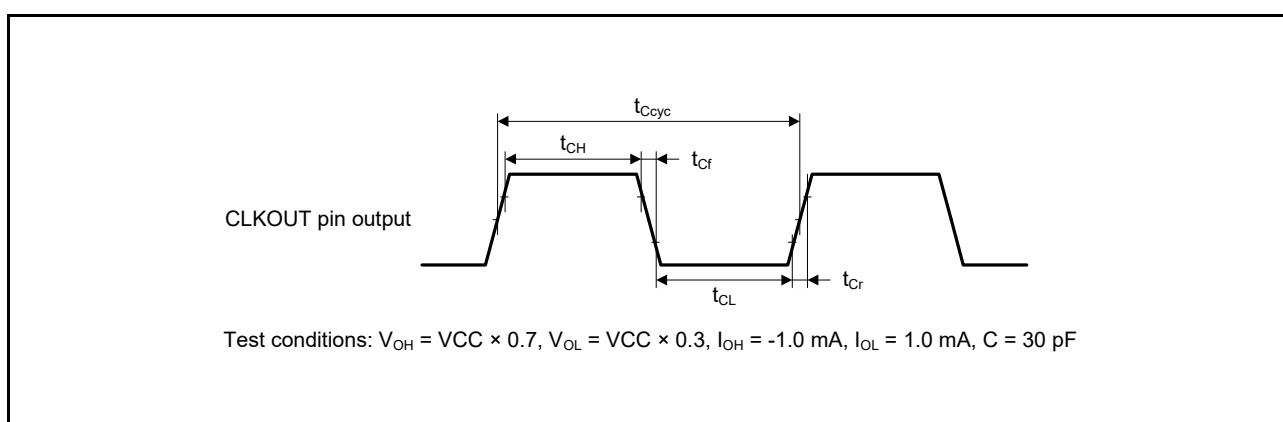


Figure 5.53 CLKOUT Output Timing

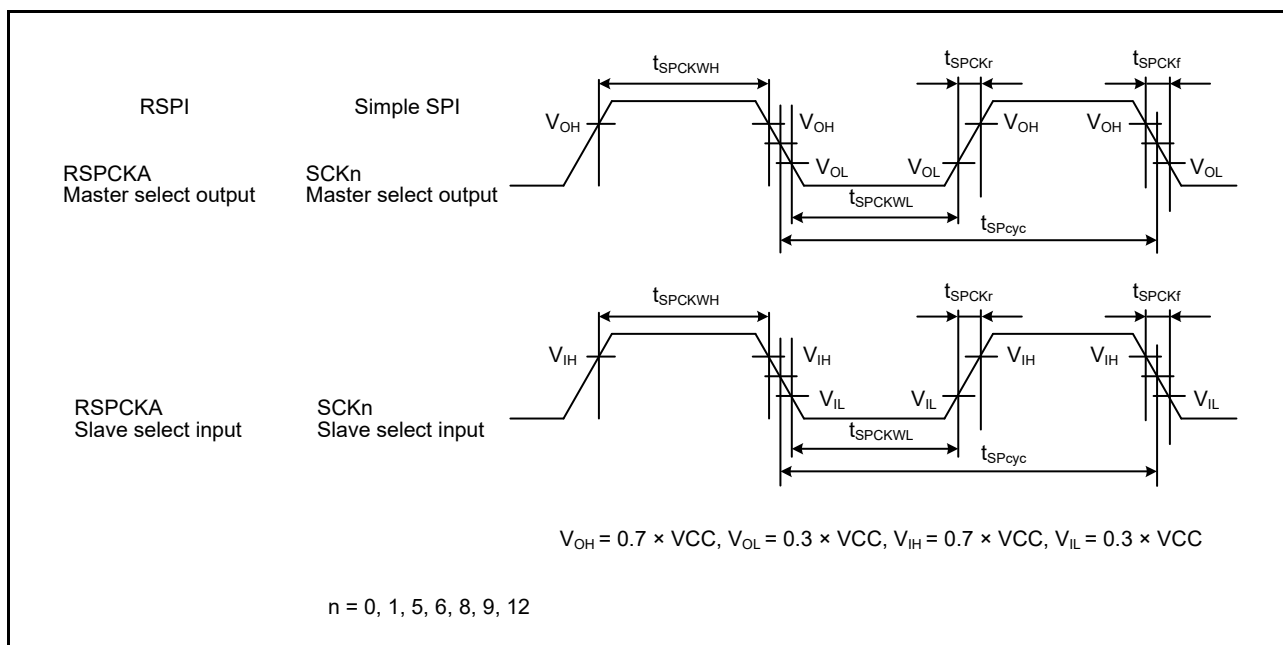


Figure 5.54 RSPI Clock Timing and Simple SPI Clock Timing

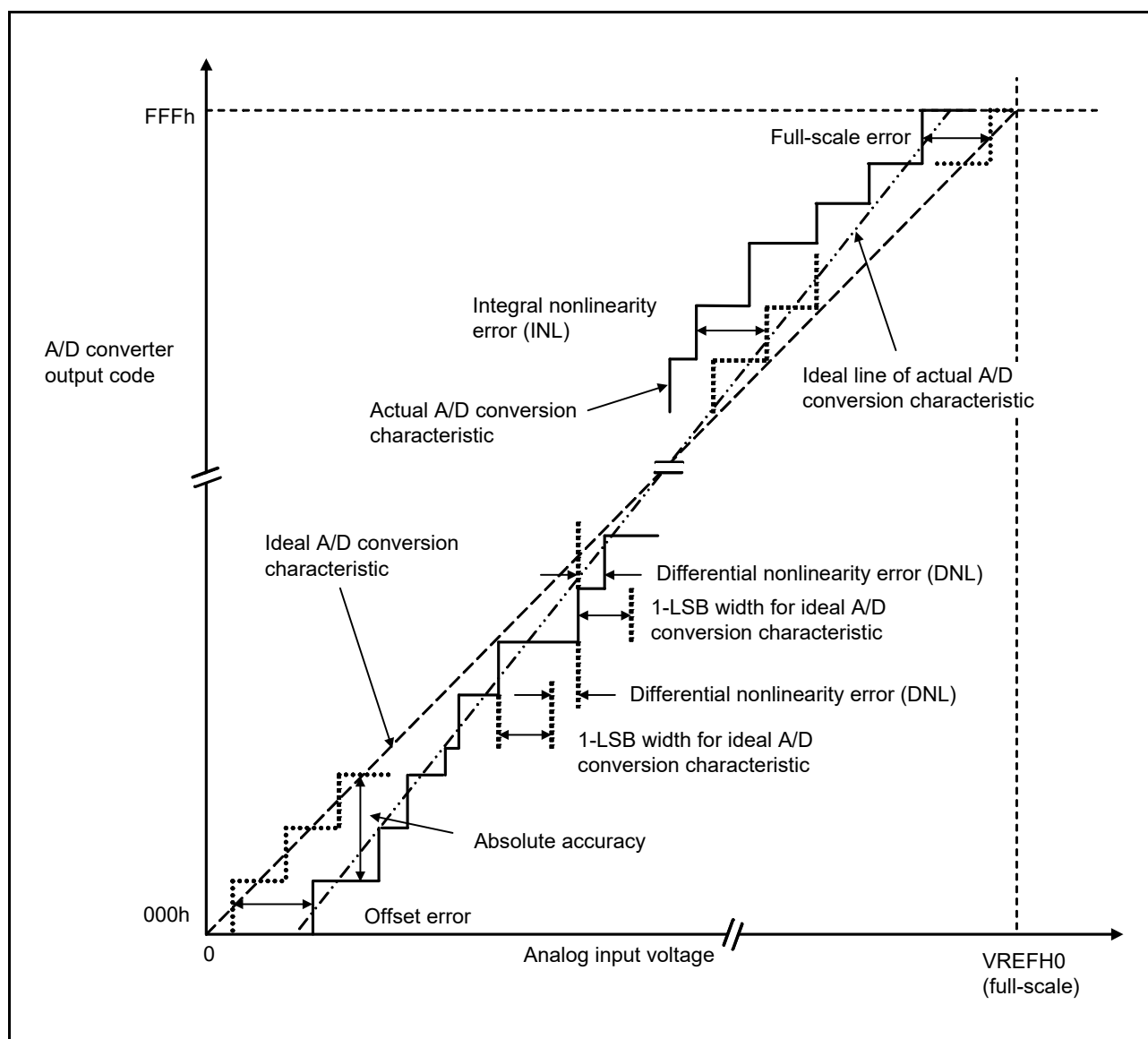


Figure 5.69 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage ($V_{REFH0} = 3.072 \text{ V}$), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = $\pm 5 \text{ LSB}$ means that the actual A/D conversion result is in the range of 003h to 00Dh, although an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral non-linearity error (INL)

The integral non-linearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Table 5.64 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating ModeConditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$ Temperature range for the programming/erasure operation: $T_a = -40$ to $+85^\circ\text{C}$

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8-byte	t_{P8}	—	152	1367	—	97.9	936	μs
Erasure time	2-Kbyte	t_{E2K}	—	8.8	279.7	—	5.9	221	ms
	512-Kbyte (when block erase command is used)	t_{E512K}	—	928	19221	—	191	4108	ms
	512-Kbyte (when all-block erase command is used)	t_{EA512K}	—	923	19015	—	185	3901	ms
Blank check time	8-byte	t_{BC8}	—	—	85.0	—	—	50.88	μs
	2-Kbyte	t_{BC2K}	—	—	1870	—	—	402	μs
Erase operation forced stop time		t_{SED}	—	—	28.0	—	—	21.3	μs
Start-up area switching setting time		t_{SAS}	—	13.0	573.3	—	7.7	451	ms
Access window time		t_{AWS}	—	13.0	573.3	—	7.7	451	ms
ROM mode transition wait time 1		t_{DIS}	2.0	—	—	2.0	—	—	μs
ROM mode transition wait time 2		t_{MS}	3.0	—	—	3.0	—	—	μs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be within $\pm 3.5\%$.

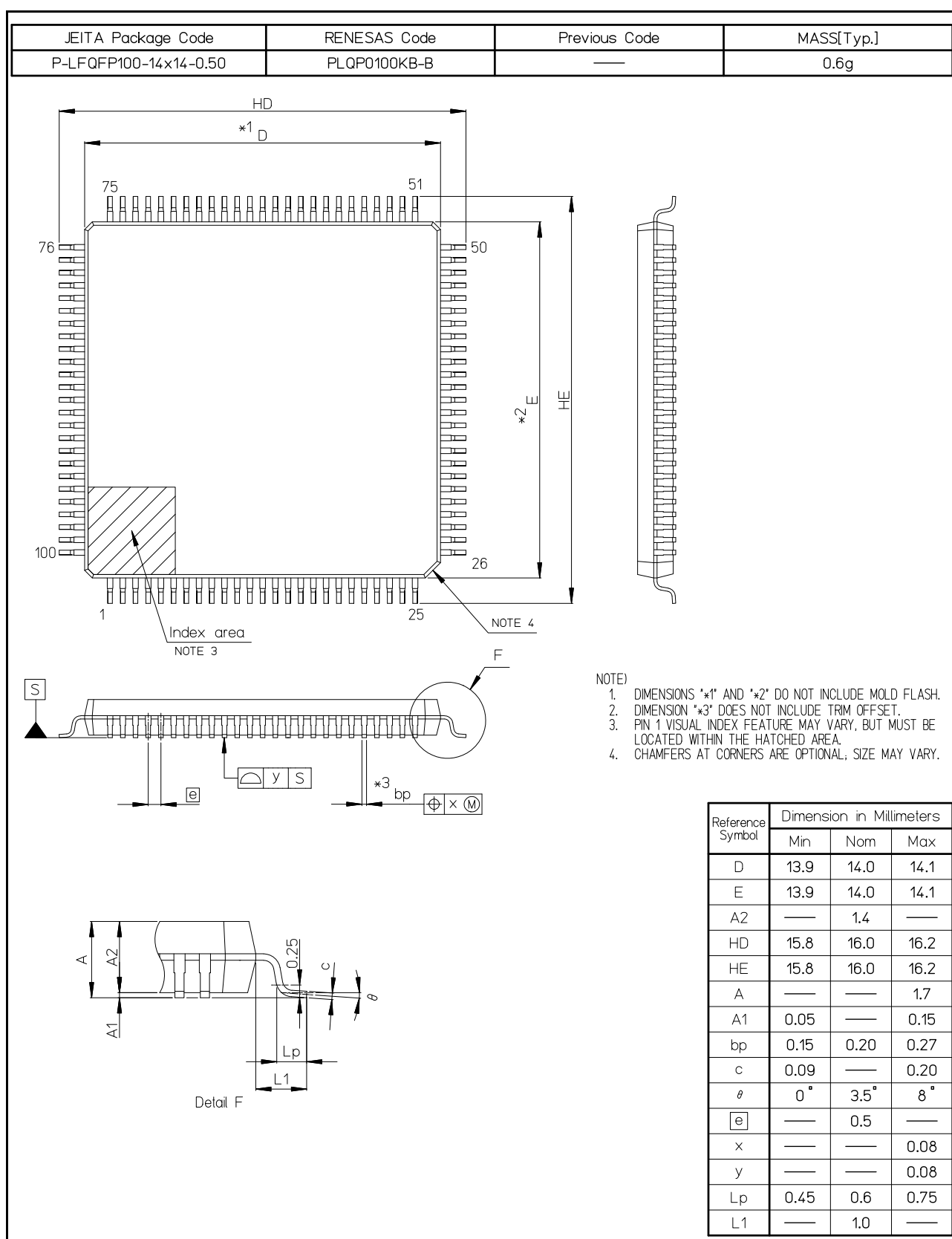


Figure B 100-Pin LFQFP (PLQP0100KB-B)

REVISION HISTORY	RX230 Group, RX231 Group Datasheet
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Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Jun 24, 2015	—	First edition, issued	
1.10	Oct 30, 2015	1. Overview		
		3	Table 1.1 Outline of Specifications (2/4), changed	
		5	Table 1.1 Outline of Specifications (4/4): SD Host Interface (SDH1a) added	
		6	Table 1.2 Comparison of Functions for Different Packages: RX230 Group added	
		3. Address Space		
		39	Figure 3.1 Memory Map in Each Operating Mode, changed	
		4. I/O Registers		
		67	Table 4.1 List of I/O Registers (Address Order) (25 / 42), changed	TN-RX*-A139A/E
		83	Table 4.1 List of I/O Registers (Address Order) (41 / 42), changed	
		5. Electrical Characteristics		
		85	Table 5.1 Absolute Maximum Ratings, changed	TN-RX*-A137A/E
		86	Table 5.2 Recommended Operating Voltage Conditions, changed	
		87	Table 5.3 DC Characteristics (1), changed	TN-RX*-A137A/E
		88	Table 5.4 DC Characteristics (2), changed	
		88	Table 5.5 DC Characteristics (3), changed	
		89	Table 5.7 DC Characteristics (5), changed	
		91	Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data), changed	
		92	Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data), changed	
		93	Figure 5.3 Voltage Dependency in Low-Speed Operating Mode (Reference Data), changed	TN-RX*-A137A/E
		94	Table 5.8 DC Characteristics (6), changed Figure 5.4 Voltage Dependency in Software Standby Mode (Reference Data), changed	
		95	Figure 5.5 Temperature Dependency in Software Standby Mode (Reference Data), changed	
		96	Figure 5.6 Temperature Dependency of RTC Operation with VCC Off (Reference Data), changed Table 5.10 DC Characteristics (8): Conditions changed	
		97	Table 5.11 DC Characteristics (9), changed	TN-RX*-A137A/E
		99	Table 5.16 Permissible Output Currents (1), changed	TN-RX*-A137A/E
		100	Table 5.17 Permissible Output Currents (2), changed	
		101	Table 5.18 Output Values of Voltage (1), changed	
		101	Table 5.19 Output Values of Voltage (2), changed	TN-RX*-A137A/E
		101	Table 5.20 Output Values of Voltage (3), changed	TN-RX*-A137A/E
		105	Figure 5.13 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C When High-Drive Output is Selected (Reference Data), changed	TN-RX*-A137A/E
		108	Figure 5.18 VOL and IOL Voltage Characteristics of RIIC Output Pin at Ta = 25°C (Reference Data)	TN-RX*-A137A/E
		110	Table 5.21 Operating Frequency Value (High-Speed Operating Mode) and Table 5.22 Operating Frequency Value (Middle-Speed Operating Mode), changed	TN-RX*-A137A/E
		112	Table 5.26 Clock Timing, changed	TN-RX*-A137A/E
		116	Table 5.27 Reset Timing, changed	
		131	Table 5.41 Timing of On-Chip Peripheral Modules (4): Note changed	
		132	Table 5.43 Timing of On-Chip Peripheral Modules (6), changed	
		138	Figure 5.61 SSI Transmission/Reception Timing (SSICP.SCKP=0), changed	TN-RX*-A137A/E
		139	Figure 5.62 SSI Transmission/Reception Timing (SSICP.SCKP=1), changed	TN-RX*-A137A/E
		142	Figure 5.66 VREFH0 Voltage Range vs. AVCC0, changed	

Rev.	Date	Description		Classification
		Page	Summary	
1.20	Sep 28, 2018	95	Figure 5.12 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 5.5 V When Normal Output is Selected (Reference Data), changed	TN-RX*-A201A/E
		124	Table 5.44 Timing of On-Chip Peripheral Modules (7), added	TN-RX*-A197A/E
		131	Figure 5.64 SD Host Interface Input/Output Signal Timing, added	TN-RX*-A197A/E
		132	Table 5.45 USB Characteristics (USB0_DP and USB0_DM Pin Characteristics) conditions, changed	

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NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.