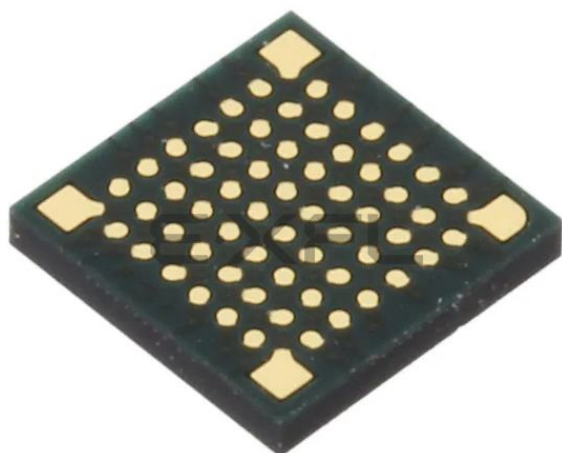




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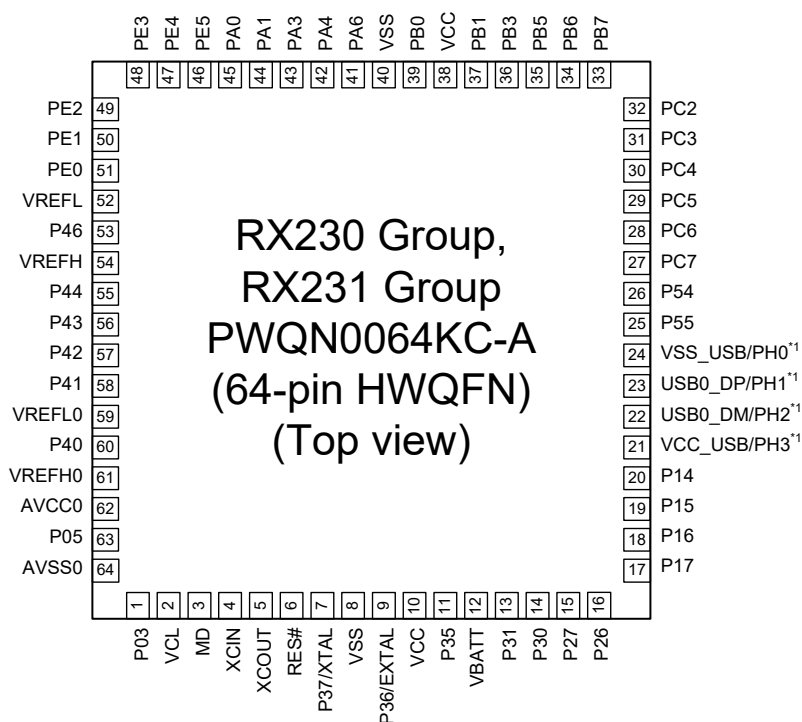
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Details

Product Status	Not For New Designs
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	I ² C, IrDA, SCI, SPI, SSI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	47
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFLGA
Supplier Device Package	64-FLGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52305adlf-20

Table 1.4 List of Products: G Version (T_a = –40 to +105°C) (1/2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature		
RX231	R5F52318AGFP	R5F52318AGFP#30	PLQP0100KB-B	512 Kbytes	64 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Available	−40 to +105°C		
	R5F52318BGFP	R5F52318BGFP#30						Available	Available	Available			
	R5F52318AGND	R5F52318AGND#U0	PWQN0064KC-A					Not available	Not available	Available			
	R5F52318BGND	R5F52318BGND#U0						Available	Available	Available			
	R5F52318AGFM	R5F52318AGFM#30	PLQP0064KB-C					Not available	Not available	Available			
	R5F52318BGFM	R5F52318BGFM#30						Available	Available	Available			
	R5F52318AGNE	R5F52318AGNE#U0	PWQN0048KB-A					Not available	Not available	Available			
	R5F52318BGNE	R5F52318BGNE#U0						Available	Not available	Available			
	R5F52318AGFL	R5F52318AGFL#30	PLQP0048KB-B					Not available	Not available	Available			
	R5F52318BGFL	R5F52318BGFL#30						Available	Not available	Available			
	R5F52317AGFP	R5F52317AGFP#30	PLQP0100KB-B	384 Kbytes				Not available	Not available	Available			
	R5F52317BGFP	R5F52317BGFP#30						Available	Available	Available			
	R5F52317AGND	R5F52317AGND#U0	PWQN0064KC-A					Not available	Not available	Available			
	R5F52317BGND	R5F52317BGND#U0						Available	Available	Available			
	R5F52317AGFM	R5F52317AGFM#30	PLQP0064KB-C					Not available	Not available	Available			
	R5F52317BGFM	R5F52317BGFM#30						Available	Available	Available			
	R5F52317AGNE	R5F52317AGNE#U0	PWQN0048KB-A					Not available	Not available	Available			
	R5F52317BGNE	R5F52317BGNE#U0						Available	Not available	Available			
	R5F52317AGFL	R5F52317AGFL#30	PLQP0048KB-B					Not available	Not available	Available			
	R5F52317BGFL	R5F52317BGFL#30						Available	Not available	Available			
	R5F52316AGFP	R5F52316AGFP#30	PLQP0100KB-B	256 Kbytes				32 Kbytes	Not available	Not available		Available	
	R5F52316CGFP	R5F52316CGFP#30							Not available	Not available		Not available	
	R5F52316AGND	R5F52316AGND#U0	PWQN0064KC-A						Not available	Not available		Available	
	R5F52316CGND	R5F52316CGND#U0							Not available	Not available		Not available	
	R5F52316AGFM	R5F52316AGFM#30	PLQP0064KB-C						Not available	Not available		Available	
	R5F52316CGFM	R5F52316CGFM#30							Not available	Not available		Not available	
	R5F52316AGNE	R5F52316AGNE#U0	PWQN0048KB-A						Not available	Not available		Available	
	R5F52316CGNE	R5F52316CGNE#U0							Not available	Not available		Not available	
	R5F52316AGFL	R5F52316AGFL#30	PLQP0048KB-B						Not available	Not available		Available	
	R5F52316CGFL	R5F52316CGFL#30							Not available	Not available		Not available	
	R5F52315AGFP	R5F52315AGFP#30	PLQP0100KB-B	128 Kbytes						Not available		Not available	Available
	R5F52315CGFP	R5F52315CGFP#30								Not available		Not available	Not available
	R5F52315AGND	R5F52315AGND#U0	PWQN0064KC-A							Not available		Not available	Available
	R5F52315CGND	R5F52315CGND#U0								Not available		Not available	Not available
	R5F52315AGFM	R5F52315AGFM#30	PLQP0064KB-C							Not available		Not available	Available
	R5F52315CGFM	R5F52315CGFM#30								Not available		Not available	Not available
	R5F52315AGNE	R5F52315AGNE#U0	PWQN0048KB-A							Not available		Not available	Available
	R5F52315CGNE	R5F52315CGNE#U0								Not available		Not available	Not available



- Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table "List of Pins and Pin Functions (64-Pin LQFP/HWQFN)".
- Note: It is recommended to connect an exposed die pad to VSS.
- Note 1. RX230: PH0, PH1, PH2, PH3
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Figure 1.6 Pin Assignments of the 64-Pin HWQFN

Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
J6	VCC_USB*1	PH3*1		TMCI0*1				
J7		P50	WR0#/WR#				TS20	
J8		PC4	A20/CS3#	MTIOC3D/MTCLKC/TMC11/POE0#	SCK5/CTS8#/RTS8#/SS8#/SSLA0	SDHI_D1	TSCAP	
J9		PC0	A16	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/SSLA1		TS35	
J10		PC1	A17	MTIOC3A/TCLKD	SCK5/SSLA2		TS33	
K1		P23		MTIOC3D/MTCLKD/TIOCD3	CTS0#/RTS0#/SS0#/SSISCK0		TS6	
K2		P22		MTIOC3B/MTCLKC/TMO0/TIOCC3	SCK0/ USB0_OVRCURB/AUDIO_MCLK		TS7	
K3		P20		MTIOC1A/TMRI0/TIOCB3	TXD0/SMOSI0/SSDA0/USB0_ID/SSIRXD0		TS9	
K4		P14		MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA		TS13	IRQ4/ CVREFB2
K5		PH2*1		TMRI0*1	USB0_DM*1			IRQ1*1
K6		PH1*1		TMO0*1	USB0_DP*1			IRQ0*1
K7		P51	WR1#/BC1#/WAIT#				TS19	
K8		PC5	A21/CS2#/WAIT#	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA		TS23	
K9		PC3	A19	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5/IRTXD5	SDHI_D0	TS27	
K10		PC2	A18	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/SSLA3/IRRXD5	SDHI_D3	TS30	

Note 1. RX230: PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, PH3/TMCI0
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Table 1.7 List of Pins and Pin Functions (100-Pin LFQFP) (2/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, IIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
42		P52	RD#				TS18	
43		P51	WR1#/BC1#/WAIT#				TS19	
44		P50	WR0#/WR#				TS20	
45	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA			CACREF
46		PC6	A22/CS1#	MTIOC3C/MTCLKA/TMC12	RXD8/SMISO8/SSCL8/MOSIA		TS22	
47		PC5	A21/CS2#/WAIT#	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA		TS23	
48		PC4	A20/CS3#	MTIOC3D/MTCLKC/TMC11/POE0#	SCK5/CTS8#/RTS8#/SS8#/SSLA0	SDHI_D1	TSCAP	
49		PC3	A19	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5/IRTXD5	SDHI_D0	TS27	
50		PC2	A18	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/SSLA3/IRRXD5	SDHI_D3	TS30	
51		PC1	A17	MTIOC3A/TCLKD	SCK5/SSLA2		TS33	
52		PC0	A16	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/SSLA1		TS35	
53		PB7	A15	MTIOC3B/TIOCB5	TXD9/SMOSI9/SSDA9	SDHI_D2		
54		PB6	A14	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9	SDHI_D1		
55		PB5	A13	MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOCB4	SCK9/USB0_VBUS	SDHI_CD		
56		PB4	A12	TIOCA4	CTS9#/RTS9#/SS9#			
57		PB3	A11	MTIOC0A/MTIOC4A/TMO0/POE3#/TIOC3D/TCLKD	SCK6	SDHI_W P		
58		PB2	A10	TIOCC3/TCLKC	CTS6#/RTS6#/SS6#			
59		PB1	A9	MTIOC0C/MTIOC4C/TMC10/TIOCB3	TXD6/SMOSI6/SSDA6	SDHI_CLK		IRQ4/CMPOB1
60	VCC							
61		PB0	A8	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/RSPCKA	SDHI_C MD		
62	VSS							
63		PA7	A7	TIOCB2	MISOA			
64		PA6	A6	MTIC5V/MTCLKB/TMC13/POE2#/TIOCA2	CTS5#/RTS5#/SS5#/MOSIA/SSIWS0			
65		PA5	A5	TIOCB1	RSPCKA			
66		PA4	A4	MTIC5U/MTCLKA/TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5			IRQ5 / CVREFB1
67		PA3	A3	MTIOC0D/MTCLKD/TIOC0D/TCLKB	RXD5/SMISO5/SSCL5/SSIRXD0/IRRXD5			IRQ6 /CMPB1
68		PA2	A2		RXD5/SMISO5/SSCL5/SSLA3/IRRXD5			
69		PA1	A1	MTIOC0B/MTCLKC/TIOCB0	SCK5/SSLA2/SSISCK0			
70		PA0	A0/BC0#	MTIOC4A/TIOCA0	SSLA1			CACREF
71		PE7	D15[A15/D15]					IRQ7/AN023
72		PE6	D14[A14/D14]					IRQ6/AN022
73		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B				IRQ5/AN021/CMPOB0
74		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A				AN020/ CMPA2/ CLKOUT
75		PE3	D11[A11/D11]	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/AUDIO_MCLK			AN019/ CLKOUT
76		PE2	D10[A10/D10]	MTIOC4A	RXD12/RXDX12/SMISO12/SSCL12			IRQ7/AN018/ CVREFB0
77		PE1	D9[A9/D9]	MTIOC4C	TXD12/TXDX12/SIOX12/SMOSI12/SSDA12			AN017/ CMPB0
78		PE0	D8[A8/D8]		SCK12			AN016

2. CPU

Figure 2.1 shows register set of the CPU.

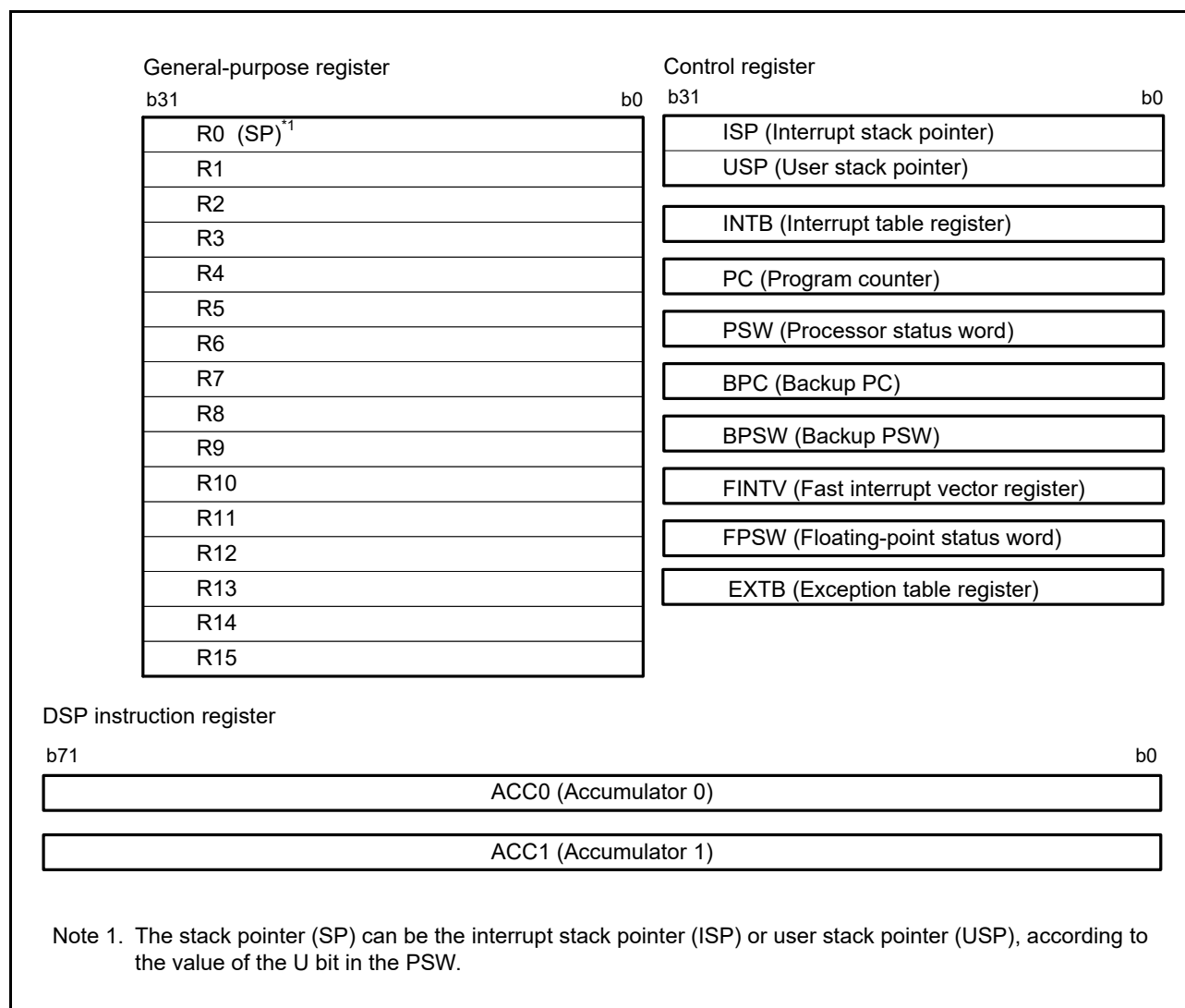


Figure 2.1 Register Set of the CPU

Table 4.1 List of I/O Registers (Address Order) (10/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 A012h	SCI0	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A024h	SCI1	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A025h	SCI1	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A026h	SCI1	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A027h	SCI1	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A028h	SCI1	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 A029h	SCI1	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A02Ah	SCI1	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A02Bh	SCI1	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A02Ch	SCI1	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A02Dh	SCI1	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A02Eh	SCI1	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A02Eh	SCI1	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A02Fh	SCI1	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A030h	SCI1	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A030h	SCI1	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A031h	SCI1	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A032h	SCI1	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A0h	SCI5	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A1h	SCI5	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A2h	SCI5	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A3h	SCI5	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A4h	SCI5	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A5h	SCI5	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A6h	SCI5	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A7h	SCI5	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A8h	SCI5	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A9h	SCI5	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A0AAh	SCI5	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A0ABh	SCI5	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A0ACh	SCI5	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0AEh	SCI5	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A0AEh	SCI5	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A0AFh	SCI5	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A0B0h	SCI5	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A0B0h	SCI5	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A0B1h	SCI5	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A0B2h	SCI5	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C0h	SCI6	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C1h	SCI6	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C2h	SCI6	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C3h	SCI6	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C4h	SCI6	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C5h	SCI6	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C6h	SCI6	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C7h	SCI6	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C8h	SCI6	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (18/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 C15Ah	MPC	P32 Pin Function Control Register	P32PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C15Bh	MPC	P33 Pin Function Control Register	P33PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C15Ch	MPC	P34 Pin Function Control Register	P34PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C160h	MPC	P40 Pin Function Control Register	P40PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C161h	MPC	P41 Pin Function Control Register	P41PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C162h	MPC	P42 Pin Function Control Register	P42PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C163h	MPC	P43 Pin Function Control Register	P43PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C164h	MPC	P44 Pin Function Control Register	P44PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C165h	MPC	P45 Pin Function Control Register	P45PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C166h	MPC	P46 Pin Function Control Register	P46PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C167h	MPC	P47 Pin Function Control Register	P47PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C168h	MPC	P50 Pin Function Control Register	P50PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C169h	MPC	P51 Pin Function Control Register	P51PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C16Ah	MPC	P52 Pin Function Control Register	P52PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C16Bh	MPC	P53 Pin Function Control Register	P53PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C16Ch	MPC	P54 Pin Function Control Register	P54PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C16Dh	MPC	P55 Pin Function Control Register	P55PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C190h	MPC	PA0 Pin Function Control Register	PA0PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C191h	MPC	PA1 Pin Function Control Register	PA1PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C192h	MPC	PA2 Pin Function Control Register	PA2PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C193h	MPC	PA3 Pin Function Control Register	PA3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C194h	MPC	PA4 Pin Function Control Register	PA4PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C195h	MPC	PA5 Pin Function Control Register	PA5PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C196h	MPC	PA6 Pin Function Control Register	PA6PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C197h	MPC	PA7 Pin Function Control Register	PA7PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C19Ah	MPC	PB2 Pin Function Control Register	PB2PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C19Ch	MPC	PB4 Pin Function Control Register	PB4PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1A0h	MPC	PC0 Pin Function Control Register	PC0PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1A1h	MPC	PC1 Pin Function Control Register	PC1PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1A4h	MPC	PC4 Pin Function Control Register	PC4PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1A5h	MPC	PC5 Pin Function Control Register	PC5PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1A6h	MPC	PC6 Pin Function Control Register	PC6PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1A7h	MPC	PC7 Pin Function Control Register	PC7PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1A8h	MPC	PD0 Pin Function Control Register	PD0PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1A9h	MPC	PD1 Pin Function Control Register	PD1PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1AAh	MPC	PD2 Pin Function Control Register	PD2PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1ABh	MPC	PD3 Pin Function Control Register	PD3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1ACh	MPC	PD4 Pin Function Control Register	PD4PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1ADh	MPC	PD5 Pin Function Control Register	PD5PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1AEh	MPC	PD6 Pin Function Control Register	PD6PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1AFh	MPC	PD7 Pin Function Control Register	PD7PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B1h	MPC	PE1 Pin Function Control Register	PE1PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B2h	MPC	PE2 Pin Function Control Register	PE2PFS	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (19/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B6h	MPC	PE6 Pin Function Control Register	PE6PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B7h	MPC	PE7 Pin Function Control Register	PE7PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1C8h	MPC	PH0 Pin Function Control Register	PH0PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1C9h	MPC	PH1 Pin Function Control Register	PH1PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1CAh	MPC	PH2 Pin Function Control Register	PH2PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1CBh	MPC	PH3 Pin Function Control Register	PH3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1D3h	MPC	PJ3 Pin Function Control Register	PJ3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVL	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Dh	SYSTEM	VBATT Control Register	VBATTCT	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Eh	SYSTEM	VBATT Status Register	VBATTST	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Fh	SYSTEM	VBATT Pin Voltage Drop Detection Interrupt Control Register	VBTLVDICR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2 or 3 PCLKB	2 ICLK
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2 or 3 PCLKB	2 ICLK
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2 or 3 PCLKB	2 ICLK
0008 C408h	RTC	Day-of-Week Counter	RWKCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2 or 3 PCLKB	2 ICLK
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2 or 3 PCLKB	2 ICLK
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2 or 3 PCLKB	2 ICLK
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2 or 3 PCLKB	2 ICLK

Table 5.4 DC Characteristics (2)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} < 2.7\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} < 2.7\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	Ports 12, 13, 16, 17, port B5 (5 V tolerant)	V_{IH}	$\text{VCC} \times 0.8$	—	5.8	V
	Ports 14 to 15, ports 20 to 27, ports 30 to 37, ports 50 to 55, ports A0 to A7, ports B0 to B4, B6, B7, ports C0 to C7, ports D0 to D7, ports E0 to E7, port J3, RES#	V_{IH}	$\text{VCC} \times 0.8$	—	$\text{VCC} + 0.3$	V
	Ports 03, 05, 07, ports 40 to 47	V_{IH}	$\text{AVCC0} \times 0.8$	—	$\text{AVCC0} + 0.3$	V
	Ports 03, 05, 07, ports 40 to 47	V_{IL}	-0.3	—	$\text{AVCC0} \times 0.2$	V
	Ports other than above	V_{IL}	-0.3	—	$\text{VCC} \times 0.2$	V
	Ports 03, 05, 07, ports 40 to 47	ΔV_T	$\text{AVCC0} \times 0.01$	—	—	V
	Ports other than above	ΔV_T	$\text{VCC} \times 0.01$	—	—	V
	Ports other than above	ΔV_T	$\text{VCC} \times 0.01$	—	—	V
Input level voltage (except for Schmitt trigger input pins)	MD	V_{IH}	$\text{VCC} \times 0.9$	—	$\text{VCC} + 0.3$	V
	EXTAL (external clock input)	V_{IH}	$\text{VCC} \times 0.8$	—	$\text{VCC} + 0.3$	V
	MD	V_{IL}	-0.3	—	$\text{VCC} \times 0.1$	V
	EXTAL (external clock input)	V_{IL}	-0.3	—	$\text{VCC} \times 0.2$	V

Table 5.5 DC Characteristics (3)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD, port 35	$ I_{in} $	—	—	1.0	μA , $V_{in} = 0\text{ V}$, VCC
Three-state leakage current (off-state)	Ports for 5 V tolerant	$ I_{TSI} $	—	—	1.0	μA , $V_{in} = 0\text{ V}$, 5.8V
	Ports except for 5 V tolerant	$ I_{TSI} $	—	—	0.2	μA , $V_{in} = 0\text{ V}$, VCC
Input capacitance	All input pins (except for port 35, USB0_DM, USB0_DP)	C_{in}	—	—	15	pF , $V_{in} = 0\text{ mV}$, $f = 1\text{ MHz}$, $T_a = 25^\circ\text{C}$
	Port 35, USB0_DM, USB0_DP	C_{in}	—	—	30	pF , $V_{in} = 0\text{ mV}$, $f = 1\text{ MHz}$, $T_a = 25^\circ\text{C}$

Table 5.6 DC Characteristics (4)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input pull-up resistor	All ports (except for port 35)	R_U	10	20	50	$\text{k}\Omega$, $V_{in} = 0\text{ V}$

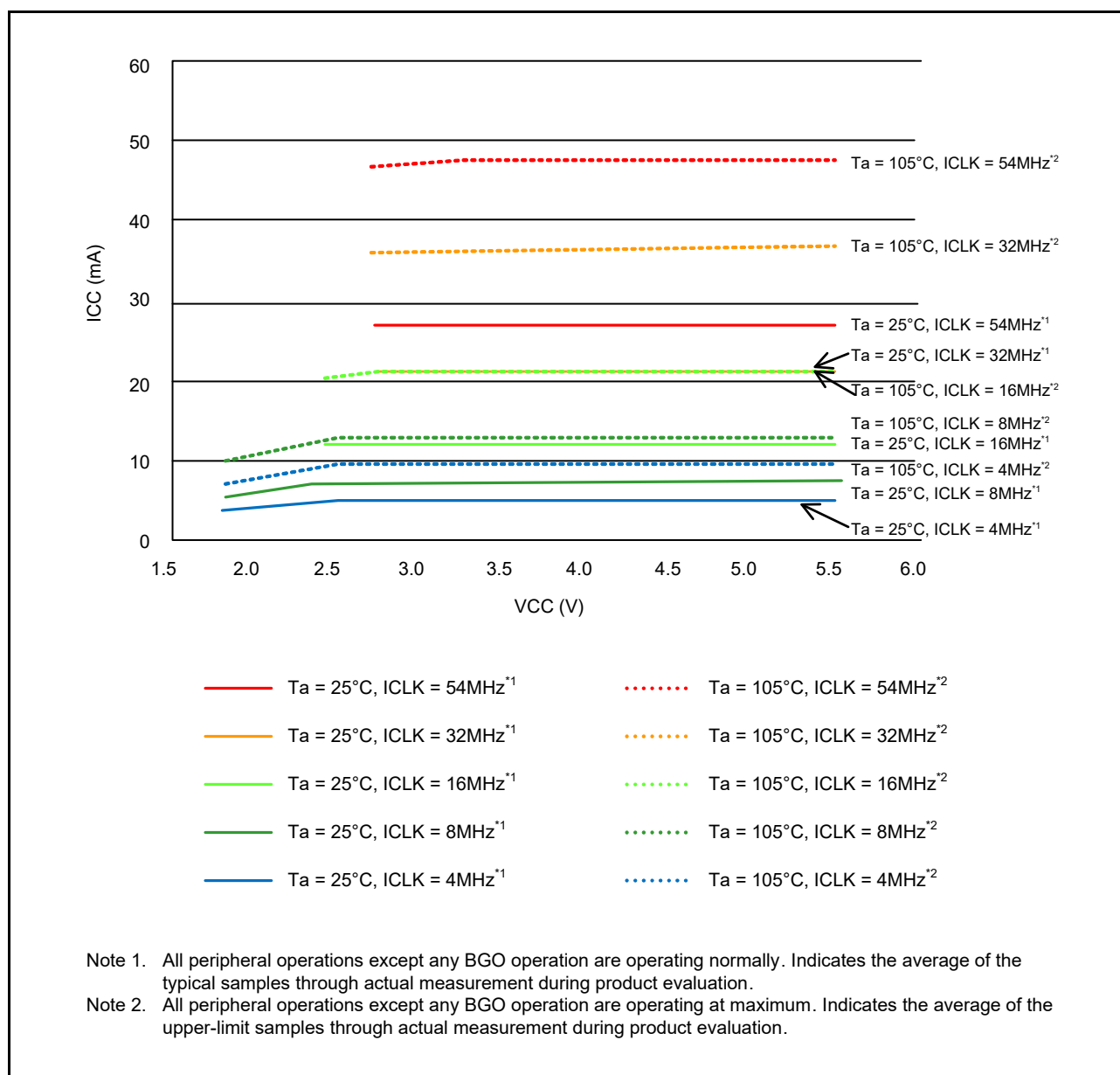


Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data)

Table 5.11 DC Characteristics (9)Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.*7	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion (at high-speed conversion)	—	0.7	1.7	mA	
	During A/D conversion (in low-current mode)	—	0.6	1.0		
	During D/A conversion (per channel)*1	—	0.4	0.8		
	Waiting for A/D and D/A conversion (all units)	—	—	0.4	μA	
Reference power supply current	During A/D conversion (at high-speed conversion)	—	25	150	μA	
	Waiting for A/D conversion (all units)	—	—	60	nA	
	During D/A conversion (per channel)	—	50	100	μA	
	Waiting for D/A conversion (all units)	—	—	100	nA	
LVD1, 2	per channel	—	0.15	—	μA	
Temperature sensor*6	—	—	75	—	μA	
Comparator B operating current*6	Window mode	—	12.5	28.6	μA	
	Comparator high-speed mode (per channel)	—	3.2	16.2	μA	
	Comparator low-speed mode (per channel)	—	1.7	4.4	μA	
CTSU operating current	When sleep mode Base clock frequency: 2MHz Pin capacitance: 50pF	—	150	—	μA	
USB operating current*4	During USB communication operation under the following settings and conditions • Host controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1 • Connect peripheral devices via a 1-meter USB cable from the USB port.	—	4.3 (VCC) 0.9 (VCC_USB)	—	mA	
	During USB communication operation under the following settings and conditions • Function controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1 • Connect the host device via a 1-meter USB cable from the USB port.	—	3.6 (VCC) 1.1 (VCC_USB)	—	mA	
	During suspended state under the following setting and conditions • Function controller operation is set to full-speed mode (pull up the USB0_DP pin) • Software standby mode • Connect the host device via a 1-meter USB cable from the USB port.	—	0.35 (VCC) 170 (VCC_USB)	—	μA	

Note 1. The value of the D/A converter is the value of the power supply current including the reference current.

Note 2. Current consumed only by the USB module.

Note 3. Includes the current supplied from the pull-up resistor of the USB0_DP pin to the pull-down resistor of the host device, in addition to the current consumed by this MCU during the suspended state.

Note 4. Current consumed by the power supplies (VCC and VCC_USB).

Note 5. Current consumed only by the comparator B module.

Note 6. Current consumed by the power supply (VCC).

Note 7. When $VCC = AVCC0 = VCC_USB = 3.3\text{ V}$.**Table 5.12 DC Characteristics (10)**Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.8	—	—	V	

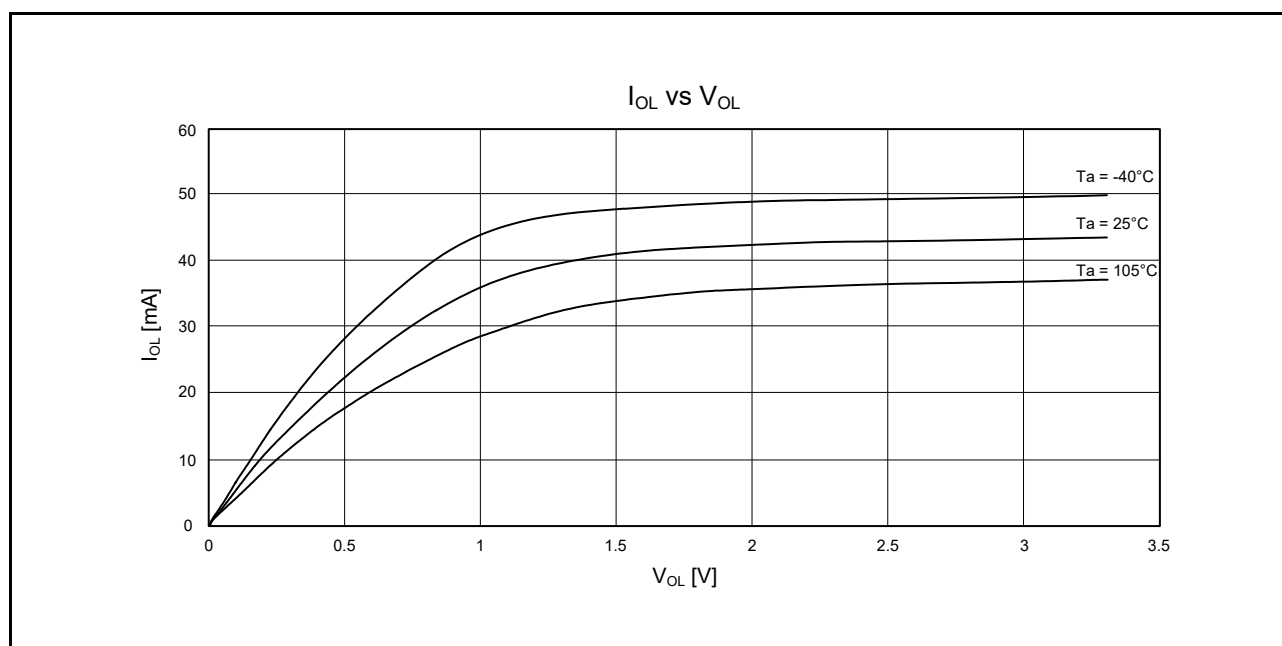


Figure 5.20 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at $V_{CC} = 3.3\text{ V}$ (Reference Data)

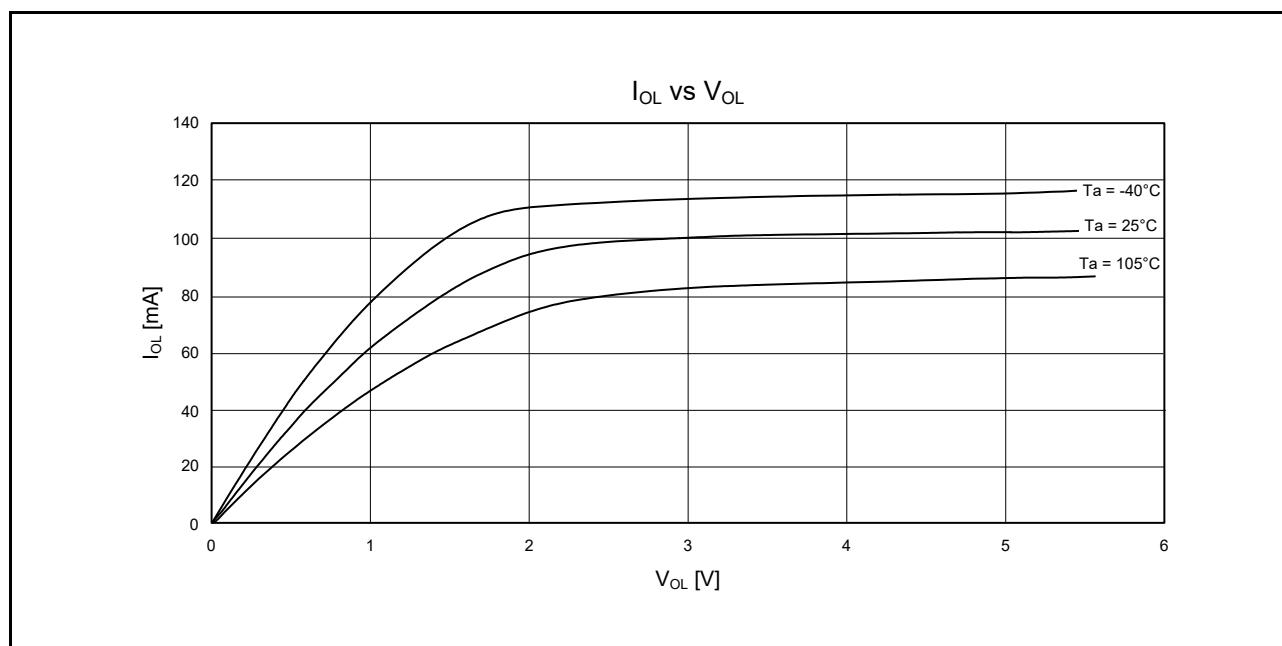


Figure 5.21 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at $V_{CC} = 5.5\text{ V}$ (Reference Data)

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.28 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{REFL0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	High-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 5.34
		External clock input to main clock oscillator	Main clock oscillator operating*3	t_{SBYEX}	—	35	50	μs	
		Sub-clock oscillator operating		t_{SBYSC}	—	650	800	μs	
		HOCO clock oscillator operating		t_{SBYHO}	—	40	55	μs	
		LOCO clock oscillator operating		t_{SBYLO}	—	40	55	μs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. When multiple oscillators are operating, the recovery time varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.

Note 2. When the frequency of the crystal is 20 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.

Note 3. When the frequency of the external clock is 20 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Table 5.29 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{REFL0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Middle-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 5.34
			Main clock oscillator and PLL circuit operating*3	t_{SBYPC}	—	2	3	ms	
		External clock input to main clock oscillator	Main clock oscillator operating*4	t_{SBYEX}	—	3	4	μs	
			Main clock oscillator and PLL circuit operating*5	t_{SBYPE}	—	65	85	μs	
		Sub-clock oscillator operating		t_{SBYSC}	—	600	750	μs	
		HOCO clock oscillator operating*6		t_{SBYHO}	—	40	50	μs	
		LOCO clock oscillator operating		t_{SBYLO}	—	5	7	μs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. When multiple oscillators are operating, the recovery time varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.

Note 2. When the frequency of the crystal is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.

Note 3. When the frequency of PLL is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.

Note 4. When the frequency of the external clock is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Note 5. When the frequency of PLL is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Note 6. This is the case when HOCO is selected as the system clock and its frequency division is set to be 8 MHz.

Table 5.40 Timing of On-Chip Peripheral Modules (3)Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.54
	SCK clock cycle input (slave)			6	65536	t_{Pcyc}	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr} t_{SPCKf}	—	20	ns	
	Data input setup time (master)	2.7 V or above	t_{SU}	65	—	ns	Figure 5.55, Figure 5.56
		1.8 V or above		95	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SSL input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SSL input hold time		t_{LAG}	3	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	2.7 V or above		—	65		
		1.8 V or above		—	100		
	Data output hold time (master)	2.7 V or above	t_{OH}	−10	—	ns	
		1.8 V or above		−20	—		
	Data output hold time (slave)			−10	—		
	Data rise/fall time		t_{Dr} t_{Df}	—	20	ns	
	SSL input rise/fall time		t_{SSLr} t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	Figure 5.57, Figure 5.58
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

Note 1. t_{Pcyc} : PCLK cycle

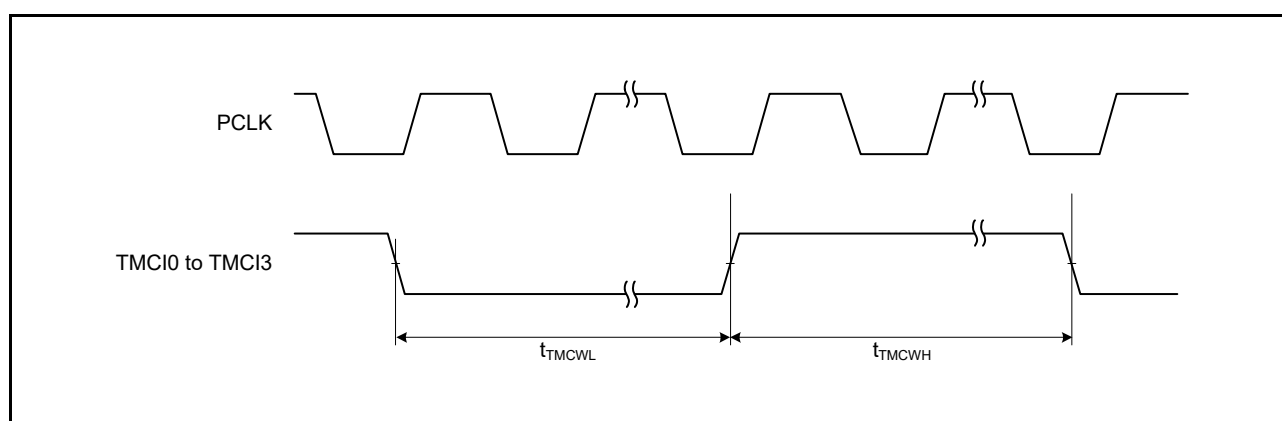


Figure 5.49 TMR Clock Input Timing

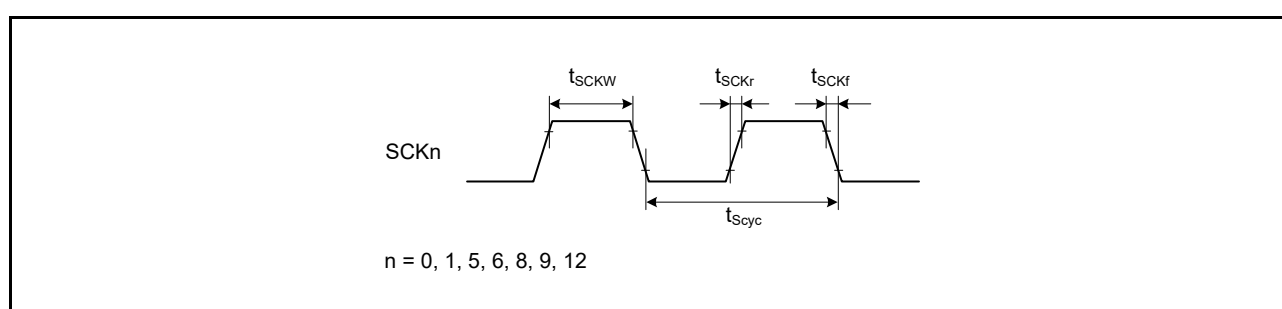


Figure 5.50 SCK Clock Input Timing

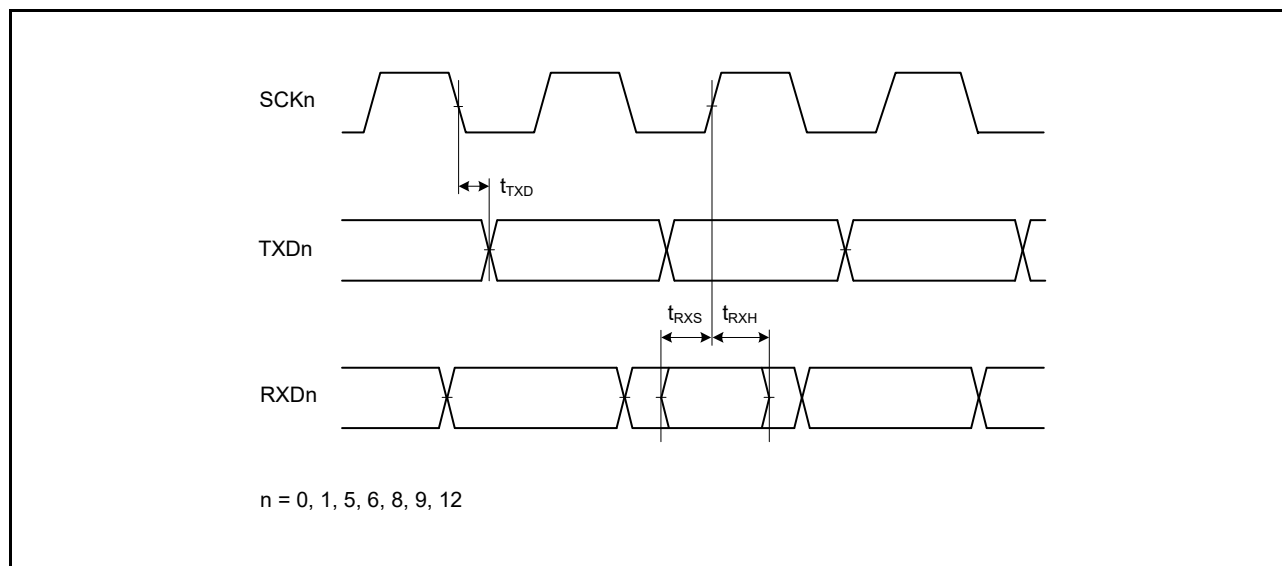


Figure 5.51 SCI Input/Output Timing: Clock Synchronous Mode

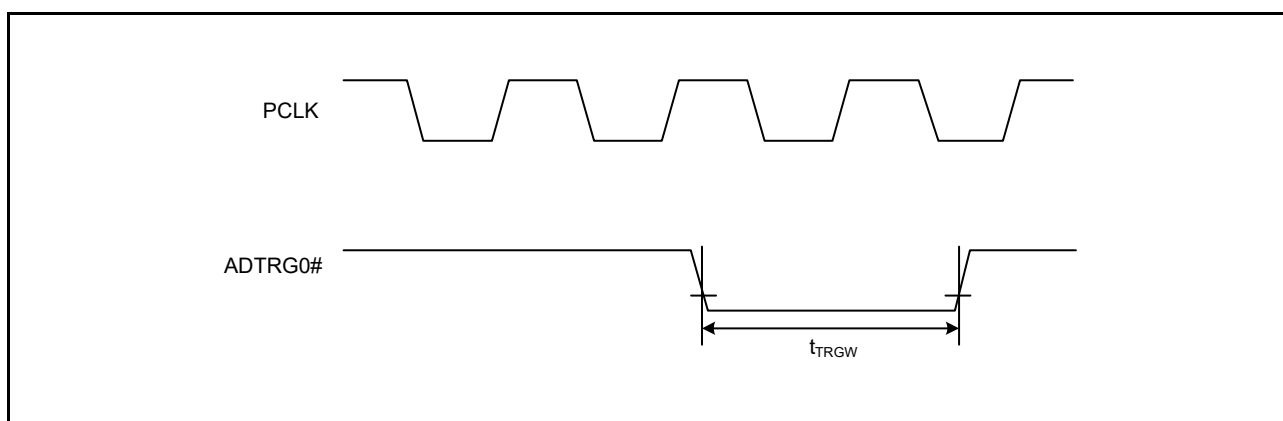


Figure 5.52 A/D Converter External Trigger Input Timing

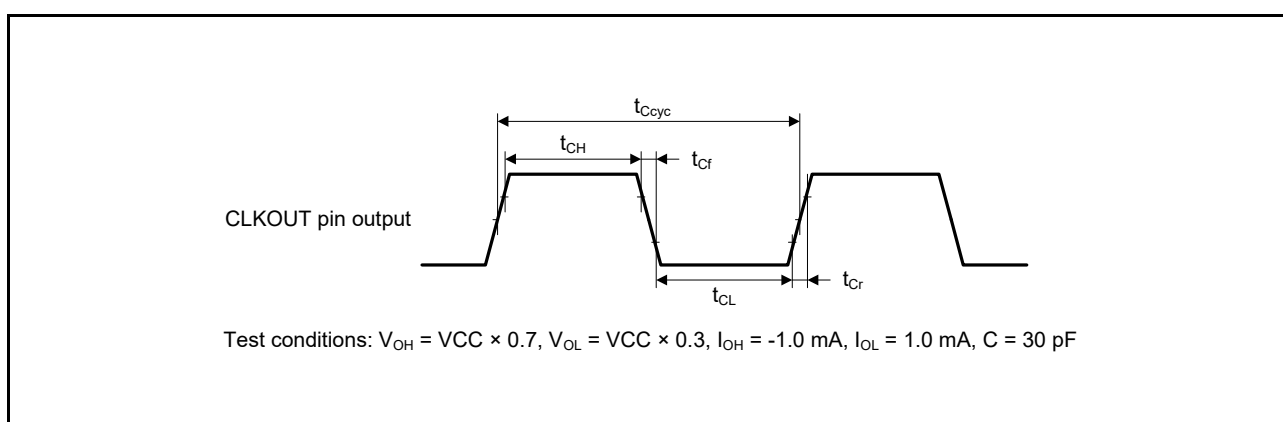


Figure 5.53 CLKOUT Output Timing

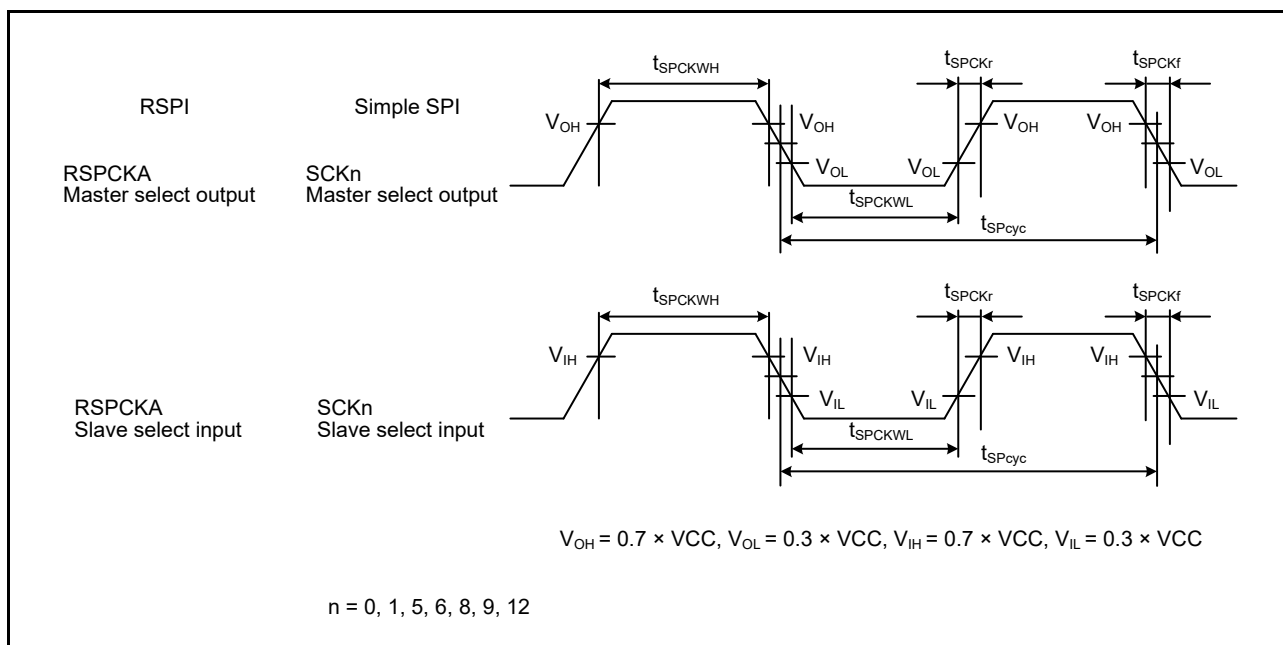


Figure 5.54 RSPI Clock Timing and Simple SPI Clock Timing

5.6 D/A Conversion Characteristics

Table 5.52 D/A Conversion Characteristics (1)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$
 Reference voltage = VREFH or VREFL selected

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Resistive load	30	—	—	k Ω	
Capacitive load	—	—	50	pF	
Output voltage range	0.35	—	$AV_{CC0} - 0.47$	V	
DNL differential non-linearity error	—	± 0.5	± 1.0	LSB	
INL integral non-linearity error	—	± 2.0	± 8.0	LSB	
Offset error	—	—	± 20	mV	
Full-scale error	—	—	± 20	mV	
Output resistance	—	5	—	Ω	
Conversion time	—	—	30	μs	

Table 5.53 D/A Conversion Characteristics (2)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{REFL} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$
 Reference voltage = AVCC0 or AVSS0 selected

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Resistive load	30	—	—	k Ω	
Capacitive load	—	—	50	pF	
Output voltage range	0.35	—	$AV_{CC0} - 0.47$	V	
DNL differential non-linearity error	—	± 0.5	± 2.0	LSB	
INL integral non-linearity error	—	± 2.0	± 8.0	LSB	
Offset error	—	—	± 30	mV	
Full-scale error	—	—	± 30	mV	
Output resistance	—	5	—	Ω	
Conversion time	—	—	30	μs	

Table 5.54 D/A Conversion Characteristics (3)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$
 Reference voltage = internal reference voltage selected

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Internal reference voltage (Vbgr)	1.36	1.43	1.50	V	
Resistive load	30	—	—	k Ω	
Capacitive load	—	—	50	pF	
Output voltage range	0.35	—	Vbgr	V	
DNL differential non-linearity error	—	± 2.0	± 16.0	LSB	
INL integral non-linearity error	—	± 8.0	± 16.0	LSB	
Offset error	—	—	30	mV	
Output resistance	—	5	—	Ω	
Conversion time	—	—	30	μs	

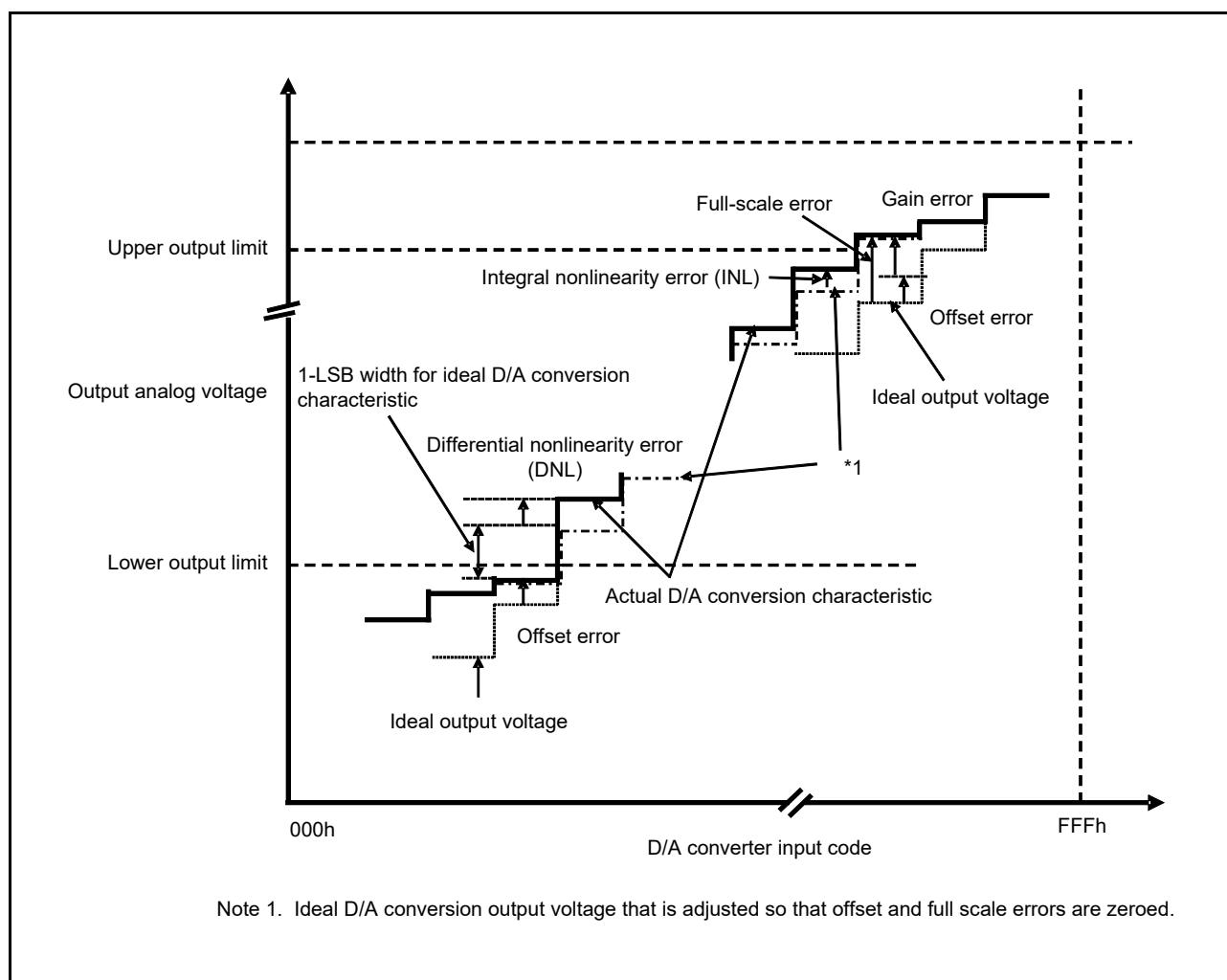


Figure 5.70 Illustration of D/A Converter Characteristic Terms

Integral non-linearity error (INL)

The integral non-linearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential non-linearity error (DNL)

The differential non-linearity error is the difference between 1-LSB width based on the ideal D/A conversion characteristics and the width of the actually output code.

Offset error

An offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

A full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

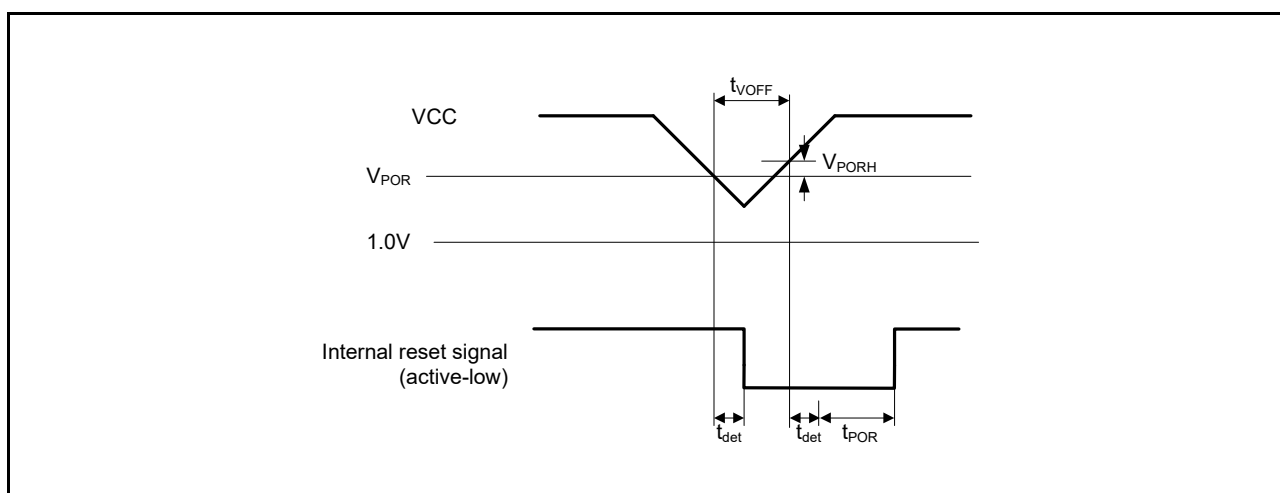


Figure 5.73 Voltage Detection Reset Timing

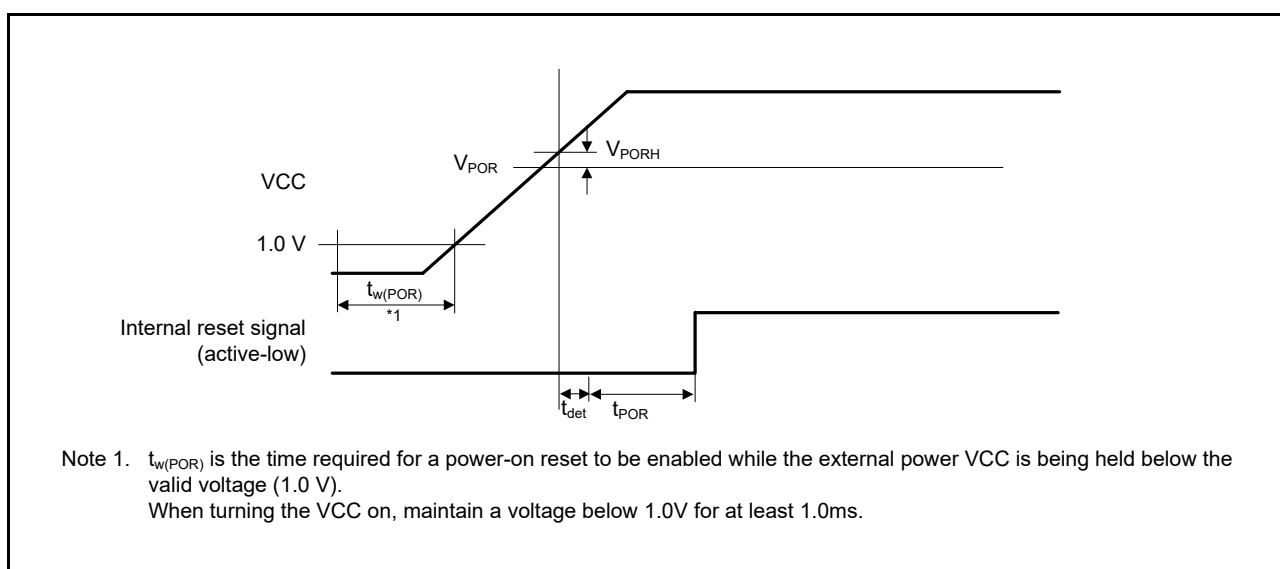


Figure 5.74 Power-On Reset Timing

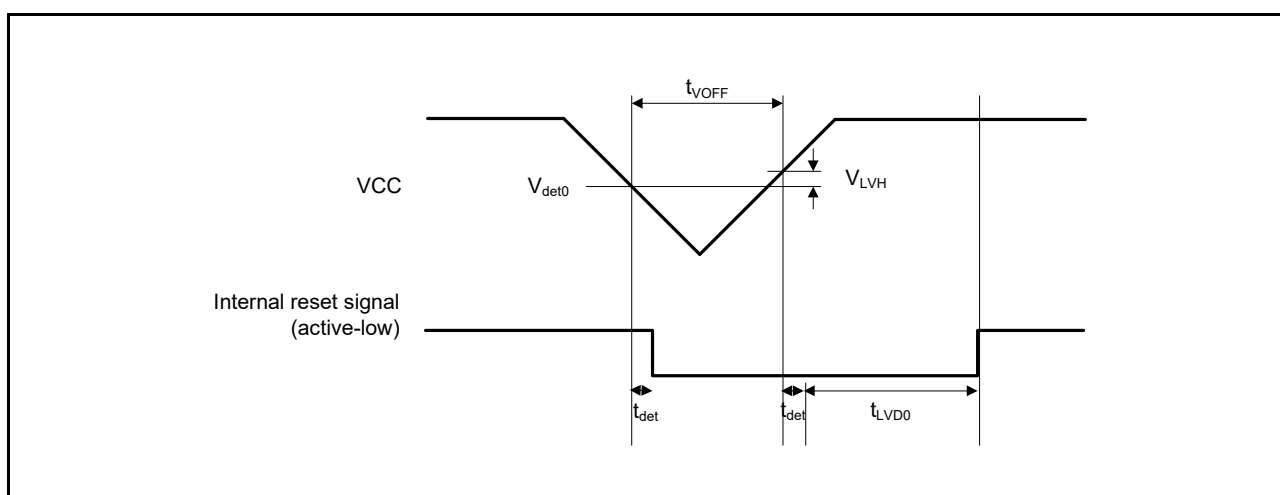


Figure 5.75 Voltage Detection Circuit Timing (Vdet0)

5.13 ROM (Flash Memory for Code Storage) Characteristics

Table 5.62 ROM (Flash Memory for Code Storage) Characteristics (1)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1	N _{PEC}	1000	—	—	Times	
Data hold time	After 1000 times of N _{PEC} t _{DRP}	20*2, *3	—	—	Year	T _a = +85°C

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in a 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.

Note 3. This result is obtained from reliability testing.

Table 5.63 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V

Temperature range for the programming/erasure operation: T_a = −40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8-byte	t _{P8}	—	112	967	—	52.3	491	μs
Erasure time	2-Kbyte	t _{E2K}	—	8.75	278	—	5.50	215	ms
	512-Kbyte (when block erase command is used)	t _{E512K}	—	928	19218	—	72.0	1679	ms
	512-Kbyte (when all-block erase command is used)	t _{EA512K}	—	923	19013	—	66.7	1469	ms
Blank check time	8-byte	t _{BC8}	—	—	55.0	—	—	16.1	μs
	2-Kbyte	t _{BC2K}	—	—	1840	—	—	136	ms
Erasure operation forced stop time		t _{SED}	—	—	18.0	—	—	10.7	μs
Start-up area switching setting time		t _{SAS}	—	12.3	566.5	—	6.2	434	ms
Access window time		t _{AWS}	—	12.3	566.5	—	6.2	434	ms
ROM mode transition wait time 1		t _{DIS}	2.0	—	—	2.0	—	—	μs
ROM mode transition wait time 2		t _{MS}	5.0	—	—	5.0	—	—	μs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be within ±3.5%.