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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	I ² C, IrDA, SCI, SPI, SSI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	47
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	64-HWQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52305adnd-u0

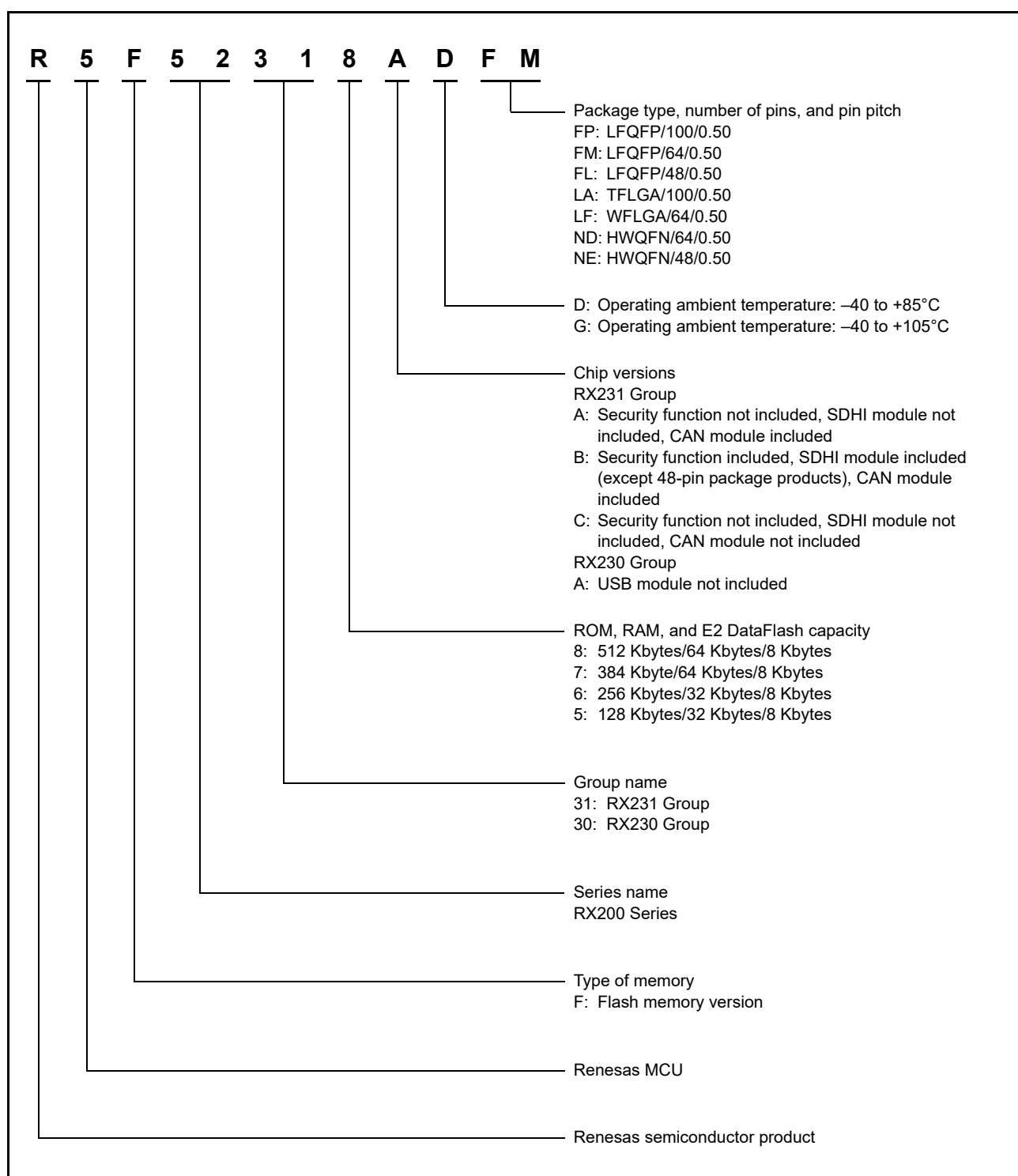


Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 shows a block diagram.

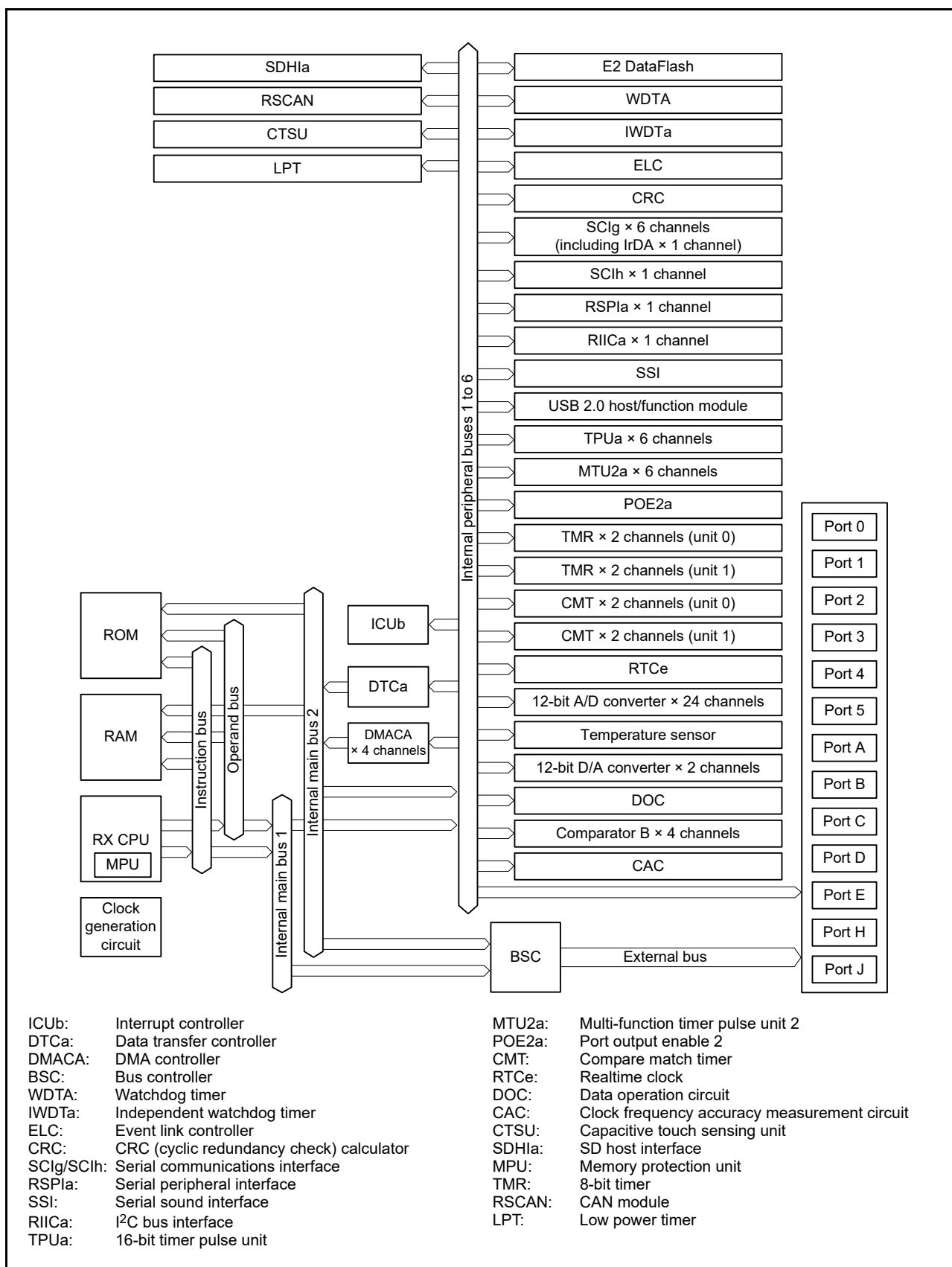


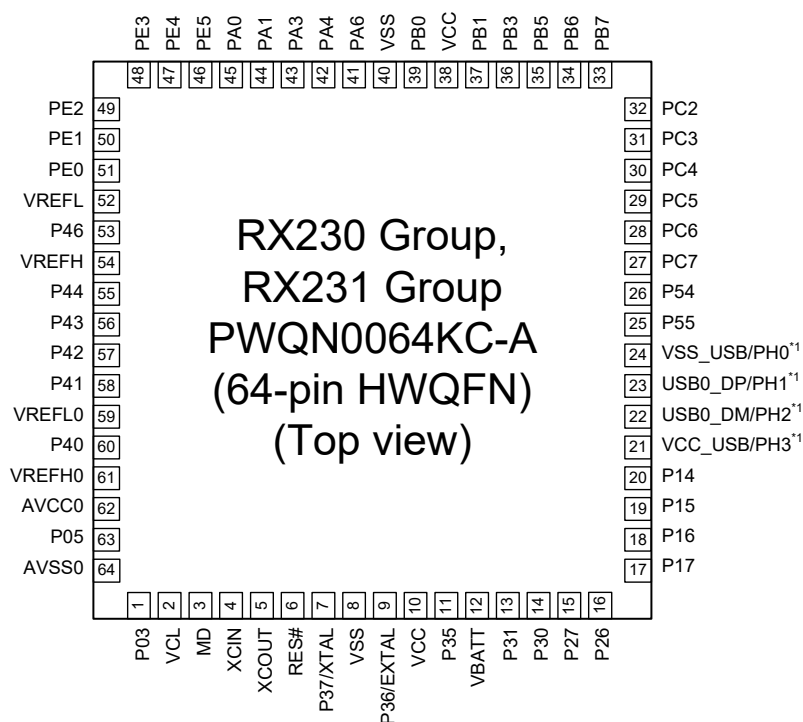
Figure 1.2 Block Diagram

Table 1.5 Pin Functions (2/4)

Classifications	Pin Name	I/O	Description
16-bit timer pulse unit	TIOCA0, TIOCB0 TIOCC0, TIOCD0	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	TIOCA1, TIOCB1	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	TIOCA2, TIOCB2	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	TIOCA3, TIOCB3 TIOCC3, TIOCD3	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	TIOCA4, TIOCB4	I/O	The TGRA4 and TGRB4 input capture input/output compare output/PWM output pins.
	TIOCA5, TIOCB5	I/O	The TGRA5 and TGRB5 input capture input/output compare output/PWM output pins.
	TCLKA, TCLKB TCLKC, TCLKD	Input	Input pins for external clock signals.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
Realtime clock	RTCOUT	Output	Output pin for the 1-Hz/64-Hz clock.
	RTCIC0 to RTCIC2	Input	Time capture event input pins.
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCi0 to TMCi3	Input	Input pins for the external clock to be input to the counter.
	TMRI0 to TMRI3	Input	Counter reset input pins.
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK0, SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock.
	RXD0, RXD1, RXD5, RXD6, RXD8, RXD9	Input	Input pins for received data.
	TXD0, TXD1, TXD5, TXD6, TXD8, TXD9	Output	Output pins for transmitted data.
	CTS0#, CTS1#, CTS5#, CTS6#, CTS8#, CTS9#	Input	Input pins for controlling the start of transmission and reception.
	RTS0#, RTS1#, RTS5#, RTS6#, RTS8#, RTS9#	Output	Output pins for controlling the start of transmission and reception.
	• Simple I ² C mode		
	SSCL0, SSCL1, SSCL5, SSCL6, SSCL8, SSCL9	I/O	Input/output pins for the I ² C clock.
	SSDA0, SSDA1, SSDA5, SSDA6, SSDA8, SSDA9	I/O	Input/output pins for the I ² C data.

Table 1.5 Pin Functions (4/4)

Classifications	Pin Name	I/O	Description
SD host interface	SDHI_D3 to SD_D0	I/O	SD data bus pins
	SDHI_CD	Input	SD card detection pin
	SDHI_WP	Input	SD write-protect signal
USB 2.0 host/ function module	VCC_USB	Input	Power supply pin for USB. Connect this pin to VCC or connect this pin to VSS via a 0.33 μ F smoothing capacitor for stabilizing the internal power supply.
	VSS_USB	Input	Ground pin for USB. Connect this pin to VSS.
	USB0_DP	I/O	D+ I/O pin of the USB on-chip transceiver.
	USB0_DM	I/O	D- I/O pin of the USB on-chip transceiver.
	USB0_VBUS	Input	USB cable connection monitor pin.
	USB0_EXICEN	Output	Low-power control signal for the OTG chip.
	USB0_VBUSEN	Output	VBUS (5 V) supply enable signal for the OTG chip.
	USB0_OVRCURA, USB0_OVRCURB	Input	External overcurrent detection pins.
	USB0_ID	Input	Mini-AB connector ID input pin during operation in OTG mode.
12-bit A/D converter	AN000 to AN007, AN016 to AN031	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signal that start the A/D conversion.
12-bit D/A converter	DA0, DA1	Output	Analog output pins of the D/A converter.
Comparator B	CMPB0 to CMPB3	Input	Input pin for the analog signal to be processed by comparator B.
	CVREFB0 to CVREFB3	Input	Analog reference voltage supply pin for comparator B.
	CMPOB0 to CMPOB3	Output	Output pin for comparator B.
CTSU	TS0 to TS9, TS12, TS13, TS15 to TS20, TS22, TS23, TS27, TS30, TS33, TS35	Output	Electrostatic capacitance measurement pins (touch pins).
	TSCAP	Output	LPF connection pin.
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter and D/A converter. Connect this pin to VCC when not using the 12-bit A/D converter and D/A converter.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter and D/A converter. Connect this pin to VSS when not using the 12-bit A/D converter and D/A converter.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter.
	VREFH	Input	Analog reference voltage supply pin for the 12-bit D/A converter.
	VREFL	Input	Analog reference ground pin for the 12-bit D/A converter.
I/O ports	P03, P05, P07	I/O	3-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins (P35 input pin).
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P55	I/O	6-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ3	I/O	1-bit input/output pin.



- Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table "List of Pins and Pin Functions (64-Pin LQFP/HWQFN)".
- Note: It is recommended to connect an exposed die pad to VSS.
- Note 1. RX230: PH0, PH1, PH2, PH3
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Figure 1.6 Pin Assignments of the 64-Pin HWQFN

Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (1/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
A1		P05						DA1
A2	VREFH							
A3		P07						ADTRG0#
A4	VREFL0							
A5		P43						AN003
A6		PD0	D0[A0/D0]					IRQ0/AN024
A7		PD4	D4[A4/D4]	POE3#				IRQ4/AN028
A8		PE0	D8[A8/D8]		SCK12			AN016
A9		PE1	D9[A9/D9]	MTIOC4C	TXD12/TXD12/SIOX12/SMOSI12/SSDA12			AN017/ CMPB0
A10		PE2	D10[A10/D10]	MTIOC4A	RXD12/RXD12/SMISO12/SSCL12			IRQ7/AN018/ CVREFB0
B1		P03						DA0
B2	AVSS0							
B3	AVCC0							
B4		P40						AN000
B5		P44						AN004
B6		PD1	D1[A1/D1]	MTIOC4B				IRQ1/AN025
B7		PD3	D3[A3/D3]	POE8#				IRQ3/AN027
B8		PD6	D6[A6/D6]	MTIC5V/POE1#				IRQ6/AN030
B9		PD7	D7[A7/D7]	MTIC5U/POE0#				IRQ7/AN031
B10		PE3	D11[A11/D11]	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/AUDIO_MCLK			AN019/ CLKOUT
C1	VCL							
C2	VREFL							
C3		PJ3		MTIOC3C	CTS6#/RTS6#/SS6#			
C4	VREFH0							
C5		P42						AN002
C6		P47						AN007
C7		PD2	D2[A2/D2]	MTIOC4D				IRQ2/AN026
C8		PD5	D5[A5/D5]	MTIC5W/POE2#				IRQ5/AN029
C9		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B				IRQ5/AN021/ CMPOB0
C10		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A				AN020/ CMPA2/ CLKOUT
D1	XCIN							
D2	XCOUT							
D3	MD							FINED
D4	VBATT							
D5		P45						AN005
D6		P46						AN006
D7		PE6	D14[A14/D14]					IRQ6/AN022
D8		PE7	D15[A15/D15]					IRQ7/AN023
D9		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0	SCK5/SSLA2/SSISCK0			
D10		PA0	A0/BC0#	MTIOC4A/TIOCA0	SSLA1			CACREF
E1	XTAL	P37						
E2	VSS							
E3	RES#							
E4		P34		MTIOC0A/TMIC3/POE2#	SCK6		TS0	IRQ4
E5		P41						AN001
E6		PA2	A2		RXD5/SMISO5/SSCL5/ SSLA3/IRRXD5			
E7		PA6	A6	MTIC5V/MTCLKB/TMIC3/ POE2#/TIOCA2	CTS5#/RTS5#/SS5#/ MOSIA/SSIWS0			

Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, IIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
79		PD7	D7[A7/D7]	MTIC5U/POE0#				IRQ7/AN031
80		PD6	D6[A6/D6]	MTIC5V/POE1#				IRQ6/AN030
81		PD5	D5[A5/D5]	MTIC5W/POE2#				IRQ5/AN029
82		PD4	D4[A4/D4]	POE3#				IRQ4/AN028
83		PD3	D3[A3/D3]	POE8#				IRQ3/AN027
84		PD2	D2[A2/D2]	MTIOC4D				IRQ2/AN026
85		PD1	D1[A1/D1]	MTIOC4B				IRQ1/AN025
86		PD0	D0[A0/D0]					IRQ0/AN024
87		P47						AN007
88		P46						AN006
89		P45						AN005
90		P44						AN004
91		P43						AN003
92		P42						AN002
93		P41						AN001
94	VREFL0							
95		P40						AN000
96	VREFH0							
97	AVCC0							
98		P07						ADTRG0#
99	AVSS0							
100		P05						DA1

Note 1. RX230: PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, PH3/TMCI0
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Table 1.9 List of Pins and Pin Functions (64-Pin LFQFP/HWQFN) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, IIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
1		P03					DA0
2	VCL						
3	MD						FINED
4	XCIN						
5	XCOUT						
6	RES#						
7	XTAL	P37					
8	VSS						
9	EXTAL	P36					
10	VCC						
11	UPSEL	P35					NMI
12	VBATT						
13		P31	MTIOC4D/TMC12/RTCIC1	CTS1#/RTS1#/SS1#/SSISCK0			IRQ1
14		P30	MTIOC4B/TMRI3/POE8#/RTCIC0	RXD1/SMISO1/SSCL1/AUDIO_MCLK			IRQ0/CMPOB3
15		P27	MTIOC2B/TMC13	SCK1/SSIWS0		TS2	CVREFB3
16		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/USB0_VBUSEN/SSIRXD0		TS3	CMPB3
17		P17	MTIOC3A/MTIOC3B/TMO1/POE8#/TIOCB0/TCLKD	SCK1/MISOA/SDA/SSITXD0			IRQ7/ CMPOB2
18		P16	MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC/RTCOUT	TXD1/SMOSI1/SSDA1/MOSIA/SCL/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB			IRQ6/ADTRG0#
19		P15	MTIOC0B/MTCLKB/TMC12/TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/CRXD0		TS12	IRQ5/CMPB2
20		P14	MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA		TS13	IRQ4/CVREFB2
21	VCC_USB*1	PH3*1	TMC10*1				
22		PH2*1	TMRI0*1	USB0_DM*1			IRQ1*1
23		PH1*1	TMO0*1	USB0_DP*1			IRQ0*1
24	VSS_USB*1	PH0*1					CACREF*1
25		P55	MTIOC4D/TMO3	CRXD0		TS15	
26		P54	MTIOC4B/TMC11	CTXD0		TS16	
27	UB	PC7	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA			CACREF
28		PC6	MTIOC3C/MTCLKA/TMC12	RXD8/SMISO8/SSCL8/MOSIA/USB0_EXICEN		TS22	
29		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA/USB0_ID		TS23	
30		PC4	MTIOC3D/MTCLKC/TMC11/POE0#	SCK5/CTS8#/RTS8#/SS8#/SSLA0	SDHI_D1	TSCAP	
31		PC3	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5/ IRTXD5	SDHI_D0	TS27	
32		PC2	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/SSLA3/IRRXD5	SDHI_D3	TS30	
33		PB7/PC1	MTIOC3B/TIOCB5	TXD9/SMOSI9/SSDA9	SDHI_D2		
34		PB6/PC0	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9	SDHI_D1		
35		PB5	MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOCB4	SCK9/USB0_VBUS	SDHI_CD		
36		PB3	MTIOC0A/MTIOC4A/TMO0/POE3#/TIOCD3/TCLKD	SCK6	SDHI_W P		
37		PB1	MTIOC0C/MTIOC4C/TMC10/TIOCB3	TXD6/SMOSI6/SSDA6	SDHI_CL K		IRQ4/ CMPOB1
38	VCC						
39		PB0	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/RSPCKA	SDHI_C MD		
40	VSS						
41		PA6	MTIC5V/MTCLKB/TMC13/POE2#/TIOCA2	CTS5#/RTS5#/SS5#/MOSIA/SSIWS0			

4. I/O Registers

This section provides information on the on-chip I/O register addresses and bit configuration. The information is given as shown below. Notes on writing to registers are also given below.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- Numbers of cycles for access indicate numbers of cycles of the given base clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.

As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERN of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

- Write to an I/O register.
- Read the value from the I/O register to a general register.
- Execute the operation using the value read.
- Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.B #SFR_DATA, [R1]
CMP [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.W #SFR_DATA, [R1]
CMP [R1].W, R1
;; Next process
```

Table 4.1 List of I/O Registers (Address Order) (7/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 or 3 PCLKB	2 ICLK
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 or 3 PCLKB	2 ICLK
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 or 3 PCLKB	2 ICLK
0008 8310h	RIIC0	I ² C-Bus Bit Rate Low-Level Register	ICBRL	8	8	2 or 3 PCLKB	2 ICLK
0008 8311h	RIIC0	I ² C-Bus Bit Rate High-Level Register	ICBRH	8	8	2 or 3 PCLKB	2 ICLK
0008 8312h	RIIC0	I ² C-Bus Transmit Data Register	ICDRT	8	8	2 or 3 PCLKB	2 ICLK
0008 8313h	RIIC0	I ² C-Bus Receive Data Register	ICDRR	8	8	2 or 3 PCLKB	2 ICLK
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2 or 3 PCLKB	2 ICLK
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2 or 3 PCLKB	2 ICLK
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2 or 3 PCLKB	2 ICLK
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2 or 3 PCLKB	2 ICLK
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2 or 3 PCLKB	2 ICLK
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2 or 3 PCLKB	2 ICLK
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 or 3 PCLKB	2 ICLK
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2 or 3 PCLKB	2 ICLK
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2 or 3 PCLKB	2 ICLK
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2 or 3 PCLKB	2 ICLK
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2 or 3 PCLKB	2 ICLK
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2 or 3 PCLKB	2 ICLK
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2 or 3 PCLKB	2 ICLK
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2 or 3 PCLKB	2 ICLK
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2 or 3 PCLKB	2 ICLK
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2 or 3 PCLKB	2 ICLK
0008 8410h	IRDA	IrDA Control Register	IRCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8900h	POE	Input Level Control/Status Register 1	ICSR1	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 8902h	POE	Output Level Control/Status Register 1	OCSR1	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 8908h	POE	Input Level Control/Status Register 2	ICSR2	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 890Ah	POE	Software Port Output Enable Register	SPOER	8	8	2 or 3 PCLKB	2 ICLK
0008 890Bh	POE	Port Output Enable Control Register 1	POECR1	8	8	2 or 3 PCLKB	2 ICLK
0008 890Ch	POE	Port Output Enable Control Register 2	POECR2	8	8	2 or 3 PCLKB	2 ICLK
0008 890Eh	POE	Input Level Control/Status Register 3	ICSR3	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB	2 ICLK
0008 9004h	S12AD	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB	2 ICLK
0008 9006h	S12AD	A/D Channel Select Register A1	ADANSA1	16	16	2 or 3 PCLKB	2 ICLK
0008 9008h	S12AD	A/D-Converted Value Addition/Average Function Select Register 0	ADADS0	16	16	2 or 3 PCLKB	2 ICLK
0008 900Ah	S12AD	A/D-Converted Value Addition/Average Function Select Register 1	ADADS1	16	16	2 or 3 PCLKB	2 ICLK
0008 900Ch	S12AD	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB	2 ICLK
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB	2 ICLK
0008 9010h	S12AD	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB	2 ICLK
0008 9012h	S12AD	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB	2 ICLK
0008 9014h	S12AD	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB	2 ICLK
0008 9016h	S12AD	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB	2 ICLK
0008 9018h	S12AD	A/D Data Duplication Register	ADBLDR	16	16	2 or 3 PCLKB	2 ICLK
0008 901Ah	S12AD	A/D Temperature Sensor Data Register	ADTSR	16	16	2 or 3 PCLKB	2 ICLK
0008 901Ch	S12AD	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (15/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK $\geq$ PCLK	ICLK < PCLK
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 B306h	SCI12	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 B309h	SCI12	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 B30Ah	SCI12	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 B30Bh	SCI12	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 B30Ch	SCI12	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 B30Eh	SCI12	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 B30Eh	SCI12	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 B30Fh	SCI12	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 B310h	SCI12	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 B310h	SCI12	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 B311h	SCI12	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 B312h	SCI12	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 B320h	SCI12	Extended Serial Module Enable Register	ESMER	8	8	2 or 3 PCLKB	2 ICLK
0008 B321h	SCI12	Control Register 0	CR0	8	8	2 or 3 PCLKB	2 ICLK
0008 B322h	SCI12	Control Register 1	CR1	8	8	2 or 3 PCLKB	2 ICLK
0008 B323h	SCI12	Control Register 2	CR2	8	8	2 or 3 PCLKB	2 ICLK
0008 B324h	SCI12	Control Register 3	CR3	8	8	2 or 3 PCLKB	2 ICLK
0008 B325h	SCI12	Port Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 B326h	SCI12	Interrupt Control Register	ICR	8	8	2 or 3 PCLKB	2 ICLK
0008 B327h	SCI12	Status Register	STR	8	8	2 or 3 PCLKB	2 ICLK
0008 B328h	SCI12	Status Clear Register	STCR	8	8	2 or 3 PCLKB	2 ICLK
0008 B329h	SCI12	Control Field 0 Data Register	CF0DR	8	8	2 or 3 PCLKB	2 ICLK
0008 B32Ah	SCI12	Control Field 0 Compare Enable Register	CF0CR	8	8	2 or 3 PCLKB	2 ICLK
0008 B32Bh	SCI12	Control Field 0 Receive Data Register	CF0RR	8	8	2 or 3 PCLKB	2 ICLK
0008 B32Ch	SCI12	Primary Control Field 1 Data Register	PCF1DR	8	8	2 or 3 PCLKB	2 ICLK
0008 B32Dh	SCI12	Secondary Control Field 1 Data Register	SCF1DR	8	8	2 or 3 PCLKB	2 ICLK
0008 B32Eh	SCI12	Control Field 1 Compare Enable Register	CF1CR	8	8	2 or 3 PCLKB	2 ICLK
0008 B32Fh	SCI12	Control Field 1 Receive Data Register	CF1RR	8	8	2 or 3 PCLKB	2 ICLK
0008 B330h	SCI12	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 B331h	SCI12	Timer Mode Register	TMR	8	8	2 or 3 PCLKB	2 ICLK
0008 B332h	SCI12	Timer Prescaler Register	TPRE	8	8	2 or 3 PCLKB	2 ICLK
0008 B333h	SCI12	Timer Count Register	TCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C004h	PORT4	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C005h	PORT5	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C00Ah	PORTA	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C00Ch	PORTC	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C00Dh	PORTD	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C011h	PORTH	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C012h	PORTJ	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C021h	PORT1	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C022h	PORT2	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (31/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 862Eh	RSCAN	RAM Test Register 87	RPGACC87	16	16	2 or 3 PCLKB	2 ICLK
000A 8630h	RSCAN0	Transmit Buffer Register 3AL	TMIDL3	16	16	2 or 3 PCLKB	2 ICLK
000A 8630h	RSCAN	RAM Test Register 88	RPGACC88	16	16	2 or 3 PCLKB	2 ICLK
000A 8632h	RSCAN0	Transmit Buffer Register 3AH	TMIDH3	16	16	2 or 3 PCLKB	2 ICLK
000A 8632h	RSCAN	RAM Test Register 89	RPGACC89	16	16	2 or 3 PCLKB	2 ICLK
000A 8634h	RSCAN	RAM Test Register 90	RPGACC90	16	16	2 or 3 PCLKB	2 ICLK
000A 8636h	RSCAN0	Transmit Buffer Register 3BH	TMPTR3	16	16	2 or 3 PCLKB	2 ICLK
000A 8636h	RSCAN	RAM Test Register 91	RPGACC91	16	16	2 or 3 PCLKB	2 ICLK
000A 8638h	RSCAN0	Transmit Buffer Register 3CL	TMDFO3	16	16	2 or 3 PCLKB	2 ICLK
000A 8638h	RSCAN	RAM Test Register 92	RPGACC92	16	16	2 or 3 PCLKB	2 ICLK
000A 863Ah	RSCAN0	Transmit Buffer Register 3CH	TMDF13	16	16	2 or 3 PCLKB	2 ICLK
000A 863Ah	RSCAN	RAM Test Register 93	RPGACC93	16	16	2 or 3 PCLKB	2 ICLK
000A 863Ch	RSCAN0	Transmit Buffer Register 3DL	TMDF23	16	16	2 or 3 PCLKB	2 ICLK
000A 863Ch	RSCAN	RAM Test Register 94	RPGACC94	16	16	2 or 3 PCLKB	2 ICLK
000A 863Eh	RSCAN0	Transmit Buffer Register 3DH	TMDF33	16	16	2 or 3 PCLKB	2 ICLK
000A 863Eh	RSCAN	RAM Test Register 95	RPGACC95	16	16	2 or 3 PCLKB	2 ICLK
000A 8640h to 000A 867Eh	RSCAN	RAM Test Register 96 to RAM Test Register 127	RPGACC96 to RPGACC127	16	16	2 or 3 PCLKB	2 ICLK
000A 8680h	RSCAN0	Transmit History Buffer Access Register	THLACC0	16	16	2 or 3 PCLKB	2 ICLK
000D 0A00h	MTU3	Timer Control Register	TCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A01h	MTU4	Timer Control Register	TCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A02h	MTU3	Timer Mode Register	TMDR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A03h	MTU4	Timer Mode Register	TMDR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A04h	MTU3	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKA	2 ICLK
000D 0A05h	MTU3	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKA	2 ICLK
000D 0A06h	MTU4	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKA	2 ICLK
000D 0A07h	MTU4	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKA	2 ICLK
000D 0A08h	MTU3	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKA	2 ICLK
000D 0A09h	MTU4	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKA	2 ICLK
000D 0A0Ah	MTU	Timer Output Master Enable Register	TOER	8	8	2 or 3 PCLKA	2 ICLK
000D 0A0Dh	MTU	Timer Gate Control Register	TGCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A0Eh	MTU	Timer Output Control Register 1	TOCR1	8	8	2 or 3 PCLKA	2 ICLK
000D 0A0Fh	MTU	Timer Output Control Register 2	TOCR2	8	8	2 or 3 PCLKA	2 ICLK
000D 0A10h	MTU3	Timer Counter	TCNT	16	16	2 or 3 PCLKA	2 ICLK
000D 0A12h	MTU4	Timer Counter	TCNT	16	16	2 or 3 PCLKA	2 ICLK
000D 0A14h	MTU	Timer Cycle Data Register	TCDR	16	16	2 or 3 PCLKA	2 ICLK
000D 0A16h	MTU	Timer Dead Time Data Register	TDDR	16	16	2 or 3 PCLKA	2 ICLK
000D 0A18h	MTU3	Timer General Register A	TGRA	16	16	2 or 3 PCLKA	2 ICLK
000D 0A1Ah	MTU3	Timer General Register B	TGRB	16	16	2 or 3 PCLKA	2 ICLK
000D 0A1Ch	MTU4	Timer General Register A	TGRA	16	16	2 or 3 PCLKA	2 ICLK
000D 0A1Eh	MTU4	Timer General Register B	TGRB	16	16	2 or 3 PCLKA	2 ICLK
000D 0A20h	MTU	Timer Subcounters	TCNTS	16	16	2 or 3 PCLKA	2 ICLK
000D 0A22h	MTU	Timer Cycle Buffer Register	TCBR	16	16	2 or 3 PCLKA	2 ICLK
000D 0A24h	MTU3	Timer General Register C	TGRC	16	16	2 or 3 PCLKA	2 ICLK
000D 0A26h	MTU3	Timer General Register D	TGRD	16	16	2 or 3 PCLKA	2 ICLK
000D 0A28h	MTU4	Timer General Register C	TGRC	16	16	2 or 3 PCLKA	2 ICLK
000D 0A2Ah	MTU4	Timer General Register D	TGRD	16	16	2 or 3 PCLKA	2 ICLK
000D 0A2Ch	MTU3	Timer Status Register	TSR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A2Dh	MTU4	Timer Status Register	TSR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A30h	MTU	Timer Interrupt Skipping Set Register	TITCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A31h	MTU	Timer Interrupt Skipping Counters	TITCNT	8	8	2 or 3 PCLKA	2 ICLK
000D 0A32h	MTU	Timer Buffer Transfer Set Register	TBTER	8	8	2 or 3 PCLKA	2 ICLK

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = VREFL = VSS_USB = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC, VCC_USB	−0.3 to +6.5	V
VBATT power supply voltage		Vbatt	−0.3 to +6.5	V
Input voltage	Ports for 5 V tolerant*1	V _{in}	−0.3 to +6.5	V
	P03, P05, P07, P40 to P47		−0.3 to AVCC0 +0.3	
	Ports other than above		−0.3 to VCC +0.3	
Reference power supply voltage		VREFH0	−0.3 to AVCC0 +0.3	V
		VREFH		
Analog power supply voltage		AVCC0	−0.3 to +6.5	V
Analog input voltage	When AN000 to AN007 are used	V _{AN}	−0.3 to AVCC0 +0.3	V
	When AN016 to AN031 are used		−0.3 to VCC +0.3	
Operating temperature*2		T _{opr}	−40 to +85 −40 to +105	°C
Storage temperature		T _{stg}	−55 to +125	°C

Caution: Permanent damage to the MCU may be caused if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the VCC_USB and VSS_USB pins, between the VREFH0 and VREFL0 pins, and between the VREFH and VREFL pins. Place capacitors of about 0.1 μF as close as possible to every power supply pin and use the shortest and heaviest possible traces.

Connect the VCL pin to a VSS pin via a 4.7 μF capacitor. The capacitor must be placed close to the pin. For details, refer to section 5.15.1, Connecting VCL Capacitor and Bypass Capacitors.

Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered.

The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Even if −0.3 to +6.5 V is input to 5-V tolerant ports, it will not cause problems such as damage to the MCU.

Note 1. Ports 12, 13, 16, 17, 30, 31, 32, and B5 are 5 V tolerant.

Note 2. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, refer to section 1.2, List of Products.

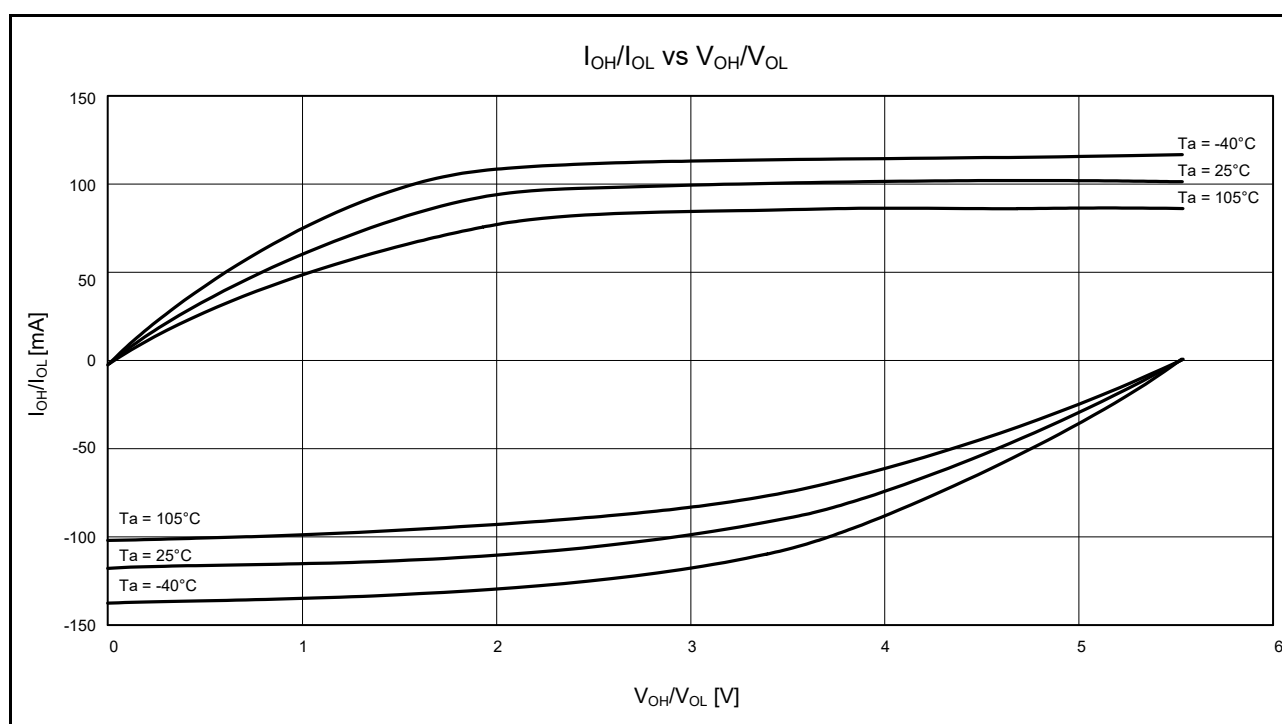


Figure 5.17 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 5.5$ V When High-Drive Output is Selected (Reference Data)

Table 5.26 Clock TimingConditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VREFL0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t _{Xcyc}	50	—	—	ns	Figure 5.23
EXTAL external clock input high pulse width		t _{XH}	20	—	—	ns	
EXTAL external clock input low pulse width		t _{XL}	20	—	—	ns	
EXTAL external clock rise time		t _{Xr}	—	—	5	ns	
EXTAL external clock fall time		t _{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1		t _{XWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency*2	2.4 ≤ VCC ≤ 5.5	f _{MAIN}	1	—	20	MHz	
	1.8 ≤ VCC < 2.4		1	—	8		
Main clock oscillation stabilization time (crystal)*2		t _{MAINOSC}	—	3	—	ms	Figure 5.24
Main clock oscillation stabilization time (ceramic resonator)*2		t _{MAINOSC}	—	50	—	μs	
LOCO clock oscillation frequency		f _{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation stabilization time		t _{LOCO}	—	—	0.5	μs	Figure 5.25
IWDT-dedicated clock oscillation frequency		f _{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time		t _{ILOCO}	—	—	50	μs	Figure 5.26
HOCO clock oscillation frequency		f _{HOCO} (32 MHz)	31.52	32	32.48	MHz	T _a = −40 to + 85°C
			31.68	32	32.32		T _a = 0 to + 55°C
			31.36	32	32.64		T _a = −40 to +105°C
		f _{HOCO} (54 MHz)	53.19	54	54.81	MHz	T _a = −40 to + 85°C
			53.46	54	54.54		T _a = 0 to + 55°C
			52.92	54	55.08		T _a = −40 to +105°C
HOCO clock oscillation stabilization time		t _{HOCO}	—	—	30	μs	Figure 5.28
PLL input frequency*3		f _{PLLIN}	4	—	12.5	MHz	
PLL circuit oscillation frequency*3		f _{PLL}	24	—	54	MHz	
PLL clock oscillation stabilization time		t _{PLL}	—	—	50	μs	Figure 5.29
PLL free-running oscillation frequency		f _{PLLFR}	—	8	—	MHz	
USBPLL input frequency*5		f _{PLLIN}	—	6, 8*6	—	MHz	
USBPLL circuit oscillation frequency*5		f _{PLL}	—	48*6	—	MHz	
USBPLL clock oscillation stabilization time		t _{PLL}	—	—	50	μs	Figure 5.29
Sub-clock oscillator oscillation frequency*7		f _{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*4		t _{SUBOSC}	—	0.5	—	s	Figure 5.30

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating).

Note 2. Reference values when an 8-MHz resonator is used.

When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.

After the MOSCCR.MOSTP bit is changed to enable the main clock oscillator, confirm that the OSCOVFSR.MOOVF flag has become 1, and then start using the main clock.

Note 3. The VCC range should be 2.4 to 5.5 V when the PLL is used.

Note 4. Reference values when a 32.768-kHz resonator is used.

After the setting of the SOSCCR.SOSTP bit or RCR3.RTCEN bit is changed to operate the sub-clock oscillator, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.

Note 5. The VCC range should be 3.0 to 5.5 V when the USBPLL is used.

Note 6. The input frequency can be set to 6 or 8 MHz and the oscillation frequency can be set to 48 MHz only.

Note 7. Only 32.768 kHz can be used.

5.3.5 Bus Timing

Table 5.34 Bus Timing (1)

Conditions: $2.7\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$,
 $f_{BCLK} \leq 32\text{ MHz}$ (BCLK pin output frequency $\leq 16\text{ MHz}$), $T_a = -40\text{ to }+105^\circ\text{C}$, $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$,
 $I_{OH} = -1.0\text{ mA}$, $I_{OL} = 1.0\text{ mA}$, $C_L = 30\text{ pF}$, when normal output is selected by the drive capacity control register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	55	ns	Figure 5.38 to Figure 5.41
Byte control delay time	t_{BCD}	—	55	ns	
CS# delay time	t_{CSD}	—	55	ns	
RD# delay time	t_{RSD}	—	55	ns	
Read data setup time	t_{RDS}	40	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	55	ns	
Write data delay time	t_{WDD}	—	55	ns	
Write data hold time	t_{WDH}	0	—	ns	Figure 5.42
WAIT# setup time	t_{WTS}	40	—	ns	
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.35 Bus Timing (2)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} < 2.7\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$,
 $f_{BCLK} \leq 16\text{ MHz}$ (BCLK pin output frequency $\leq 8\text{ MHz}$), $T_a = -40\text{ to }+105^\circ\text{C}$, $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$,
 $I_{OH} = -1.0\text{ mA}$, $I_{OL} = 1.0\text{ mA}$, $C_L = 30\text{ pF}$, when normal output is selected by the drive capacity control register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	90	ns	Figure 5.38 to Figure 5.41
Byte control delay time	t_{BCD}	—	90	ns	
CS# delay time	t_{CSD}	—	90	ns	
RD# delay time	t_{RSD}	—	90	ns	
Read data setup time	t_{RDS}	60	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	90	ns	
Write data delay time	t_{WDD}	—	90	ns	
Write data hold time	t_{WDH}	0	—	ns	Figure 5.42
WAIT# setup time	t_{WTS}	60	—	ns	
WAIT# hold time	t_{WTH}	0	—	ns	

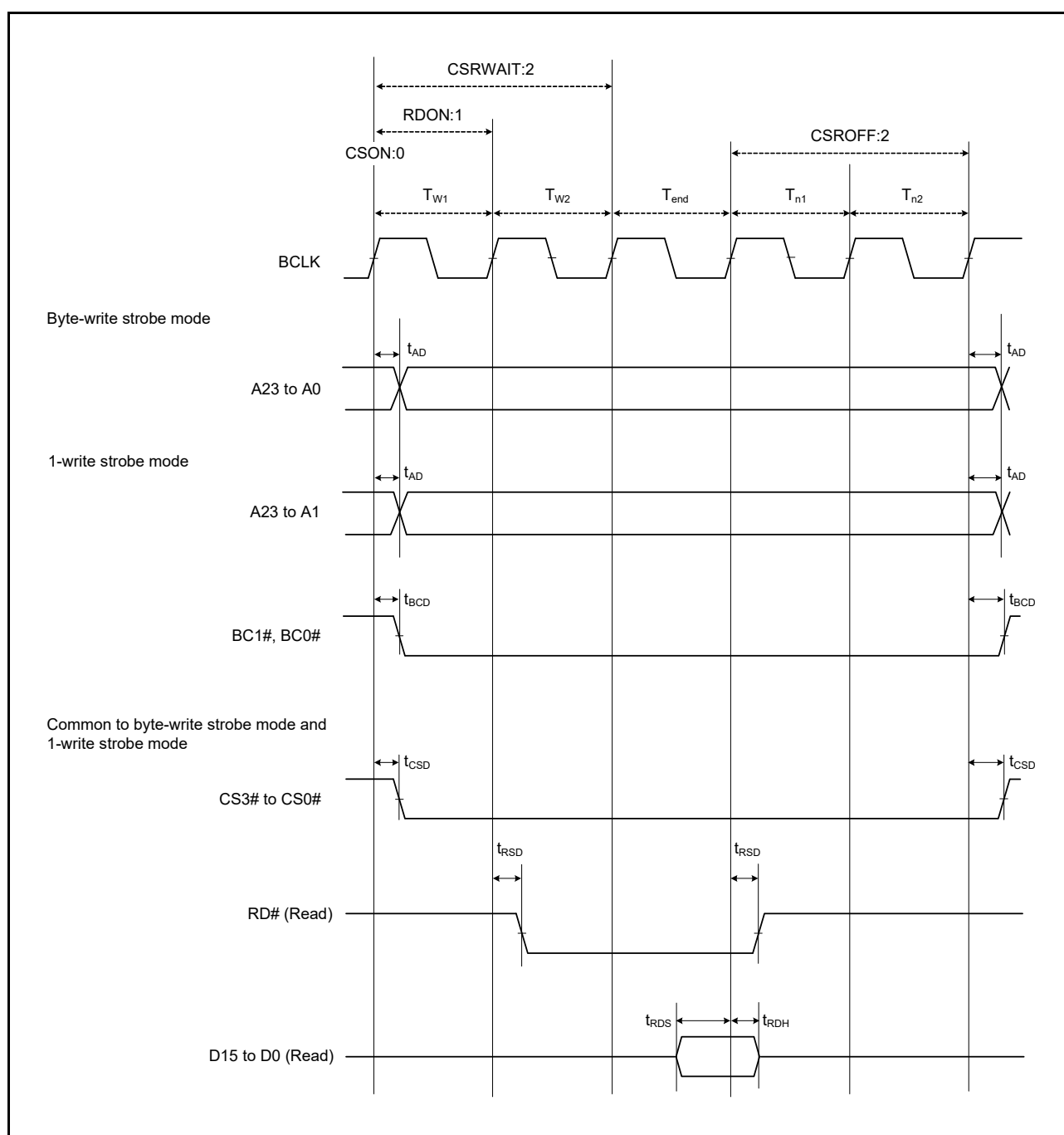


Figure 5.38 External Bus Timing/Normal Read Cycle (Bus Clock Synchronization)

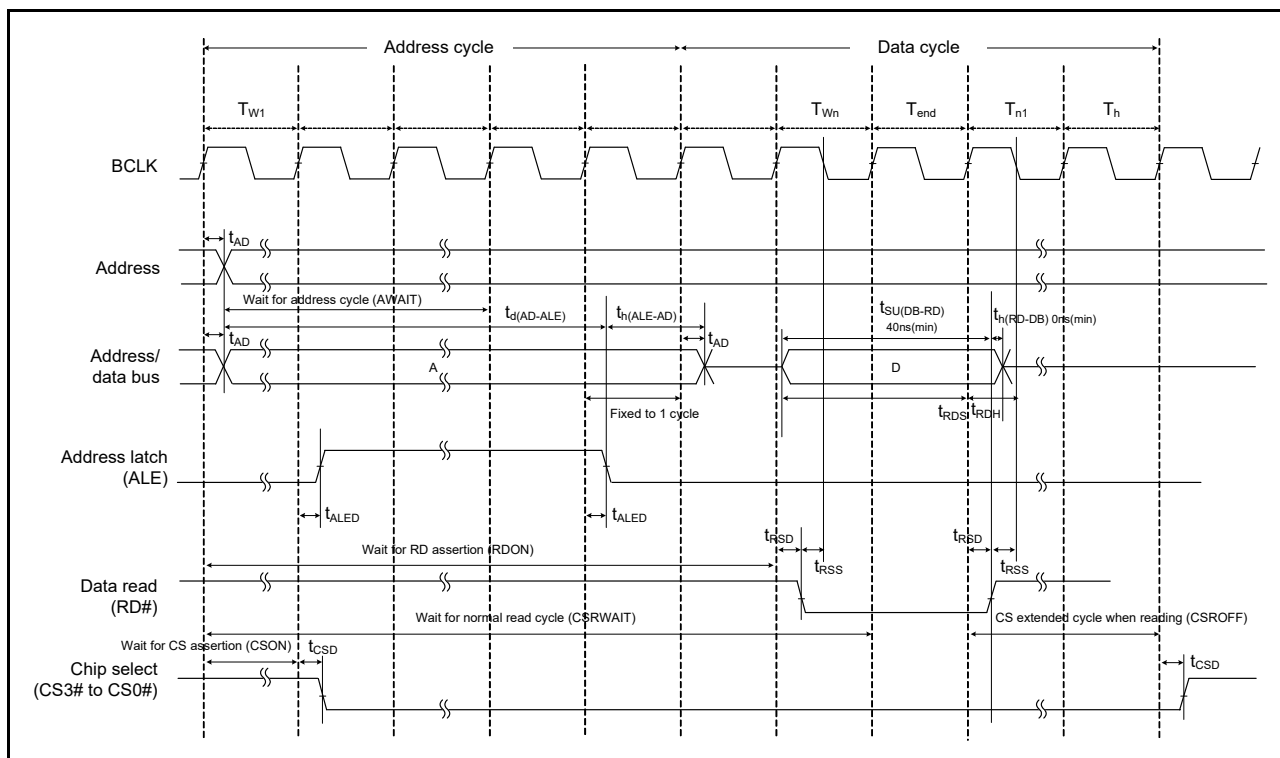


Figure 5.43 External Bus Timing/Read Access Operation Example (Multiplex)

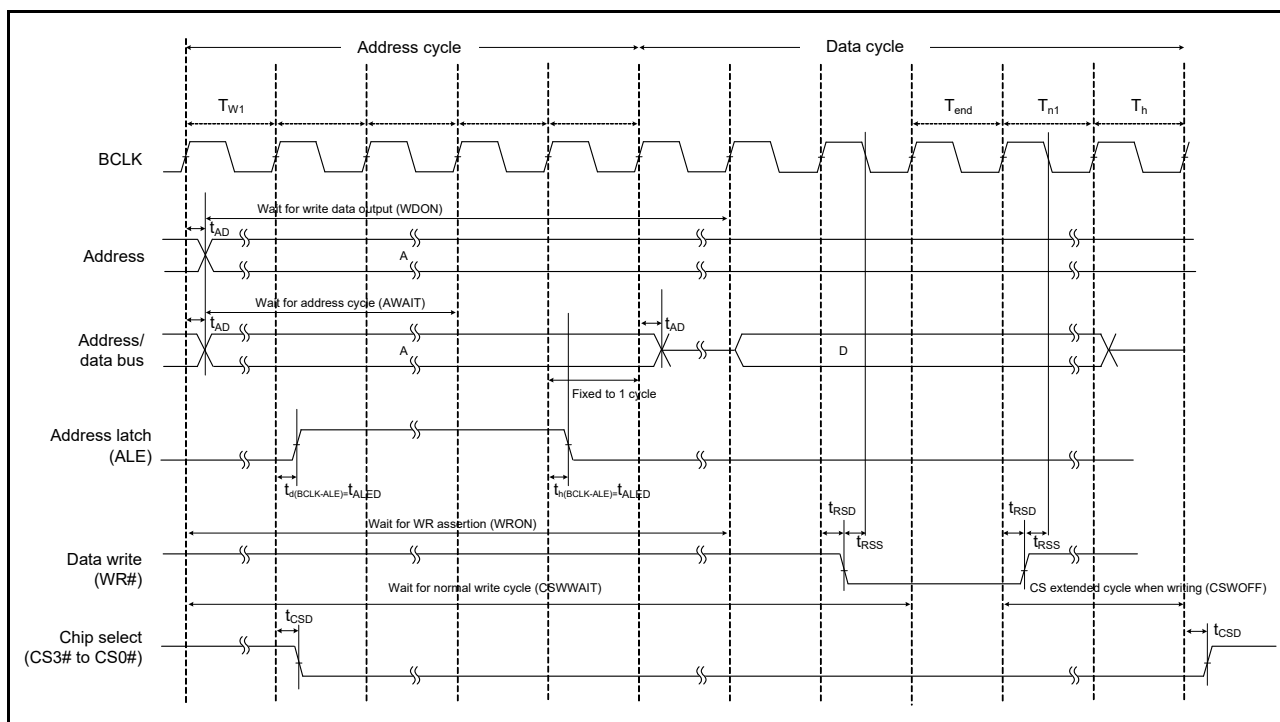


Figure 5.44 External Bus Timing/Write Access Operation Example (Multiplex)

Table 5.40 Timing of On-Chip Peripheral Modules (3)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.54
	SCK clock cycle input (slave)			6	65536	t_{Pcyc}	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		$t_{\text{SPCKr}}, t_{\text{SPCKf}}$	—	20	ns	
Simple SPI	Data input setup time (master)	2.7 V or above	t_{SU}	65	—	ns	Figure 5.55, Figure 5.56
		1.8 V or above		95	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_{H}	40	—	ns	
	SSL input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SSL input hold time		t_{LAG}	3	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	2.7 V or above		—	65		
		1.8 V or above		—	100		
	Data output hold time (master)	2.7 V or above	t_{OH}	−10	—	ns	
		1.8 V or above		−20	—		
	Data output hold time (slave)			−10	—		
	Data rise/fall time		$t_{\text{Dr}}, t_{\text{Df}}$	—	20	ns	
	SSL input rise/fall time		$t_{\text{SSLr}}, t_{\text{SSLf}}$	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	Figure 5.57, Figure 5.58
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

Note 1. t_{Pcyc} : PCLK cycle

Table 5.49 A/D Conversion Characteristics (4)

Conditions: $2.4V \leq VCC = VCC_USB = AVCC0 \leq 5.5V$, $2.4V \leq VREFH0 \leq AVCC0$, $VSS = AVSS0 = VSS_USB = 0V$,
reference voltage = VREFH0 selected, $T_a = -40$ to $+105^\circ C$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance (Max.) = 2.2 kΩ	3.38	—	—	μs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 0Dh
		5.06	—	—		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 5.68
Analog input resistance	Rs	—	—	2.5	kΩ	Figure 5.68
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential non-linearity error		—	±1.0	—	LSB	
INL integral non-linearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.