Renesas Electronics America Inc - R5F52306ADFP#30 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	EBI/EMI, I²C, IrDA, SCI, SPI, SSI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52306adfp-30

Table 1.4 List of Products: G Version (T_a = –40 to +105°C) (1/2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature
RX231	R5F52318AGFP	R5F52318AGFP#30	PLQP0100KB-B	512 Kbytes	64 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Available	–40 to +105°C
	R5F52318BGFP	R5F52318BGFP#30						Available	Available	Available	
	R5F52318AGND	R5F52318AGND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52318BGND	R5F52318BGND#U0						Available	Available	Available	
	R5F52318AGFM	R5F52318AGFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52318BGFM	R5F52318BGFM#30						Available	Available	Available	
	R5F52318AGNE	R5F52318AGNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52318BGNE	R5F52318BGNE#U0						Available	Not available	Available	
	R5F52318AGFL	R5F52318AGFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52318BGFL	R5F52318BGFL#30						Available	Not available	Available	
	R5F52317AGFP	R5F52317AGFP#30	PLQP0100KB-B	384 Kbytes				Not available	Not available	Available	
	R5F52317BGFP	R5F52317BGFP#30						Available	Available	Available	
	R5F52317AGND	R5F52317AGND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52317BGND	R5F52317BGND#U0						Available	Available	Available	
	R5F52317AGFM	R5F52317AGFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52317BGFM	R5F52317BGFM#30						Available	Available	Available	
	R5F52317AGNE	R5F52317AGNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52317BGNE	R5F52317BGNE#U0						Available	Not available	Available	
	R5F52317AGFL	R5F52317AGFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52317BGFL	R5F52317BGFL#30						Available	Not available	Available	
	R5F52316AGFP	R5F52316AGFP#30	PLQP0100KB-B	256 Kbytes	32 Kbytes			Not available	Not available	Available	
	R5F52316CGFP	R5F52316CGFP#30						Not available	Not available	Not available	
	R5F52316AGND	R5F52316AGND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52316CGND	R5F52316CGND#U0						Not available	Not available	Not available	
	R5F52316AGFM	R5F52316AGFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52316CGFM	R5F52316CGFM#30						Not available	Not available	Not available	
	R5F52316AGNE	R5F52316AGNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52316CGNE	R5F52316CGNE#U0						Not available	Not available	Not available	
	R5F52316AGFL	R5F52316AGFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52316CGFL	R5F52316CGFL#30						Not available	Not available	Not available	
	R5F52315AGFP	R5F52315AGFP#30	PLQP0100KB-B	128 Kbytes				Not available	Not available	Available	
	R5F52315CGFP	R5F52315CGFP#30						Not available	Not available	Not available	
	R5F52315AGND	R5F52315AGND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52315CGND	R5F52315CGND#U0						Not available	Not available	Not available	
	R5F52315AGFM	R5F52315AGFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52315CGFM	R5F52315CGFM#30						Not available	Not available	Not available	
	R5F52315AGNE	R5F52315AGNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52315CGNE	R5F52315CGNE#U0						Not available	Not available	Not available	

Table 1.5 Pin Functions (3/4)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIg)	• Simple SPI mode		
	SCK0, SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock.
	SMISO0, SMISO1, SMISO5, SMISO6, SMISO8, SMISO9	I/O	Input/output pins for slave transmit data.
	SMOSI0, SMOSI1, SMOSI5, SMOSI6, SMOSI8, SMOSI9	I/O	Input/output pins for master transmit data.
	SS0#, SS1#, SS5#, SS6#, SS8#, SS9#	Input	Slave-select input pins.
IrDA interface	IRTXD5	Output	Data output pin in the IrDA format.
	IRRXD5	Input	Data input pin in the IrDA format.
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock.
	RXD12	Input	Input pin for receiving data.
	TXD12	Output	Output pin for transmitting data.
	CTS12#	Input	Input pin for controlling the start of transmission and reception.
	RTS12#	Output	Output pin for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock.
	SSDA12	I/O	Input/output pin for the I^2C data.
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock.
	SMISO12	I/O	Input/output pin for slave transmit data.
	SMOSI12	I/O	Input/output pin for master transmit data.
	SS12#	Input	Slave-select input pin.
	• Extended serial mode		
	RXDX12	Input	Input pin for data reception by SCIf.
	TXDX12	Output	Output pin for data transmission by SCIf.
	SIOX12	I/O	Input/output pin for data reception or transmission by SCIf.
I^2C bus interface	SCL	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the N-channel open drain output.
Serial peripheral interface	RSPCKA	I/O	Input/output pin for the RSPI clock.
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master.
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI.
Serial sound interface	SSISCK0	I/O	SSI serial bit clock pin.
	SSIWS0	I/O	Word selection pin.
	SSITXD0	Output	Serial data output pin.
	SSIRXD0	Input	Serial data input pin.
	AUDIO_MCLK	Input	Master clock pin for audio.
CAN module	CRXD0	Input	Input pin
	CTXD0	Output	Output pin
SD host interface	SDHI_CLK	Output	SD clock output pin
	SDHI_CMD	I/O	SD command output, response input signal pin

Table 1.7 List of Pins and Pin Functions (100-Pin LFQFP) (1/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
1	VREFH							
2		P03						DA0
3	VREFL							
4		PJ3		MTIOC3C	CTS6#/RTS6#/SS6#			
5	VCL							
6	VBATT							
7	MD							FINED
8	XCIN							
9	XCOUT							
10	RES#							
11	XTAL	P37						
12	VSS							
13	EXTAL	P36						
14	VCC							
15	UPSEL	P35						NMI
16		P34		MTIOC0A/TMCI3/POE2#	SCK6		TS0	IRQ4
17		P33		MTIOC0D/TMRI3/POE3#/ TIOCD0	RXD6/SMISO6/SSCL6		TS1	IRQ3
18		P32		MTIOC0C/TMO3/TIOCC0/ RTCOUT/RTCIC2	TXD6/SMOSI6/SSDA6/ USB0_VBUSEN			IRQ2
19		P31		MTIOC4D/TMCI2/RTCIC1	CTS1#/RTS1#/SS1#/ SSISCK0			IRQ1
20		P30		MTIOC4B/TMRI3/POE8#/ RTCIC0	RXD1/SMISO1/SSCL1/ AUDIO_MCLK			IRQ0/ CMPOB3
21		P27	CS3#	MTIOC2B/TMCI3	SCK1/ SSIWS0		TS2	CVREFB3
22		P26	CS2#	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ SSIRXD0		TS3	CMPB3
23		P25	CS1#	MTIOC4C/MTCLKB/ TIOCA4			TS4	ADTRG0#
24		P24	CS0#	MTIOC4A/MTCLKA/TMRI1/ TIOCB4	USB0_VBUSEN		TS5	
25		P23		MTIOC3D/MTCLKD/ TIOCD3	CTS0#/RTS0#/SS0#/ SSISCK0		TS6	
26		P22		MTIOC3B/MTCLKC/TMO0/ TIOCC3	SCK0/ USB0_OVRCURB/ AUDIO_MCLK		TS7	
27		P21		MTIOC1B/TMCI0/TIOCA3	RXD0/SMISO0/SSCL0/ USB0_EXICEN/SSIWS0		TS8	
28		P20		MTIOC1A/TMRI0/TIOCB3	TXD0/SMOSI0/SSDA0/ USB0_ID/SSIRXD0		TS9	
29		P17		MTIOC3A/MTIOC3B/TMO1/ POE8#/TIOCB0/TCLKD	SCK1/MISOA/SDA/ SSITXD0			IRQ7/ CMPOB2
30		P16		MTIOC3C/MTIOC3D/ TMO2/TIOCB1/TCLKC/ RTCOUT	TXD1/SMOSI1/SSDA1/ MOSIA/SCL/USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB			IRQ6/ ADTRG0#
31		P15		MTIOC0B/MTCLKB/TMCI2/ TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/ CRXD0		TS12	IRQ5/CMPB2
32		P14		MTIOC3A/MTCLKA/TMRI2/ TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/ CTXD0/USB0_OVRCURA		TS13	IRQ4/ CVREFB2
33		P13		MTIOC0B/TMO3/TIOCA5	SDA			IRQ3
34		P12		TMCI1	SCL			IRQ2
35	VCC_USB*1	PH3*1		TMCI0*1				
36		PH2*1		TMRI0*1	USB0_DM*1			IRQ1*1
37		PH1*1		TMO0*1	USB0_DP*1			IRQ0*1
38	VSS_USB*1	PH0*1						CACREF*1
39		P55	WAIT#	MTIOC4D/TMO3	CRXD0		TS15	
40		P54	ALE	MTIOC4B/TMCI1	CTXD0		TS16	
41	BCLK	P53					TS17	

Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
A1		P05					DA1
A2	AVCC0						
A3	VREFH0						
A4	VREFL0						
A5	VREFH						
A6	VREFL						
A7		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12			IRQ7/AN018/ CVREFB0
A8		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/ AUDIO_MCLK			AN019/CLKOUT
B1	VCL						
B2	AVSS0						
B3		P40					AN000
B4		P42					AN002
B5		P44					AN004
B6		P46					AN006
B7		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12			AN017/CMPB0
B8		PE4	MTIOC4D/MTIOC1A				AN020/CMPA2/ CLKOUT
C1	XCIN						
C2	MD						FINED
C3		P03					DA0
C4		P41					AN001
C5		P43					AN003
C6		PE0		SCK12			AN016
C7		PE5	MTIOC4C/MTIOC2B				IRQ5/AN021/ CMPOB0
C8		PA0	MTIOC4A/TIOCA0	SSLA1			CACREF
D1	XCOUT						
D2	RES#						
D3		P27	MTIOC2B/TMCI3	SCK1/ SSIWS0		TS2	CVREFB3
D4		P14	MTIOC3A/MTCLKA/TMRI2/ TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/ USB0_OVRCURA		TS13	IRQ4/CVREFB2
D5		PA6	MTIC5V/MTCLKB/TMCI3/POE2#/ TIOCA2	CTS5#/RTS5#/SS5#/MOSIA/ SSIWS0			
D6		PA4	MTIC5U/MTCLKA/TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/SSLA0/ SSITXD0/IRTXD5			IRQ5 /CVREFB1
D7		PA1	MTIOC0B/MTCLKC/TIOCB0	SCK5/SSLA2/SSISCK0			
D8		PA3	MTIOC0D/MTCLKD/TIOCD0/ TCLKB	RXD5/SMISO5/SSCL5/SSIRXD0/ IRRXD5			IRQ6 /CMPB1
E1	VSS						
E2	VBATT						
E3		P30	MTIOC4B/TMRI3/POE8#/RTCIC0	RXD1/SMISO1/SSCL1/ AUDIO_MCLK			IRQ0/CMPOB3
E4		P16	MTIOC3C/MTIOC3D/TMO2/ TIOCB1/TCLKC/RTCOUT	TXD1/SMOSI1/SSDA1/MOSIA/ SCL/USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB			IRQ6/ADTRG0#
E5		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	SDHI_D1	TSCAP	
E6	VCC						
E7	VSS						
E8		PB0	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/RSPCKA	SDHI_C MD		
F1	VCC						
F2	UPSEL	P35					NMI
F3		P31	MTIOC4D/TMCI2/RTCIC1	CTS1#/RTS1#/SS1#/SSISCK0			IRQ1

Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
F4		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA/USB0_ID			TS23
F5		P15	MTIOC0B/MTCLKB/TMCI2/ TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/CRXD0		TS12	IRQ5/CMPB2
F6		PB1	MTIOC0C/MTIOC4C/TMCI0/ TIOCB3	TXD6/SMOSI6/SSDA6	SDHI_CLK		IRQ4/ CMPOB1
F7		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#/TIOCB4	SCK9/USB0_VBUS	SDHI_CD		
F8		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#/TIOCD3/TCLKD	SCK6	SDHI_WP		
G1	EXTAL	P36					
G2		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ USB0_VBUSEN/SSIRXD0		TS3	CMPB3
G3	VCC_USB*1	PH3*1	TMCI0*1				
G4	VSS_USB*1	PH0*1					CACREF*1
G5	UB	PC7	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA			CACREF
G6		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA/ USB0_EXICEN		TS22	
G7		PC3	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5/IRTXD5	SDHI_D0	TS27	
G8		PB6/PC0	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9	SDHI_D1		
H1	XTAL	P37					
H2		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#/TIOCB0/TCLKD	SCK1/MISOA/SDA/SSITXD0			IRQ7/ CMPOB2
H3		PH2*1	TMRI0*1	USB0_DM*1			IRQ1*1
H4		PH1*1	TMO0*1	USB0_DP*1			IRQ0*1
H5		P55	MTIOC4D/TMO3	CRXD0		TS15	
H6		P54	MTIOC4B/TMCI1	CTXD0		TS16	
H7		PC2	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/SSLA3/ IRRXD5	SDHI_D3	TS30	
H8		PB7/PC1	MTIOC3B/TIOCB5	TXD9/SMOSI9/SSDA9	SDHI_D2		

Note 1. RX230: PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, PH3/TMCI0
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Table 1.9 List of Pins and Pin Functions (64-Pin LFQFP/HWQFN) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
42		PA4	MTIC5U/MTCLKA/TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/SSLA0/ SSITXD0/IRTXD5			IRQ5 /CVREFB1
43		PA3	MTIOC0D/MTCLKD/TIOCD0/ TCLKB	RXD5/SMISO5/SSCL5/SSIRXD0/ IRRXD5			IRQ6 /CMPB1
44		PA1	MTIOC0B/MTCLKC/TIOCB0	SCK5/SSLA2/SSISCK0			
45		PA0	MTIOC4A/TIOCA0	SSLA1			CACREF
46		PE5	MTIOC4C/MTIOC2B				IRQ5/AN021/ CMPOB0
47		PE4	MTIOC4D/MTIOC1A				AN020/CMPA2/ CLKOUT
48		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/ AUDIO_MCLK			AN019/CLKOUT
49		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12			IRQ7/AN018/ CVREFB0
50		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12			AN017/CMPB0
51		PE0		SCK12			AN016
52	VREFL						
53		P46					AN006
54	VREFH						
55		P44					AN004
56		P43					AN003
57		P42					AN002
58		P41					AN001
59	VREFL0						
60		P40					AN000
61	VREFH0						
62	AVCC0						
63		P05					DA1
64	AVSS0						

Note 1. RX230: PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, PH3/TMCI0
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Table 1.10 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (1/2)

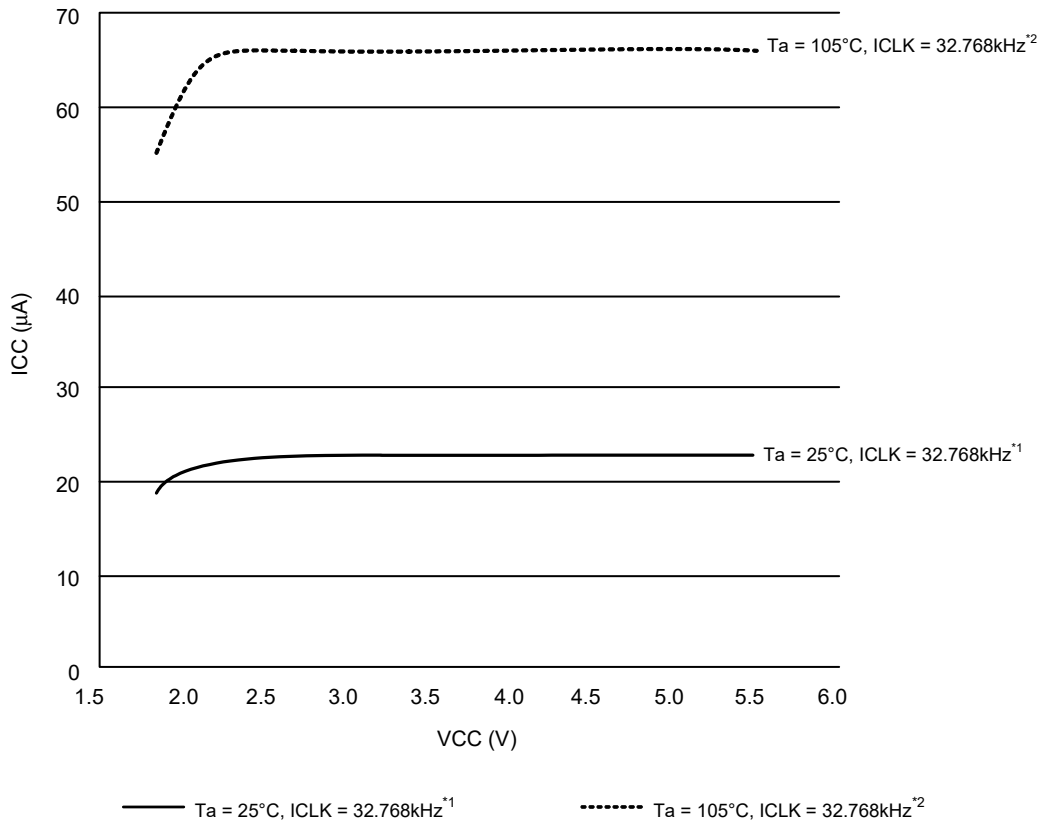
Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
1	VCL						
2	MD						FINED
3	RES#						
4	XTAL	P37					
5	VSS						
6	EXTAL	P36					
7	VCC						
8	UPSEL	P35					NMI
9		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#/SSISCK0			IRQ1
10		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1/ AUDIO_MCLK			IRQ0/CMPOB3
11		P27	MTIOC2B/TMCI3	SCK1/SSIWS0		TS2	CVREFB3
12		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ USB0_VBUSEN/SSIRXD0		TS3	CMPB3
13		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#/TIOCB0/TCLKD	SCK1/MISOA/SDA/ SSITXD0			IRQ7/ CMPOB2
14		P16	MTIOC3C/MTIOC3D/TMO2/ TIOCB1/TCLKC	TXD1/SMOSI1/SSDA1/MOSIA/ SCL/USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB			IRQ6/ADTRG0#
15		P15	MTIOC0B/MTCLKB/TMCI2/ TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/CRXD0		TS12	IRQ5/CMPB2
16		P14	MTIOC3A/MTCLKA/TMRI2/ TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/ USB0_OVRCURA		TS13	IRQ4/CVREFB2
17	VCC_USB*1	PH3*1	TMCI0*1				
18		PH2*1	TMRI0*1	USB0_DM*1			IRQ1*1
19		PH1*1	TMO0*1	USB0_DP*1			IRQ0*1
20	VSS_USB*1	PH0*1					CACREF*1
21	UB	PC7	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA			CACREF
22		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA/ USB0_EXICEN		TS22	
23		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA/USB0_ID		TS23	
24		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0		TSCAP	
25		PB5/PC3	MTIOC2A/MTIOC1B/TMRI1/ POE1#/TIOCB4	USB0_VBUS			
26		PB3/PC2	MTIOC0A/MTIOC4A/TMO0/ POE3#/TIOCD3/TCLKD	SCK6			
27		PB1/PC1	MTIOC0C/MTIOC4C/TMCI0/ TIOCB3	TXD6/SMOSI6/SSDA6			IRQ4/ CMPOB1
28	VCC						
29		PB0/PC0	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/RSPCKA			
30	VSS						
31		PA6	MTIC5V/MTCLKB/TMCI3/POE2#/ TIOCA2	CTS5#/RTS5#/SS5#/MOSIA/ SSIWS0			
32		PA4	MTIC5U/MTCLKA/TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/SSLA0/ SSITXD0/IRTXD5			IRQ5 /CVREFB1
33		PA3	MTIOC0D/MTCLKD/TIOCD0/ TCLKB	RXD5/SMISO5/SSCL5/SSIRXD0/ IRRXD5			IRQ6 /CMPB1
34		PA1	MTIOC0B/MTCLKC/TIOCB0	SCK5/SSLA2/SSISCK0			
35		PE4	MTIOC4D/MTIOC1A				AN020/CMPA2/ CLKOUT
36		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/AUDIO_MCLK			AN019/CLKOUT
37		PE2	MTIOC4A	RXD12/RXDX12/SSCL12			IRQ7/AN018/ CVREFB0
38		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SSDA12			AN017/CMPB0
39	VREFL						
40		P46					AN006
41	VREFH						

Table 4.1 List of I/O Registers (Address Order) (2/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK	
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK	
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK	
0008 2000h	DMAC0	DMA Source Address Register	DMSAR	32	32	2 ICLK	
0008 2004h	DMAC0	DMA Destination Address Register	DMDAR	32	32	2 ICLK	
0008 2008h	DMAC0	DMA Transfer Count Register	DMCRA	32	32	2 ICLK	
0008 200Ch	DMAC0	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK	
0008 2010h	DMAC0	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK	
0008 2013h	DMAC0	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK	
0008 2014h	DMAC0	DMA Address Mode Register	DMAMD	16	16	2 ICLK	
0008 2018h	DMAC0	DMA Offset Register	DMOFR	32	32	2 ICLK	
0008 201Ch	DMAC0	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK	
0008 201Dh	DMAC0	DMA Software Start Register	DMREQ	8	8	2 ICLK	
0008 201Eh	DMAC0	DMA Status Register	DMSTS	8	8	2 ICLK	
0008 201Fh	DMAC0	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK	
0008 2040h	DMAC1	DMA Source Address Register	DMSAR	32	32	2 ICLK	
0008 2044h	DMAC1	DMA Destination Address Register	DMDAR	32	32	2 ICLK	
0008 2048h	DMAC1	DMA Transfer Count Register	DMCRA	32	32	2 ICLK	
0008 204Ch	DMAC1	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK	
0008 2050h	DMAC1	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK	
0008 2053h	DMAC1	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK	
0008 2054h	DMAC1	DMA Address Mode Register	DMAMD	16	16	2 ICLK	
0008 205Ch	DMAC1	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK	
0008 205Dh	DMAC1	DMA Software Start Register	DMREQ	8	8	2 ICLK	
0008 205Eh	DMAC1	DMA Status Register	DMSTS	8	8	2 ICLK	
0008 205Fh	DMAC1	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK	
0008 2080h	DMAC2	DMA Source Address Register	DMSAR	32	32	2 ICLK	
0008 2084h	DMAC2	DMA Destination Address Register	DMDAR	32	32	2 ICLK	
0008 2088h	DMAC2	DMA Transfer Count Register	DMCRA	32	32	2 ICLK	
0008 208Ch	DMAC2	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK	
0008 2090h	DMAC2	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK	
0008 2093h	DMAC2	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK	
0008 2094h	DMAC2	DMA Address Mode Register	DMAMD	16	16	2 ICLK	
0008 209Ch	DMAC2	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK	
0008 209Dh	DMAC2	DMA Software Start Register	DMREQ	8	8	2 ICLK	
0008 209Eh	DMAC2	DMA Status Register	DMSTS	8	8	2 ICLK	
0008 209Fh	DMAC2	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK	
0008 20C0h	DMAC3	DMA Source Address Register	DMSAR	32	32	2 ICLK	
0008 20C4h	DMAC3	DMA Destination Address Register	DMDAR	32	32	2 ICLK	
0008 20C8h	DMAC3	DMA Transfer Count Register	DMCRA	32	32	2 ICLK	
0008 20CCh	DMAC3	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK	
0008 20D0h	DMAC3	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK	
0008 20D3h	DMAC3	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK	
0008 20D4h	DMAC3	DMA Address Mode Register	DMAMD	16	16	2 ICLK	
0008 20DCh	DMAC3	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK	
0008 20DDh	DMAC3	DMA Software Start Register	DMREQ	8	8	2 ICLK	
0008 20DEh	DMAC3	DMA Status Register	DMSTS	8	8	2 ICLK	
0008 20DFh	DMAC3	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK	
0008 2200h	DMAC	DMA Module Activation Register	DMAST	8	8	2 ICLK	
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK	
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK	
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (3/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK	
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK	
0008 3002h	BSC	CS0 Mode Register	CS0MOD	16	16	1 or 2 BCLK	
0008 3004h	BSC	CS0 Wait Control Register 1	CS0WCR1	32	32	1 or 2 BCLK	
0008 3008h	BSC	CS0 Wait Control Register 2	CS0WCR2	32	32	1 or 2 BCLK	
0008 3012h	BSC	CS1 Mode Register	CS1MOD	16	16	1 or 2 BCLK	
0008 3014h	BSC	CS1 Wait Control Register 1	CS1WCR1	32	32	1 or 2 BCLK	
0008 3018h	BSC	CS1 Wait Control Register 2	CS1WCR2	32	32	1 or 2 BCLK	
0008 3022h	BSC	CS2 Mode Register	CS2MOD	16	16	1 or 2 BCLK	
0008 3024h	BSC	CS2 Wait Control Register 1	CS2WCR1	32	32	1 or 2 BCLK	
0008 3028h	BSC	CS2 Wait Control Register 2	CS2WCR2	32	32	1 or 2 BCLK	
0008 3032h	BSC	CS3 Mode Register	CS3MOD	16	16	1 or 2 BCLK	
0008 3034h	BSC	CS3 Wait Control Register 1	CS3WCR1	32	32	1 or 2 BCLK	
0008 3038h	BSC	CS3 Wait Control Register 2	CS3WCR2	32	32	1 or 2 BCLK	
0008 3802h	BSC	CS0 Control Register	CS0CR	16	16	1 or 2 BCLK	
0008 380Ah	BSC	CS0 Recovery Cycle Register	CS0REC	16	16	1 or 2 BCLK	
0008 3812h	BSC	CS1 Control Register	CS1CR	16	16	1 or 2 BCLK	
0008 381Ah	BSC	CS1 Recovery Cycle Register	CS1REC	16	16	1 or 2 BCLK	
0008 3822h	BSC	CS2 Control Register	CS2CR	16	16	1 or 2 BCLK	
0008 382Ah	BSC	CS2 Recovery Cycle Register	CS2REC	16	16	1 or 2 BCLK	
0008 3832h	BSC	CS3 Control Register	CS3CR	16	16	1 or 2 BCLK	
0008 383Ah	BSC	CS3 Recovery Cycle Register	CS3REC	16	16	1 or 2 BCLK	
0008 3880h	BSC	CS Recovery Cycle Insertion Enable Register	CSRECEN	16	16	1 or 2 BCLK	
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK	
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK	
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK	
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK	
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK	
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK	
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK	
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK	
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK	
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK	
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK	
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32	1 ICLK	
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32	1 ICLK	
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32	1 ICLK	
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32	1 ICLK	
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32	1 ICLK	
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32	1 ICLK	
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32	1 ICLK	
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32	1 ICLK	
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32	1 ICLK	
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32	1 ICLK	
0008 6520h	MPU	Region Search Address Register	MPSA	32	32	1 ICLK	
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16	1 ICLK	
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16	1 ICLK	
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32	1 ICLK	
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32	1 ICLK	
0008 7010h to 0008 70FFh	ICU	Interrupt Request Register 016 to Interrupt Request Register 255	IR016 to IR255	8	8	2 ICLK	



Note 1. All peripheral operations except any BGO operation are operating normally. Indicates the average of the typical samples through actual measurement during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. Indicates the average of the upper-limit samples through actual measurement during product evaluation.

Figure 5.3 Voltage Dependency in Low-Speed Operating Mode (Reference Data)

5.2.2 Normal I/O Pin Output Characteristics (2)

Figure 5.13 to Figure 5.17 show the characteristics when high-drive output is selected by the drive capacity control register.

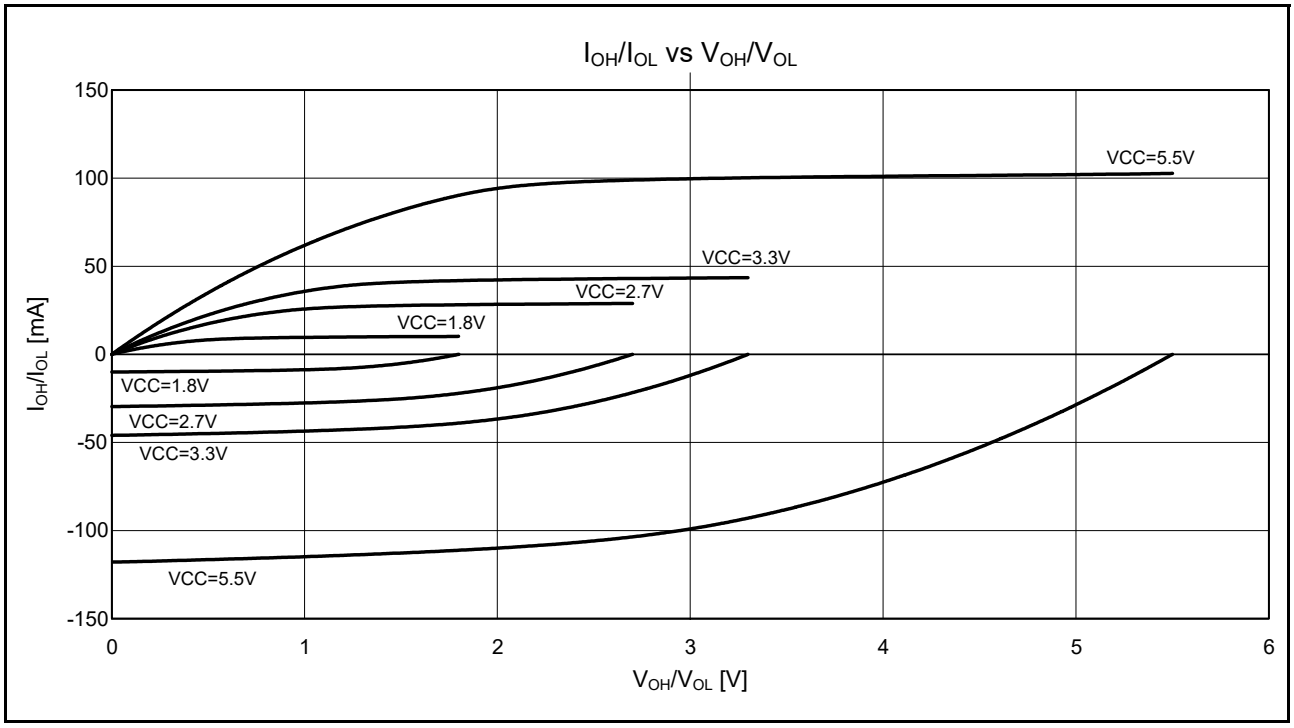


Figure 5.13 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at T_a = 25°C When High-Drive Output is Selected (Reference Data)

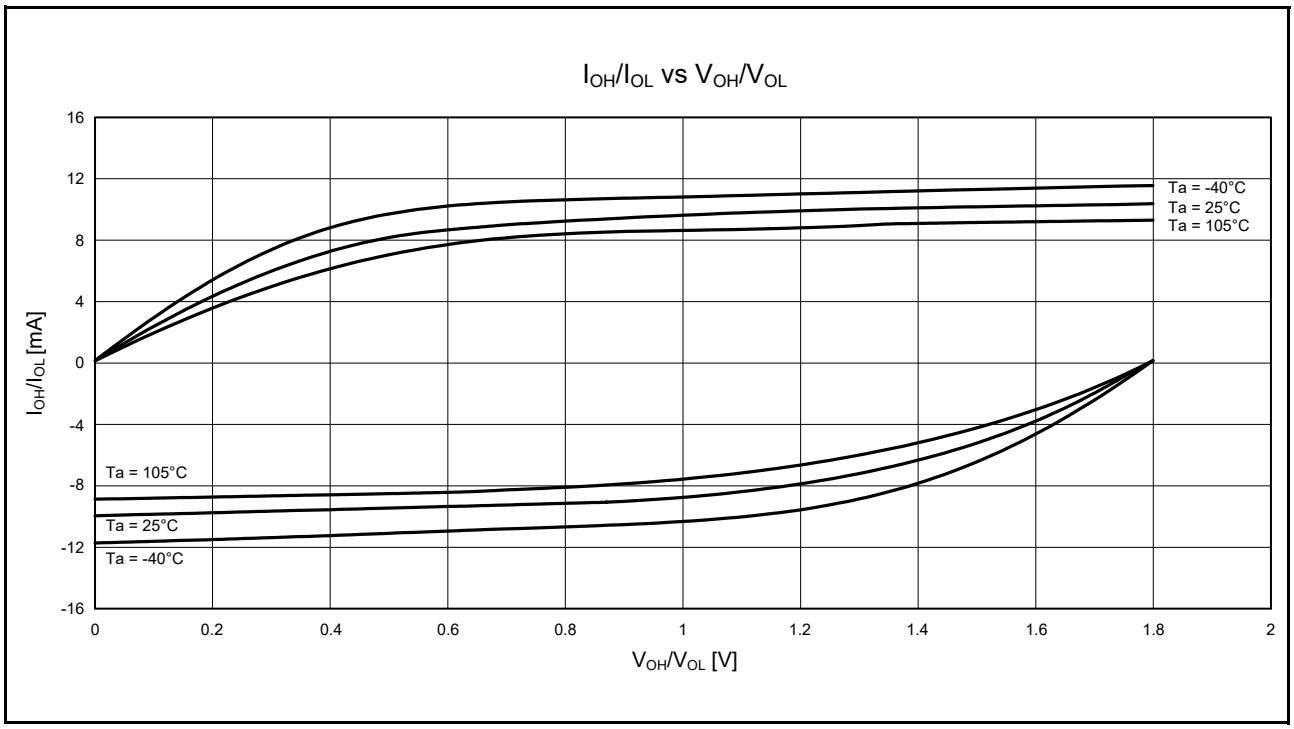


Figure 5.14 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 1.8 V When High-Drive Output is Selected (Reference Data)

5.3.2 Reset Timing

Table 5.27 Reset Timing

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t_{RESWP}	3	—	—	ms	Figure 5.31
	Other than above	t_{RESW}	30	—	—	µs	Figure 5.32
Wait time after RES# cancellation (at power-on)	At normal startup*1	t_{RESWT}	—	8.5	—	ms	Figure 5.31
	During fast startup time*2	t_{RESWT}	—	560	—	µs	
Wait time after RES# cancellation (during powered-on state)		t_{RESWT}	—	120	—	µs	Figure 5.32
Independent watchdog timer reset period		t_{RESWIW}	—	1	—	IWDT clock cycle	Figure 5.33
Watchdog timer reset period		t_{RESWWW}	—	4	—	PCLKB cycle	
Software reset period		t_{RESWSW}	—	1	—	ICLK cycle	
Wait time after independent watchdog timer reset cancellation*3		t_{RESWT2}	—	300	—	µs	
Wait time after watchdog timer reset cancellation*4		t_{RESWT2}	—	300	—	µs	
Wait time after software reset cancellation		t_{RESWT2}	—	170	—	µs	

Note 1. When OFS1.(LVDAS, FASTSTUP) bits are 11b.
Note 2. When OFS1.(LVDAS, FASTSTUP) bits are a value other than 11b.
Note 3. When IWDTCR.CKS[3:0] bits are 0000b.
Note 4. When WDTCR.CKS[3:0] bits are 0001b.

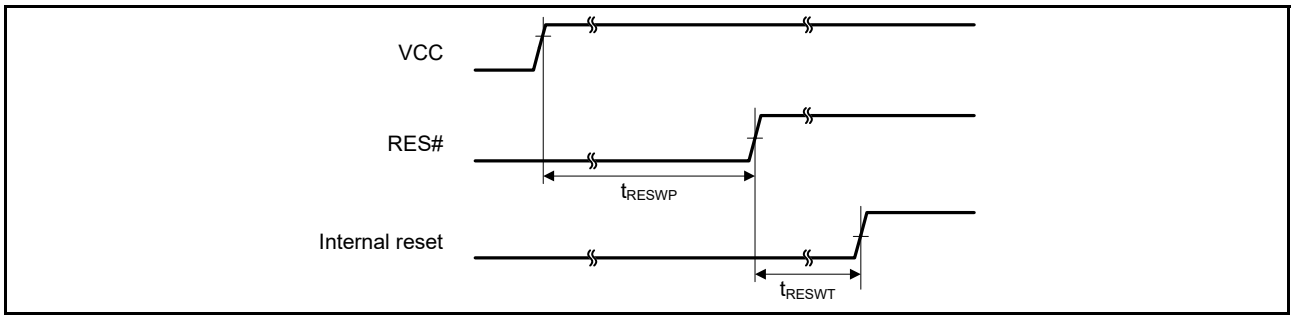


Figure 5.31 Reset Input Timing at Power-On

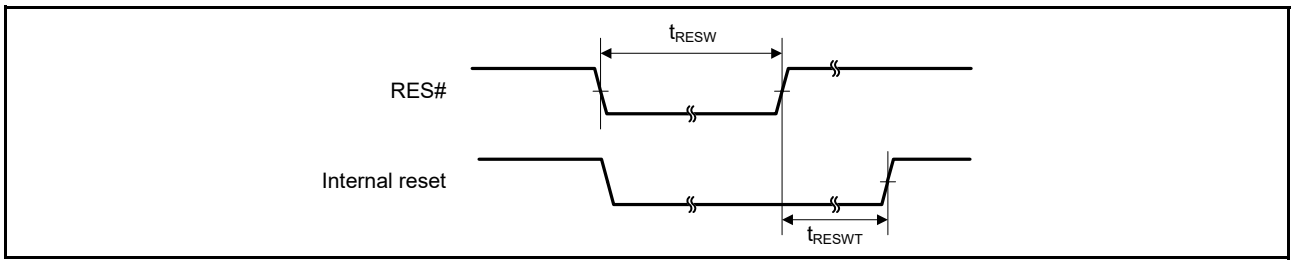


Figure 5.32 Reset Input Timing (1)

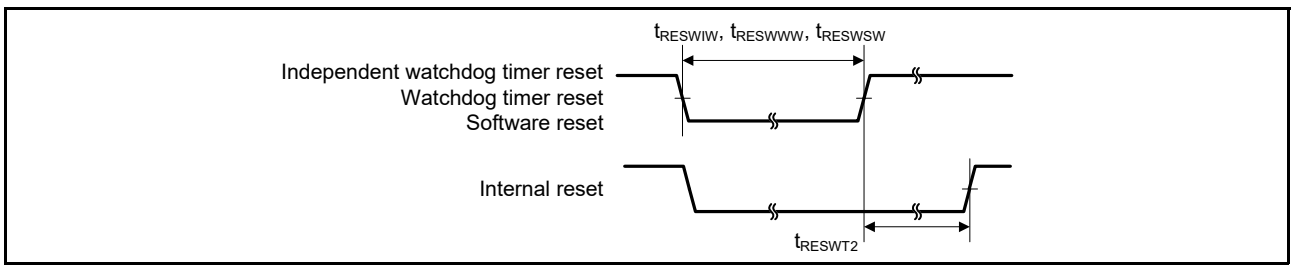


Figure 5.33 Reset Input Timing (2)

5.3.4 Control Signal Timing

Table 5.33 Control Signal Timing

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter is disabled (NMIFLTE.NFLTEN = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		NMI digital filter is enabled (NMIFLTE.NFLTEN = 1)	t_{NMICK} × 3 ≤ 200 ns
		t_{NMICK} × 3.5*2	—	—			t_{NMICK} × 3 > 200 ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter is disabled (IRQFLTE0.FLTENi = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		IRQ digital filter is enabled (IRQFLTE0.FLTENi = 1)	t_{IRQCK} × 3 ≤ 200 ns
		t_{IRQCK} × 3.5*3	—	—			t_{IRQCK} × 3 > 200 ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

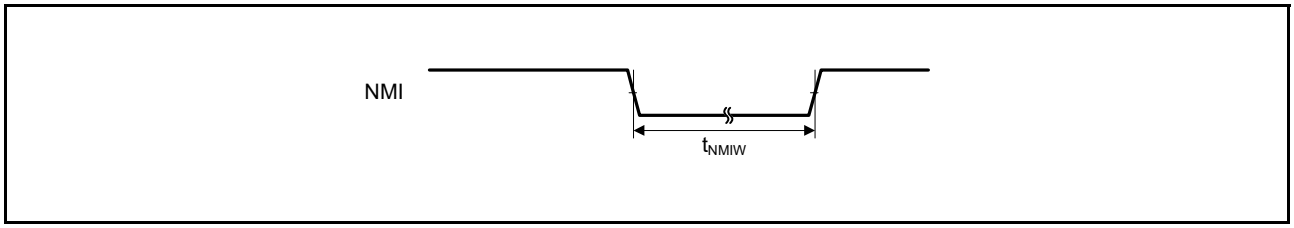


Figure 5.36 NMI Interrupt Input Timing

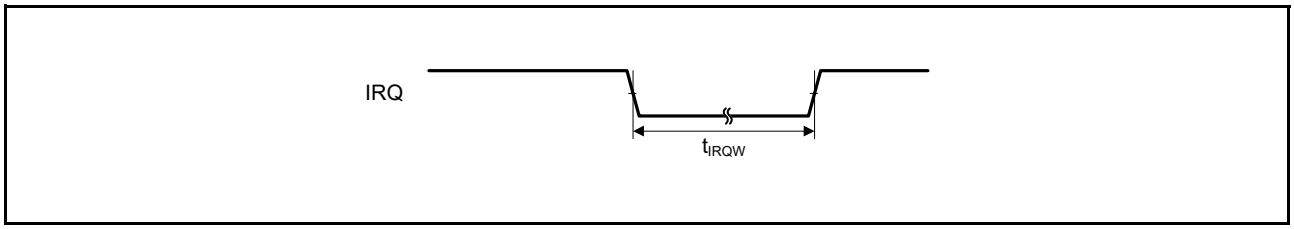


Figure 5.37 IRQ Interrupt Input Timing

Table 5.39 Timing of On-Chip Peripheral Modules (2)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C, C = 30 pF, when high-drive output is selected by the drive capacity control register

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}*1	Figure 5.54
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	2.7 V or above	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	1	µs	
	Data input setup time	Master	2.7 V or above	t_{SU}	10	—	ns	Figure 5.55 to Figure 5.58
			1.8 V or above		30	—		
		Slave			$25 - t_{Pcyc}$	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	$-30 + N^{*2} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	$-30 + N^{*3} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V or above	t_{OD}	—	14	ns	
			1.8 V or above		—	30		
		Slave	2.7 V or above		—	$3 \times t_{Pcyc} + 65$		
			1.8 V or above		—	$3 \times t_{Pcyc} + 105$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	2.7 V or above	t_{Dr}, t_{Df}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	1	µs	
	SSL rise/fall time	Output	2.7 V or above	t_{SSLr}, t_{SSLf}	—	10	ns	
			1.8 V or above		—	15	ns	
		Input			—	1	µs	
	Slave access time		2.7 V or above	t_{SA}	—	6	t_{Pcyc}	Figure 5.57, Figure 5.58
			1.8 V or above		—	7		
	Slave output release time		2.7 V or above	t_{REL}	—	5	t_{Pcyc}	
			1.8 V or above		—	6		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

Table 5.44 Timing of On-Chip Peripheral Modules (7)

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, fPCLKB ≤ 32 MHz,
T_a = –40 to +105°C,
when high-drive output is selected by the drive capacity control register

Item		Symbol	Min.	Max.	Unit	Test Conditions
SDHI	SDHI_CLK pin output cycle time	$t_{PP(SD)}$	62.5	—	ns	Figure 5.64
	SDHI_CLK pin output high pulse width	$t_{WH(SD)}$	18.25	—	ns	
	SDHI_CLK pin output low pulse width	$t_{WL(SD)}$	18.25	—	ns	
	SDHI_CLK pin output rise time	$t_{TLH(SD)}$	—	10	ns	
	SDHI_CLK pin output fall time	$t_{THL(SD)}$	—	10	ns	
	Output data delay time (data transfer mode) for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ODLY(SD)}$	–18.25	18.25	ns	
	Input data setup time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ISU(SD)}$	9.25	—	ns	
	Input data hold time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{IH(SD)}$	8.3	—	ns	

5.5 A/D Conversion Characteristics

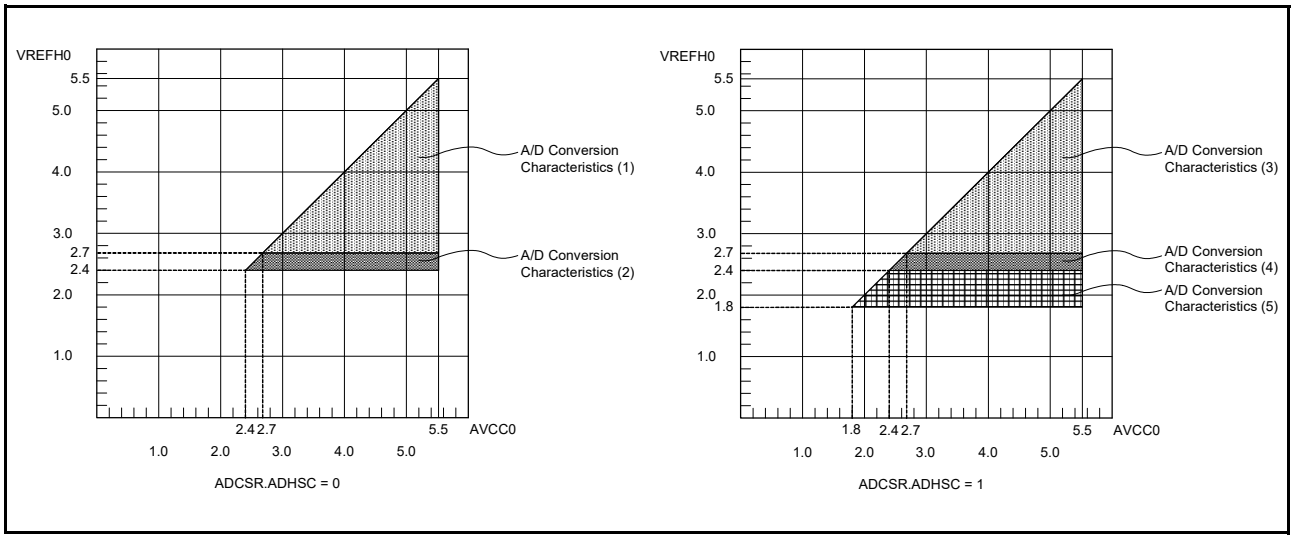


Figure 5.67 VREFH0 Voltage Range vs. AVCC0

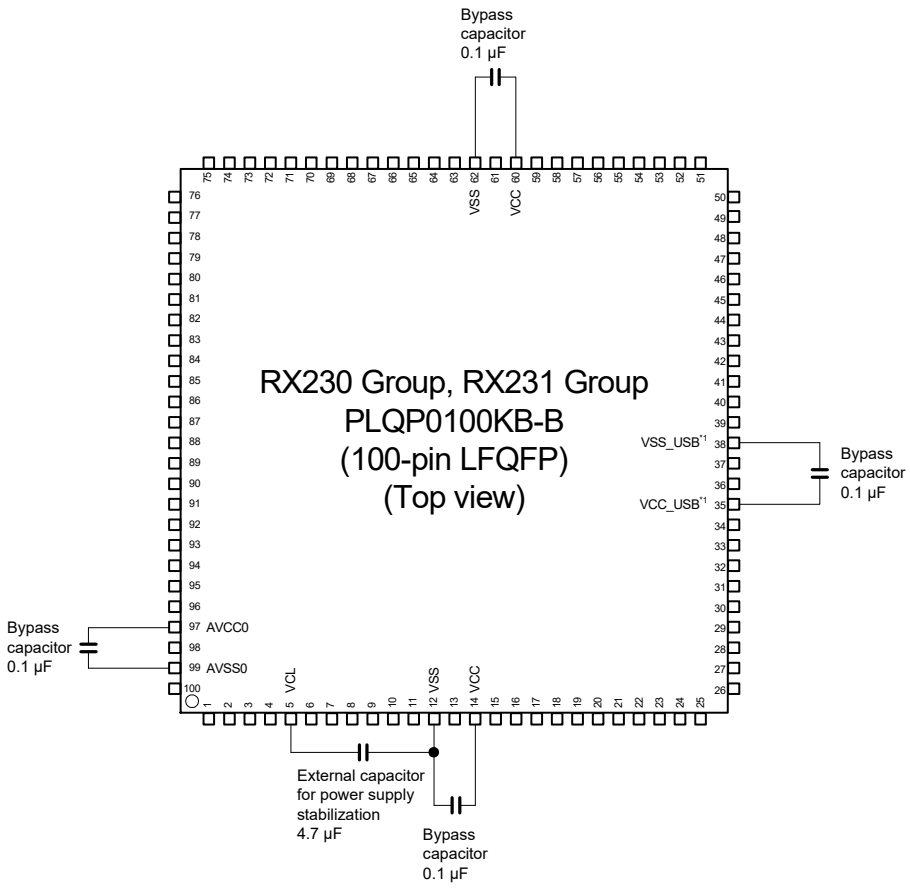
Table 5.46 A/D Conversion Characteristics (1)

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, 2.7 V ≤ VREFH0 ≤ AVCC0, reference voltage = VREFH0 selected, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	54	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 54 MHz)	Permissible signal source impedance (Max.) = 0.3 kΩ	0.83	—	—	µs	High-precision channel The ADCSR.ADHSC bit is 0 The ADSSTRn register is 0Dh
		1.33	—	—		Normal-precision channel The ADCSR.ADHSC bit is 0 The ADSSTRn register is 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 5.68
Analog input resistance	Rs	—	—	2.5	kΩ	Figure 5.68
Analog input voltage range	Ain	0	—	VREFH0	V	
Offset error		—	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		—	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		—	± 0.5	—	LSB	
Absolute accuracy		—	± 1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential non-linearity error		—	±1.0	—	LSB	
INL integral non-linearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

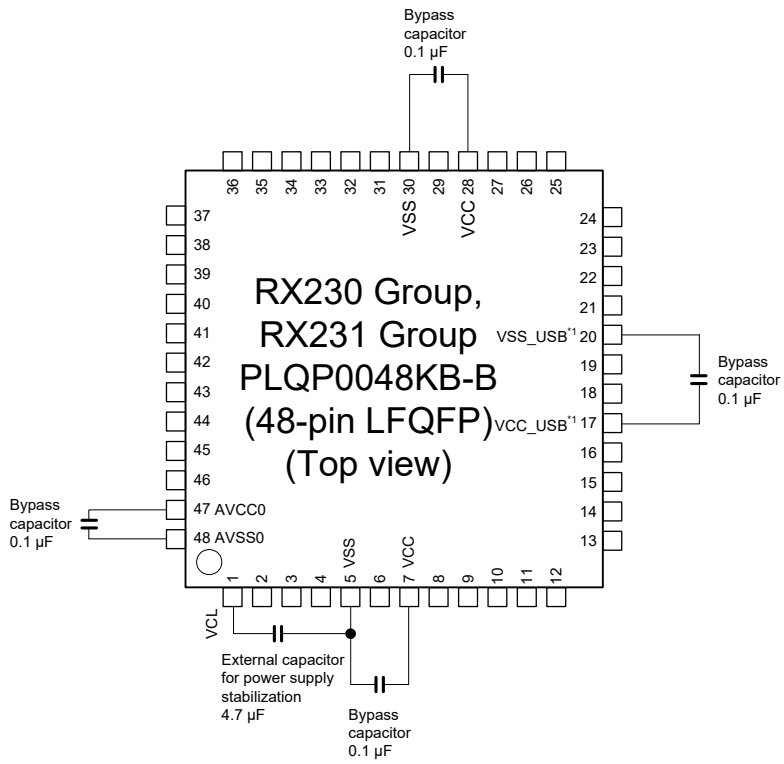
Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.



Note: Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic capacitor for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Note 1. As the products of the RX230 group do not have VCC_USB or VSS_USB, a bypass capacitor is not required.

Figure 5.80 Connecting Capacitors (100 Pins)



Note: Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic capacitor for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Note 1. As the products of the RX230 group do not have VCC_USB or VSS_USB, a bypass capacitor is not required.

Figure 5.82 Connecting Capacitors (48 Pins)

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		Page	Summary	
1.10	Oct 30, 2015	142	Table 5.45 A/D Conversion Characteristics (1): Conditions and Voltage Range of Analog Input (Max.), changed	
		143	Table 5.46 A/D Conversion Characteristics (2): Conditions changed	
		144	Table 5.47 A/D Conversion Characteristics (3): Conditions changed	
		145	Table 5.48 A/D Conversion Characteristics (4): Conditions changed	
		146	Table 5.49 A/D Conversion Characteristics (5): Conditions changed and Absolute accuracy (Test Conditions) deleted	
		153	Table 5.57 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (1), changed	TN-RX*-A137A/E
		154	Table 5.58 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (2), changed	
		155	Figure 5.73 Power-On Reset Timing and Figure 5.74 Voltage Detection Circuit Timing (Vdet0), changed	
		159	Table 5.62 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode: Note changed	
		160	Table 5.63 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating Mode: Note changed	
		161	Table 5.65 E2 DataFlash Characteristics (2): high-speed operating mode, Note changed	
		161	Table 5.66 E2 DataFlash Characteristics (3): middle-speed operating mode, Conditions and Note changed	
		163	Figure 5.79 Connecting Capacitors (100 Pins), changed	
		164	Figure 5.80 Connecting Capacitors (64 Pins), changed	
		165	Figure 5.81 Connecting Capacitors (48 Pins), changed	
		Appendix 1. Package Dimensions		
		167	Figure B 100 -Pin LQFP (PLQP0100KB-B), changed	TN-RX*-A137A/E
		170	Figure E 64 -Pin LQFP (PLQP0064KB-C), changed	TN-RX*-A137A/E
		172	Figure G 48 -Pin LQFP (PLQP0048KB-B), changed	TN-RX*-A137A/E
1.20	Sep 28, 2018	Features		
		1	SD host interface (optional: one channel) SD memory/ SDIO 1-bit or 4-bit SD bus supported, Note deleted	TN-RX*-A145A/E
		1. Overview		
		6	Table 1.2 Comparison of Functions for Different Packages, changed (deletion of IRQ2 on 64-pin package)	
		6	Table 1.2 Comparison of Functions for Different Packages, Note 1 added	TN-RX*-A145A/E
		7	Table 1.3 List of Products: D Version (Ta = –40 to +85°C) (1/2), changed	TN-RX*-A145A/E
		9	Table 1.4 List of Products: G Version (Ta = –40 to +105°C) (1/2), changed	TN-RX*-A145A/E
		11	Figure 1.1 How to Read the Product Part Number, changed	TN-RX*-A145A/E
		16	Table 1.5 Pin Functions (4/4), changed (changes in description for VCC_USB)	TN-RX*-A201A/E
		24	Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (2/3), changed (UPSEL was added to the column of P35)	
		24	Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (2/3), changed (USB0_VBUS was added to the column of PB5)	
		26	Table 1.7 List of Pins and Pin Functions (100-Pin LFQFP) (1/3), changed (UPSEL was added to the column of P35)	
		29	Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (1/2), changed (UPSEL was added to the column of P35)	
		30	Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (2/2), changed (USB0_VBUS was added to the column of PB5)	
		31	Table 1.9 List of Pins and Pin Functions (64-Pin LFQFP/HWQFN) (1/2), changed (UPSEL was added to the column of P35)	
		31	Table 1.9 List of Pins and Pin Functions (64-Pin LQFP/HWQFN) (1/2), changed (USB0_VBUS was added to the column of PB5)	
		33	Table 1.10 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (1/2), changed (UPSEL was added to the column of P35)	
		33	Table 1.10 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (1/2), changed	TN-RX*-A145A/E
		5. Electrical Characteristics		
		92	Table 5.18 Output Values of Voltage (1), changed	TN-RX*-A201A/E
		92	Table 5.19 Output Values of Voltage (2), changed	TN-RX*-A201A/E

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1.20	Sep 28, 2018	95	Figure 5.12 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 5.5 V When Normal Output is Selected (Reference Data), changed	TN-RX*-A201A/E
		124	Table 5.44 Timing of On-Chip Peripheral Modules (7), added	TN-RX*-A197A/E
		131	Figure 5.64 SD Host Interface Input/Output Signal Timing, added	TN-RX*-A197A/E
		132	Table 5.45 USB Characteristics (USB0_DP and USB0_DM Pin Characteristics) conditions, changed	