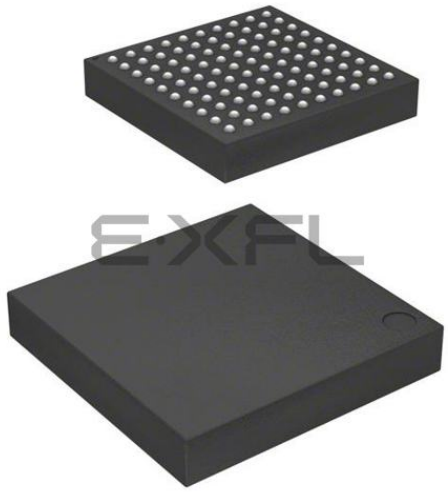
Renesas Electronics America Inc - R5F52306ADLA#20 Datasheet



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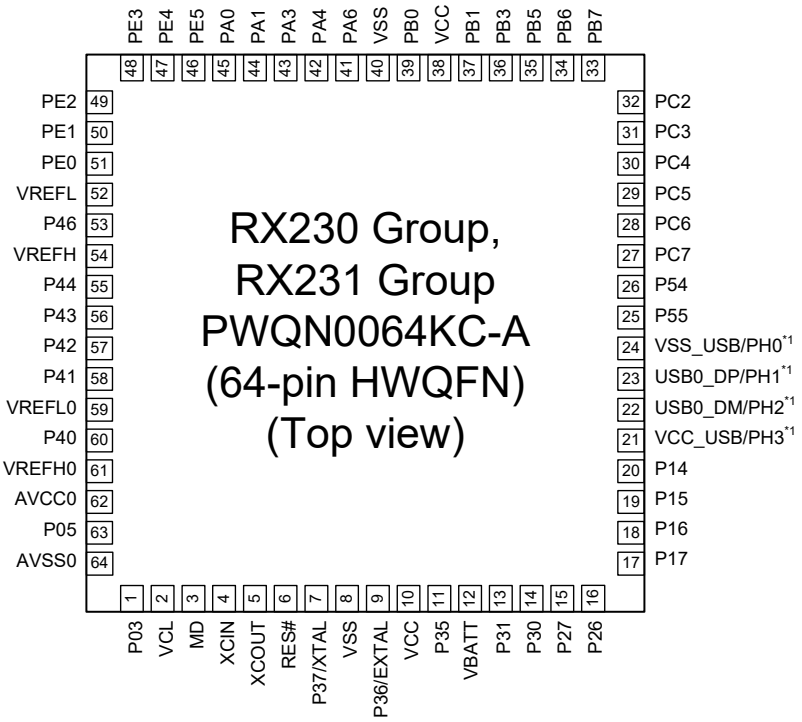
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	EBI/EMI, I²C, IrDA, SCI, SPI, SSI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (5.5x5.5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52306adla-20

Table 1.4 List of Products: G Version (T_a = –40 to +105°C) (1/2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature
RX231	R5F52318AGFP	R5F52318AGFP#30	PLQP0100KB-B	512 Kbytes	64 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Available	–40 to +105°C
	R5F52318BGFP	R5F52318BGFP#30						Available	Available	Available	
	R5F52318AGND	R5F52318AGND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52318BGND	R5F52318BGND#U0						Available	Available	Available	
	R5F52318AGFM	R5F52318AGFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52318BGFM	R5F52318BGFM#30						Available	Available	Available	
	R5F52318AGNE	R5F52318AGNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52318BGNE	R5F52318BGNE#U0						Available	Not available	Available	
	R5F52318AGFL	R5F52318AGFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52318BGFL	R5F52318BGFL#30						Available	Not available	Available	
	R5F52317AGFP	R5F52317AGFP#30	PLQP0100KB-B	384 Kbytes				Not available	Not available	Available	
	R5F52317BGFP	R5F52317BGFP#30						Available	Available	Available	
	R5F52317AGND	R5F52317AGND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52317BGND	R5F52317BGND#U0						Available	Available	Available	
	R5F52317AGFM	R5F52317AGFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52317BGFM	R5F52317BGFM#30						Available	Available	Available	
	R5F52317AGNE	R5F52317AGNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52317BGNE	R5F52317BGNE#U0						Available	Not available	Available	
	R5F52317AGFL	R5F52317AGFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52317BGFL	R5F52317BGFL#30						Available	Not available	Available	
	R5F52316AGFP	R5F52316AGFP#30	PLQP0100KB-B	256 Kbytes	32 Kbytes			Not available	Not available	Available	
	R5F52316CGFP	R5F52316CGFP#30						Not available	Not available	Not available	
	R5F52316AGND	R5F52316AGND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52316CGND	R5F52316CGND#U0						Not available	Not available	Not available	
	R5F52316AGFM	R5F52316AGFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52316CGFM	R5F52316CGFM#30						Not available	Not available	Not available	
	R5F52316AGNE	R5F52316AGNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52316CGNE	R5F52316CGNE#U0						Not available	Not available	Not available	
	R5F52316AGFL	R5F52316AGFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52316CGFL	R5F52316CGFL#30						Not available	Not available	Not available	
	R5F52315AGFP	R5F52315AGFP#30	PLQP0100KB-B	128 Kbytes				Not available	Not available	Available	
	R5F52315CGFP	R5F52315CGFP#30						Not available	Not available	Not available	
	R5F52315AGND	R5F52315AGND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52315CGND	R5F52315CGND#U0						Not available	Not available	Not available	
	R5F52315AGFM	R5F52315AGFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52315CGFM	R5F52315CGFM#30						Not available	Not available	Not available	
	R5F52315AGNE	R5F52315AGNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52315CGNE	R5F52315CGNE#U0						Not available	Not available	Not available	



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin LFQFP/HWQFN)”.
Note: It is recommended to connect an exposed die pad to VSS.

Note 1. RX230: PH0, PH1, PH2, PH3
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Figure 1.6 Pin Assignments of the 64-Pin HWQFN

(9) Floating-point status word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

2.3 Accumulator

The accumulator (ACC0 or ACC1) is a 72-bit register used for DSP instructions. The accumulator is handled as a 96-bit register for reading and writing. At this time, when bits 95 to 72 of the accumulator are read, the value where the value of bit 71 is sign extended is read. Writing to bits 95 to 72 of the accumulator is ignored. ACC0 is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in ACC0 is modified by execution of the instruction.
Use the MVTACGU, MVTACHI, and MVTACLO instructions for writing to the accumulator. The MVTACGU, MVTACHI, and MVTACLO instructions write data to bits 95 to 64, the higher-order 32 bits (bits 63 to 32), and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions for reading data from the accumulator. The MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions read data from the guard bits (bits 95 to 64), higher-order 32 bits (bits 63 to 32), the middle 32 bits (bits 47 to 16), and the lower-order 32 bits (bits 31 to 0), respectively.

Table 4.1 List of I/O Registers (Address Order) (17/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 C0A4h	PORTJ	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C0C0h	PORT0	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0C1h	PORT1	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0C2h	PORT2	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0C3h	PORT3	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0C4h	PORT4	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0C5h	PORT5	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0CAh	PORTA	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0CBh	PORTB	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0CCh	PORTC	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0CDh	PORTD	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0CEh	PORTE	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0D1h	PORTH	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0D2h	PORTJ	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0E1h	PORT1	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0E2h	PORT2	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0E3h	PORT3	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0E5h	PORT5	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0EAh	PORTA	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0EBh	PORTB	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0ECh	PORTC	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0EDh	PORTD	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0EEh	PORTE	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0F1h	PORTH	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0F2h	PORTJ	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C100h	MPC	CS Output Enable Register	PFCSE	8	8	2 or 3 PCLKB	2 ICLK
0008 C104h	MPC	Address Output Enable Register 0	PFAOE0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C105h	MPC	Address Output Enable Register 1	PFAOE1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C106h	MPC	External Bus Control Register 0	PFBCR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C107h	MPC	External Bus Control Register 1	PFBCR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2 or 3 PCLKB	2 ICLK
0008 C120h	PORT	Port Switching Register B	PSRB	8	8	2 or 3 PCLKB	2 ICLK
0008 C121h	PORT	Port Switching Register A	PSRA	8	8	2 or 3 PCLKB	2 ICLK
0008 C143h	MPC	P03 Pin Function Control Register	P03PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C145h	MPC	P05 Pin Function Control Register	P05PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C147h	MPC	P07 Pin Function Control Register	P07PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C14Ah	MPC	P12 Pin Function Control Register	P12PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C14Bh	MPC	P13 Pin Function Control Register	P13PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C14Ch	MPC	P14 Pin Function Control Register	P14PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C14Dh	MPC	P15 Pin Function Control Register	P15PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C14Eh	MPC	P16 Pin Function Control Register	P16PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C14Fh	MPC	P17 Pin Function Control Register	P17PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C150h	MPC	P20 Pin Function Control Register	P20PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C151h	MPC	P21 Pin Function Control Register	P21PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C152h	MPC	P22 Pin Function Control Register	P22PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C153h	MPC	P23 Pin Function Control Register	P23PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C154h	MPC	P24 Pin Function Control Register	P24PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C155h	MPC	P25 Pin Function Control Register	P25PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C156h	MPC	P26 Pin Function Control Register	P26PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C157h	MPC	P27 Pin Function Control Register	P27PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C158h	MPC	P30 Pin Function Control Register	P30PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C159h	MPC	P31 Pin Function Control Register	P31PFS	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (23/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
000A 00B0h	USB0	BC Control Register 0	USBBCCTRL0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00CCh	USB0	USB Module Control Register	USBMC	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00D0h	USB0	Device Address 0 Configuration Register	DEVADD0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00D2h	USB0	Device Address 1 Configuration Register	DEVADD1	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00D4h	USB0	Device Address 2 Configuration Register	DEVADD2	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00D6h	USB0	Device Address 3 Configuration Register	DEVADD3	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00D8h	USB0	Device Address 4 Configuration Register	DEVADD4	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00DAh	USB0	Device Address 5 Configuration Register	DEVADD5	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0900h	CTSU	CTSU Control Register 0	CTSUCR0	8	8	2 or 3 PCLKB	2 ICLK
000A 0901h	CTSU	CTSU Control Register 1	CTSUCR1	8	8	2 or 3 PCLKB	2 ICLK
000A 0902h	CTSU	CTSU Synchronous Noise Reduction Setting Register	CTSUSDPRS	8	8	2 or 3 PCLKB	2 ICLK
000A 0903h	CTSU	CTSU Sensor Stabilization Wait Control Register	CTSUSST	8	8	2 or 3 PCLKB	2 ICLK
000A 0904h	CTSU	CTSU Measurement Channel Register 0	CTSUMCH0	8	8	2 or 3 PCLKB	2 ICLK
000A 0905h	CTSU	CTSU Measurement Channel Register 1	CTSUMCH1	8	8	2 or 3 PCLKB	2 ICLK
000A 0906h	CTSU	CTSU Channel Enable Control Register 0	CTSUCHAC0	8	8	2 or 3 PCLKB	2 ICLK
000A 0907h	CTSU	CTSU Channel Enable Control Register 1	CTSUCHAC1	8	8	2 or 3 PCLKB	2 ICLK
000A 0908h	CTSU	CTSU Channel Enable Control Register 2	CTSUCHAC2	8	8	2 or 3 PCLKB	2 ICLK
000A 0909h	CTSU	CTSU Channel Enable Control Register 3	CTSUCHAC3	8	8	2 or 3 PCLKB	2 ICLK
000A 090Ah	CTSU	CTSU Channel Enable Control Register 4	CTSUCHAC4	8	8	2 or 3 PCLKB	2 ICLK
000A 090Bh	CTSU	CTSU Channel Transmit/Receive Control Register 0	CTSUCHTRC0	8	8	2 or 3 PCLKB	2 ICLK
000A 090Ch	CTSU	CTSU Channel Transmit/Receive Control Register 1	CTSUCHTRC1	8	8	2 or 3 PCLKB	2 ICLK
000A 090Dh	CTSU	CTSU Channel Transmit/Receive Control Register 2	CTSUCHTRC2	8	8	2 or 3 PCLKB	2 ICLK
000A 090Eh	CTSU	CTSU Channel Transmit/Receive Control Register 3	CTSUCHTRC3	8	8	2 or 3 PCLKB	2 ICLK
000A 090Fh	CTSU	CTSU Channel Transmit/Receive Control Register 4	CTSUCHTRC4	8	8	2 or 3 PCLKB	2 ICLK
000A 0910h	CTSU	CTSU High-Pass Noise Reduction Control Register	CTSUDCLKC	8	8	2 or 3 PCLKB	2 ICLK
000A 0911h	CTSU	CTSU Status Register	CTSUST	8	8	2 or 3 PCLKB	2 ICLK
000A 0912h	CTSU	CTSU High-Pass Noise Reduction Spectrum Diffusion Control Register	CTSUSSC	16	16	2 or 3 PCLKB	2 ICLK
000A 0914h	CTSU	CTSU Sensor Offset Register 0	CTSUSO0	16	16	2 or 3 PCLKB	2 ICLK
000A 0916h	CTSU	CTSU Sensor Offset Register 1	CTSUSO1	16	16	2 or 3 PCLKB	2 ICLK
000A 0918h	CTSU	CTSU Sensor Counter	CTSUSC	16	16	2 or 3 PCLKB	2 ICLK
000A 091Ah	CTSU	CTSU Reference Counter	CTSURC	16	16	2 or 3 PCLKB	2 ICLK
000A 091Ch	CTSU	CTSU Error Status Register	CTSUERRS	16	16	2 or 3 PCLKB	2 ICLK
000A 8300h	RSCAN0	Bit Configuration Register L	CFGL	16	16	2 or 3 PCLKB	2 ICLK
000A 8302h	RSCAN0	Bit Configuration Register H	CFGH	16	16	2 or 3 PCLKB	2 ICLK
000A 8304h	RSCAN0	Control Register L	CTRL	16	16	2 or 3 PCLKB	2 ICLK
000A 8306h	RSCAN0	Control Register H	CTRH	16	16	2 or 3 PCLKB	2 ICLK
000A 8308h	RSCAN0	Status Register L	STSL	16	16	2 or 3 PCLKB	2 ICLK
000A 830Ah	RSCAN0	Status Register H	STSH	16	16	2 or 3 PCLKB	2 ICLK
000A 830Ch	RSCAN0	Error Flag Register L	ERFLL	16	16	2 or 3 PCLKB	2 ICLK
000A 830Eh	RSCAN0	Error Flag Register H	ERFLH	16	16	2 or 3 PCLKB	2 ICLK
000A 8322h	RSCAN	Global Configuration Register L	GCFGL	16	16	2 or 3 PCLKB	2 ICLK
000A 8324h	RSCAN	Global Configuration Register H	GCFGH	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (24/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
000A 8326h	RSCAN	Global Control Register L	GCTRL	16	16	2 or 3 PCLKB	2 ICLK
000A 8328h	RSCAN	Global Control Register H	GCTRH	16	16	2 or 3 PCLKB	2 ICLK
000A 832Ah	RSCAN	Global Status Register	GSTS	16	16	2 or 3 PCLKB	2 ICLK
000A 832Ch	RSCAN	Global Error Flag Register	GERFLL	8	8	2 or 3 PCLKB	2 ICLK
000A 832Eh	RSCAN	Timestamp Register	GTSC	16	16	2 or 3 PCLKB	2 ICLK
000A 8330h	RSCAN	Receive Rule Number Configuration Register	GAFLCFG	16	16	2 or 3 PCLKB	2 ICLK
000A 8332h	RSCAN	Receive Buffer Number Configuration Register	RMNB	16	16	2 or 3 PCLKB	2 ICLK
000A 8334h	RSCAN	Receive Buffer Receive Complete Flag Register	RMND0	16	16	2 or 3 PCLKB	2 ICLK
000A 8338h	RSCAN	Receive FIFO Control Register 0	RFCC0	16	16	2 or 3 PCLKB	2 ICLK
000A 833Ah	RSCAN	Receive FIFO Control Register 1	RFCC1	16	16	2 or 3 PCLKB	2 ICLK
000A 8340h	RSCAN	Receive FIFO Status Register 0	RFSTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 8342h	RSCAN	Receive FIFO Status Register 1	RFSTS1	16	16	2 or 3 PCLKB	2 ICLK
000A 8348h	RSCAN	Receive FIFO Pointer Control Register 0	RFPCTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 834Ah	RSCAN	Receive FIFO Pointer Control Register 1	RFPCTR1	16	16	2 or 3 PCLKB	2 ICLK
000A 8350h	RSCAN0	Transmit/Receive FIFO Control Register 0L	CFCCL0	16	16	2 or 3 PCLKB	2 ICLK
000A 8352h	RSCAN0	Transmit/Receive FIFO Control Register 0H	CFCCH0	16	16	2 or 3 PCLKB	2 ICLK
000A 8358h	RSCAN0	Transmit/Receive FIFO Status Register 0	CFSTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 835Ch	RSCAN0	Transmit/Receive FIFO Pointer Control Register 0	CFPCTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 8360h	RSCAN	Receive FIFO Message Lost Status Register	RFMSTS	8	8	2 or 3 PCLKB	2 ICLK
000A 8361h	RSCAN0	Transmit/Receive FIFO Message Lost Status Register	CFMSTS	8	8	2 or 3 PCLKB	2 ICLK
000A 8362h	RSCAN	Receive FIFO Interrupt Status Register	RFISTS	8	8	2 or 3 PCLKB	2 ICLK
000A 8363h	RSCAN	Transmit/Receive FIFO Receive Interrupt Status Register	CFISTS	8	8	2 or 3 PCLKB	2 ICLK
000A 8364h	RSCAN0	Transmit Buffer Control Register 0	TMC0	8	8	2 or 3 PCLKB	2 ICLK
000A 8365h	RSCAN0	Transmit Buffer Control Register 1	TMC1	8	8	2 or 3 PCLKB	2 ICLK
000A 8366h	RSCAN0	Transmit Buffer Control Register 2	TMC2	8	8	2 or 3 PCLKB	2 ICLK
000A 8367h	RSCAN0	Transmit Buffer Control Register 3	TMC3	8	8	2 or 3 PCLKB	2 ICLK
000A 836Ch	RSCAN0	Transmit Buffer Status Register 0	TMSTS0	8	8	2 or 3 PCLKB	2 ICLK
000A 836Dh	RSCAN0	Transmit Buffer Status Register 1	TMSTS1	8	8	2 or 3 PCLKB	2 ICLK
000A 836Eh	RSCAN0	Transmit Buffer Status Register 2	TMSTS2	8	8	2 or 3 PCLKB	2 ICLK
000A 836Fh	RSCAN0	Transmit Buffer Status Register 3	TMSTS3	8	8	2 or 3 PCLKB	2 ICLK
000A 8374h	RSCAN0	Transmit Buffer Transmit Request Status Register	TMTRSTS	16	16	2 or 3 PCLKB	2 ICLK
000A 8376h	RSCAN0	Transmit Buffer Transmit Complete Status Register	TMTCSTS	16	16	2 or 3 PCLKB	2 ICLK
000A 8378h	RSCAN0	Transmit Buffer Transmit Abort Status Register	TMTASTS	16	16	2 or 3 PCLKB	2 ICLK
000A 837Ah	RSCAN0	Transmit Buffer Interrupt Enable Register	TMIEC	16	16	2 or 3 PCLKB	2 ICLK
000A 837Ch	RSCAN0	Transmit History Buffer Control Register	THLCC0	16	16	2 or 3 PCLKB	2 ICLK
000A 8380h	RSCAN0	Transmit History Buffer Status Register	THLSTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 8384h	RSCAN0	Transmit History Buffer Pointer Control Register	THLPCTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 8388h	RSCAN	Global Transmit Interrupt Status Register	GTINTSTS	16	16	2 or 3 PCLKB	2 ICLK
000A 838Ah	RSCAN	Global RAM Window Control Register	GRWCR	16	16	2 or 3 PCLKB	2 ICLK
000A 838Ch	RSCAN	Global Test Configuration Register	GTSTCFG	16	16	2 or 3 PCLKB	2 ICLK
000A 838Eh	RSCAN	Global Test Control Register	GTSTCTRL	16	16	2 or 3 PCLKB	2 ICLK
000A 8394h	RSCAN	Global Test Protection Unlock Register	GLOCKK	16	16	2 or 3 PCLKB	2 ICLK
000A 83A0h	RSCAN	Receive Rule Entry Register 0AL	GAFLIDL0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A0h	RSCAN	Receive Buffer Register 0AL	RMIDL0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A2h	RSCAN	Receive Rule Entry Register 0AH	GAFLIDH0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A2h	RSCAN	Receive Buffer Register 0AH	RMIDH0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A4h	RSCAN	Receive Rule Entry Register 0BL	GAFLML0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A4h	RSCAN	Receive Buffer Register 0BL	RMTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A6h	RSCAN	Receive Rule Entry Register 0BH	GAFLMH0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A6h	RSCAN	Receive Buffer Register 0BH	RMPTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A8h	RSCAN	Receive Rule Entry Register 0CL	GAFLPL0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A8h	RSCAN	Receive Buffer Register 0CL	RMDF00	16	16	2 or 3 PCLKB	2 ICLK

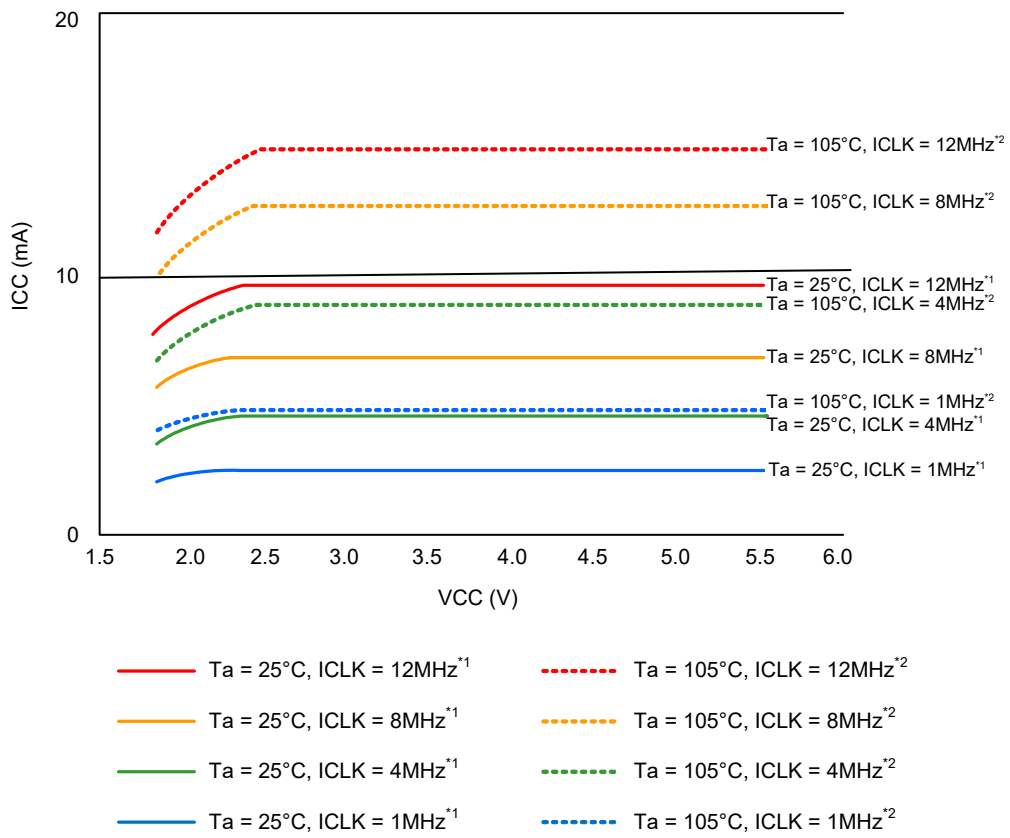
Table 4.1 List of I/O Registers (Address Order) (28/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
000A 8446h	RSCAN	Receive Rule Entry Register 13CH	GAFLPH13	16	16	2 or 3 PCLKB	2 ICLK
000A 8446h	RSCAN	Receive Buffer Register 10BH	RMPTR10	16	16	2 or 3 PCLKB	2 ICLK
000A 8448h	RSCAN	Receive Rule Entry Register 14AL	GAFLIDL14	16	16	2 or 3 PCLKB	2 ICLK
000A 8448h	RSCAN	Receive Buffer Register 10CL	RMDF010	16	16	2 or 3 PCLKB	2 ICLK
000A 844Ah	RSCAN	Receive Rule Entry Register 14AH	GAFLIDH14	16	16	2 or 3 PCLKB	2 ICLK
000A 844Ah	RSCAN	Receive Buffer Register 10CH	RMDF110	16	16	2 or 3 PCLKB	2 ICLK
000A 844Ch	RSCAN	Receive Rule Entry Register 14BL	GAFLML14	16	16	2 or 3 PCLKB	2 ICLK
000A 844Ch	RSCAN	Receive Buffer Register 10DL	RMDF210	16	16	2 or 3 PCLKB	2 ICLK
000A 844Eh	RSCAN	Receive Rule Entry Register 14BH	GAFLMH14	16	16	2 or 3 PCLKB	2 ICLK
000A 844Eh	RSCAN	Receive Buffer Register 10DH	RMDF310	16	16	2 or 3 PCLKB	2 ICLK
000A 8450h	RSCAN	Receive Rule Entry Register 14CL	GAFLPL14	16	16	2 or 3 PCLKB	2 ICLK
000A 8450h	RSCAN	Receive Buffer Register 11AL	RMIDL11	16	16	2 or 3 PCLKB	2 ICLK
000A 8452h	RSCAN	Receive Rule Entry Register 14CH	GAFLPH14	16	16	2 or 3 PCLKB	2 ICLK
000A 8452h	RSCAN	Receive Buffer Register 11AH	RMIDH11	16	16	2 or 3 PCLKB	2 ICLK
000A 8454h	RSCAN	Receive Rule Entry Register 15AL	GAFLIDL15	16	16	2 or 3 PCLKB	2 ICLK
000A 8454h	RSCAN	Receive Buffer Register 11BL	RMTS11	16	16	2 or 3 PCLKB	2 ICLK
000A 8456h	RSCAN	Receive Rule Entry Register 15AH	GAFLIDH15	16	16	2 or 3 PCLKB	2 ICLK
000A 8456h	RSCAN	Receive Buffer Register 11BH	RMPTR11	16	16	2 or 3 PCLKB	2 ICLK
000A 8458h	RSCAN	Receive Rule Entry Register 15BL	GAFLML15	16	16	2 or 3 PCLKB	2 ICLK
000A 8458h	RSCAN	Receive Buffer Register 11CL	RMDF011	16	16	2 or 3 PCLKB	2 ICLK
000A 845Ah	RSCAN	Receive Rule Entry Register 15BH	GAFLMH15	16	16	2 or 3 PCLKB	2 ICLK
000A 845Ah	RSCAN	Receive Buffer Register 11CH	RMDF111	16	16	2 or 3 PCLKB	2 ICLK
000A 845Ch	RSCAN	Receive Rule Entry Register 15CL	GAFLPL15	16	16	2 or 3 PCLKB	2 ICLK
000A 845Ch	RSCAN	Receive Buffer Register 11DL	RMDF211	16	16	2 or 3 PCLKB	2 ICLK
000A 845Eh	RSCAN	Receive Rule Entry Register 15CH	GAFLPH15	16	16	2 or 3 PCLKB	2 ICLK
000A 845Eh	RSCAN	Receive Buffer Register 11DH	RMDF311	16	16	2 or 3 PCLKB	2 ICLK
000A 8460h	RSCAN	Receive Buffer Register 12AL	RMIDL12	16	16	2 or 3 PCLKB	2 ICLK
000A 8462h	RSCAN	Receive Buffer Register 12AH	RMIDH12	16	16	2 or 3 PCLKB	2 ICLK
000A 8464h	RSCAN	Receive Buffer Register 12BL	RMTS12	16	16	2 or 3 PCLKB	2 ICLK
000A 8466h	RSCAN	Receive Buffer Register 12BH	RMPTR12	16	16	2 or 3 PCLKB	2 ICLK
000A 8468h	RSCAN	Receive Buffer Register 12CL	RMDF012	16	16	2 or 3 PCLKB	2 ICLK
000A 846Ah	RSCAN	Receive Buffer Register 12CH	RMDF112	16	16	2 or 3 PCLKB	2 ICLK
000A 846Ch	RSCAN	Receive Buffer Register 12DL	RMDF212	16	16	2 or 3 PCLKB	2 ICLK
000A 846Eh	RSCAN	Receive Buffer Register 12DH	RMDF312	16	16	2 or 3 PCLKB	2 ICLK
000A 8470h	RSCAN	Receive Buffer Register 13AL	RMIDL13	16	16	2 or 3 PCLKB	2 ICLK
000A 8472h	RSCAN	Receive Buffer Register 13AH	RMIDH13	16	16	2 or 3 PCLKB	2 ICLK
000A 8474h	RSCAN	Receive Buffer Register 13BL	RMTS13	16	16	2 or 3 PCLKB	2 ICLK
000A 8476h	RSCAN	Receive Buffer Register 13BH	RMPTR13	16	16	2 or 3 PCLKB	2 ICLK
000A 8478h	RSCAN	Receive Buffer Register 13CL	RMDF013	16	16	2 or 3 PCLKB	2 ICLK
000A 847Ah	RSCAN	Receive Buffer Register 13CH	RMDF113	16	16	2 or 3 PCLKB	2 ICLK
000A 847Ch	RSCAN	Receive Buffer Register 13DL	RMDF213	16	16	2 or 3 PCLKB	2 ICLK
000A 847Eh	RSCAN	Receive Buffer Register 13DH	RMDF313	16	16	2 or 3 PCLKB	2 ICLK
000A 8480h	RSCAN	Receive Buffer Register 14AL	RMIDL14	16	16	2 or 3 PCLKB	2 ICLK
000A 8482h	RSCAN	Receive Buffer Register 14AH	RMIDH14	16	16	2 or 3 PCLKB	2 ICLK
000A 8484h	RSCAN	Receive Buffer Register 14BL	RMTS14	16	16	2 or 3 PCLKB	2 ICLK
000A 8486h	RSCAN	Receive Buffer Register 14BH	RMPTR14	16	16	2 or 3 PCLKB	2 ICLK
000A 8488h	RSCAN	Receive Buffer Register 14CL	RMDF014	16	16	2 or 3 PCLKB	2 ICLK
000A 848Ah	RSCAN	Receive Buffer Register 14CH	RMDF114	16	16	2 or 3 PCLKB	2 ICLK
000A 848Ch	RSCAN	Receive Buffer Register 14DL	RMDF214	16	16	2 or 3 PCLKB	2 ICLK
000A 848Eh	RSCAN	Receive Buffer Register 14DH	RMDF314	16	16	2 or 3 PCLKB	2 ICLK
000A 8490h	RSCAN	Receive Buffer Register 15AL	RMIDL15	16	16	2 or 3 PCLKB	2 ICLK
000A 8492h	RSCAN	Receive Buffer Register 15AH	RMIDH15	16	16	2 or 3 PCLKB	2 ICLK

Table 5.2 Recommended Operating Voltage Conditions

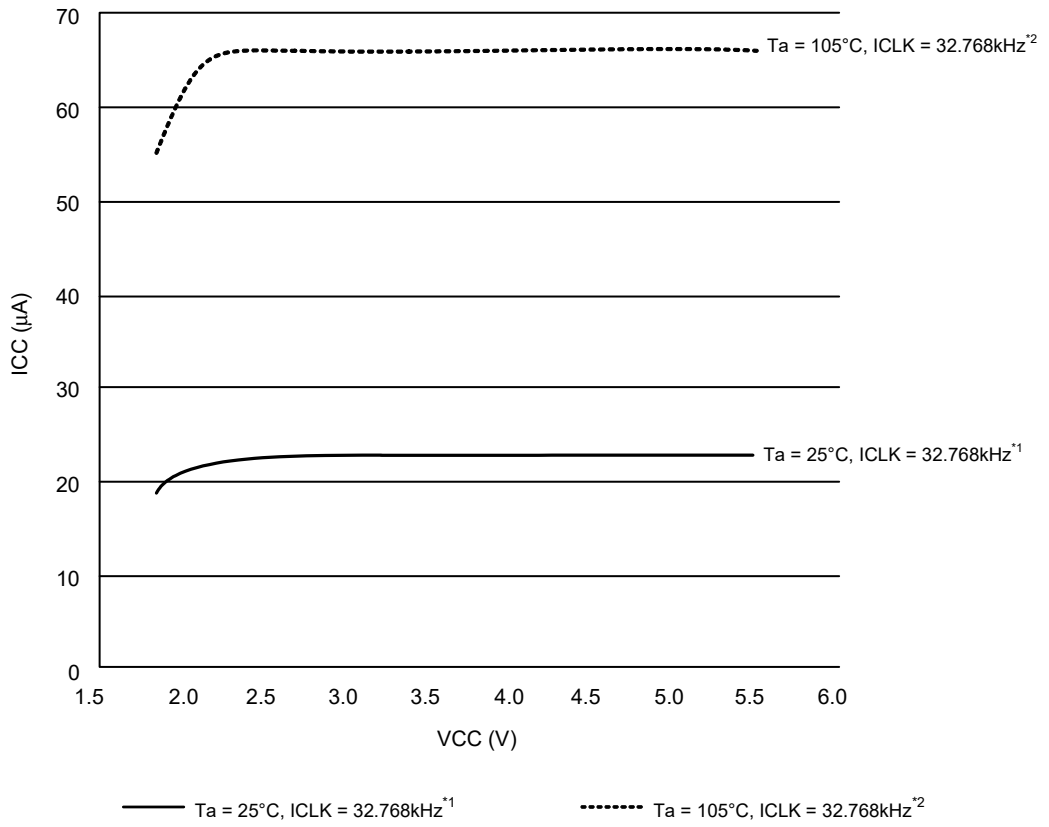
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltages	VCC*1, *2	When USB is not used	1.8	—	5.5	V
		When USB is used When USB regulator is not used	3.0	—	3.6	
		When USB is used When USB regulator is used	4.0	—	5.5	
	VSS		—	0	—	
USB power supply voltages	VCC_USB	When USB regulator is not used	—	VCC	—	V
	VSS_USB		—	0	—	
VBATT power supply voltage	VBATT		1.8	—	5.5	V
Analog power supply voltages	AVCC0*1, *2		1.8	—	5.5	V
	AVSS0		—	0	—	
	VREFH0		1.8	—	AVCC0	
	VREFL0		—	0	—	
	VREFH		1.8	—	AVCC0	
	VREFL		—	0	—	

Note 1. Use AVCC0 and VCC under the following conditions:
AVCC0 and VCC can be set individually within the operating range when VCC ≥ 2.0 V
AVCC0 = VCC when VCC < 2.0 V
Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.



Note 1. All peripheral operations except any BGO operation are operating normally. Indicates the average of the typical samples through actual measurement during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. Indicates the average of the upper-limit samples through actual measurement during product evaluation.

Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)



Note 1. All peripheral operations except any BGO operation are operating normally. Indicates the average of the typical samples through actual measurement during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. Indicates the average of the upper-limit samples through actual measurement during product evaluation.

Figure 5.3 Voltage Dependency in Low-Speed Operating Mode (Reference Data)

Table 5.16 Permissible Output Currents (1)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +85°C

Item			Symbol	Max.	Unit
Permissible output low current (average value per pin)	Ports 40 to 47, ports 03, 05, 07, port 36, 37		I_{OL}	4.0	mA
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current (maximum value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37			4.0	
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current	Total of ports 40 to 47, ports 03, 05, 07		ΣI_{OL}	40	
	Total of ports 12 to 17, ports 20 to 27, ports 30 to 37, port PJ3			40	
	Total of ports 50 to 55, ports C0 to C7, ports B0 to B7			40	
	Total of ports E0 to E7, ports A0 to A7, ports D0 to D4			40	
	Total of all output pins			80	
Permissible output high current (average value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37		I_{OH}	–4.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current (maximum value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37			–4.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current	Total of ports 40 to 47, ports 03, 05, 07		ΣI_{OH}	–40	
	Total of ports 12 to 17, ports 20 to 27, ports 30 to 37, port PJ3			–40	
	Total of ports 50 to 55, ports C0 to C7, ports B0 to B7			–40	
	Total of ports E0 to E7, ports A0 to A7, ports D0 to D4			–40	
	Total of all output pins			–80	

Note: Do not exceed the permissible total supply current.

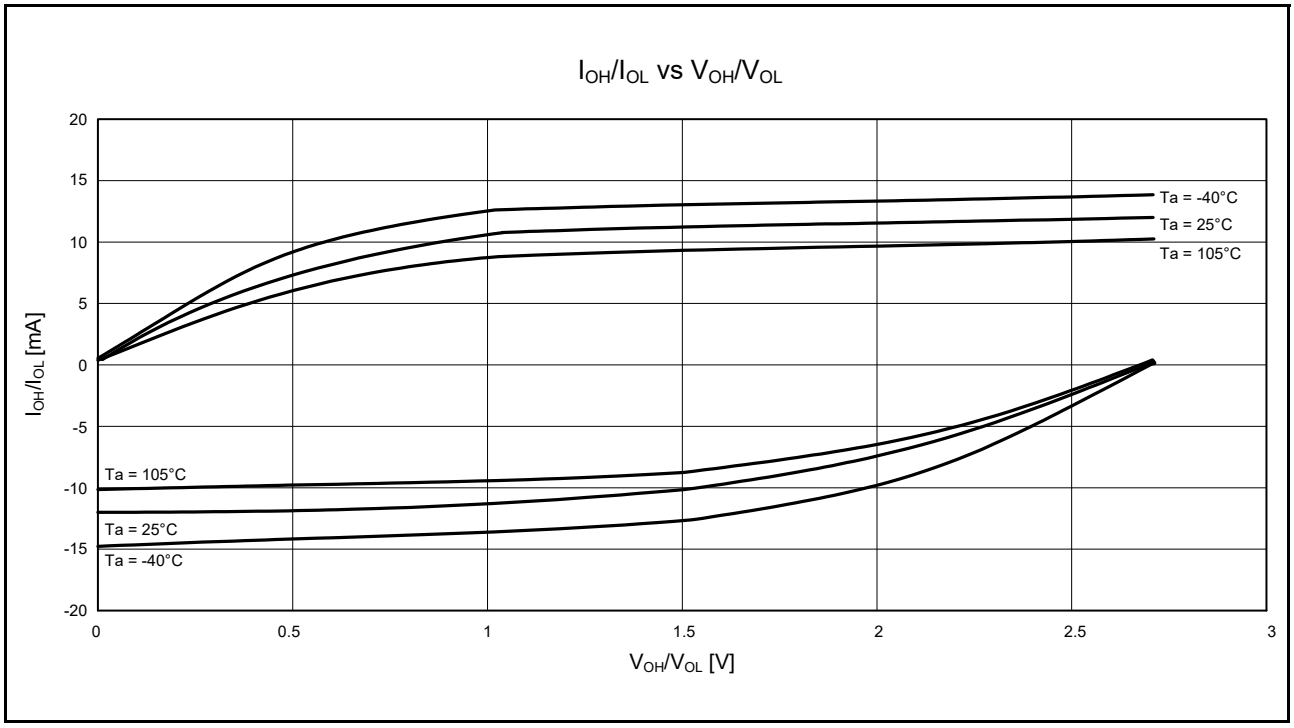


Figure 5.10 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V When Normal Output is Selected (Reference Data)

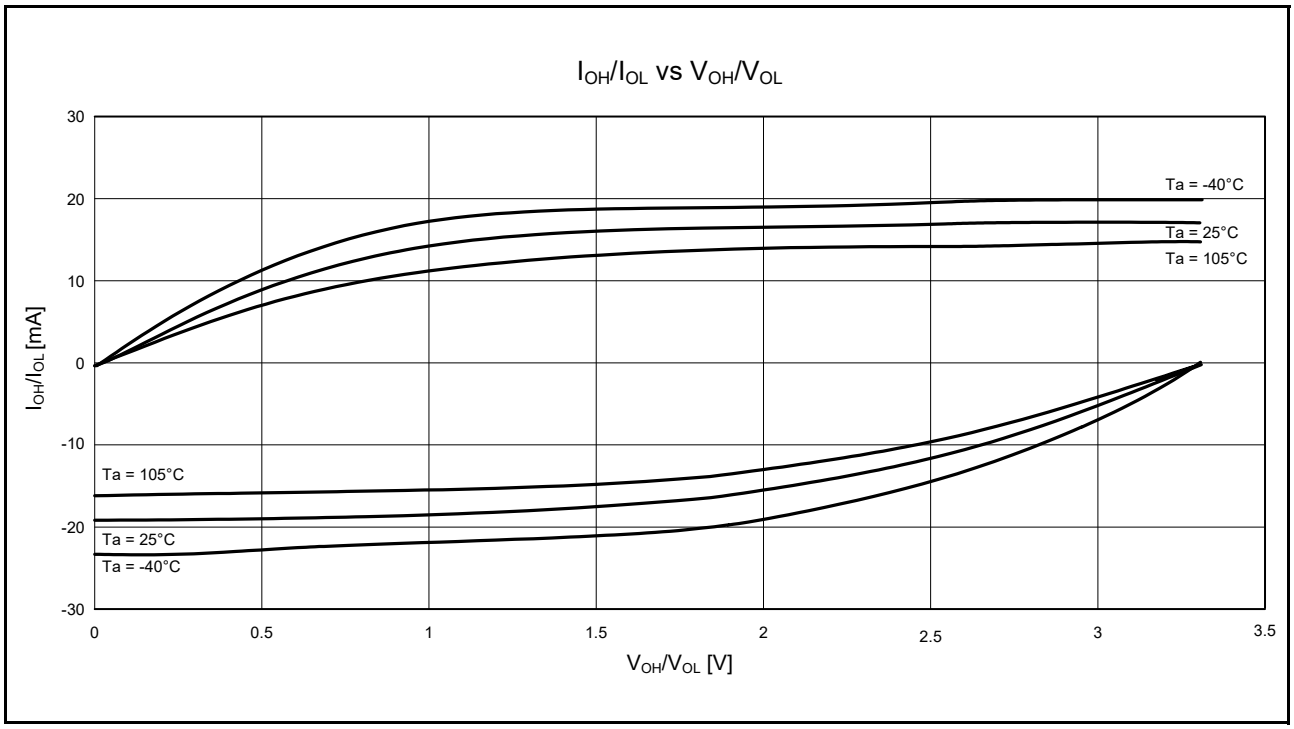


Figure 5.11 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 3.3 V When Normal Output is Selected (Reference Data)

Table 5.30 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Low-speed mode	Sub-clock oscillator operating	t_{SBYSC}	—	600	750	µs	Figure 5.34

Note 1. The sub-clock continues oscillating in software standby mode during low-speed mode.

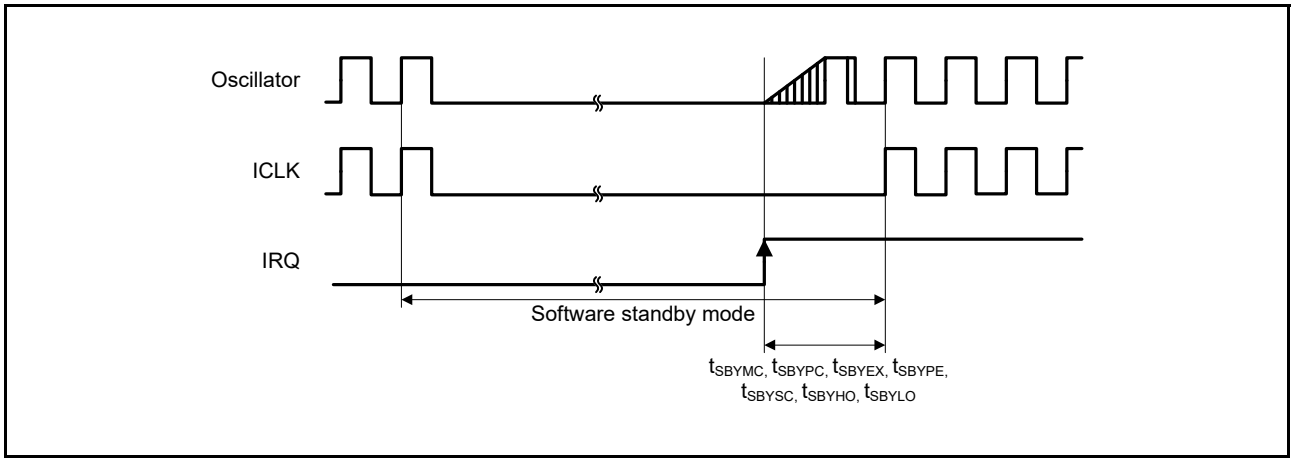


Figure 5.34 Software Standby Mode Recovery Timing

Table 5.31 Timing of Recovery from Low Power Consumption Modes (4)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	t_{DSLP}	—	2	3.5	µs	Figure 5.35
	Middle-speed mode*3	t_{DSLP}	—	3	4	µs	
	Low-speed mode*4	t_{DSLP}	—	400	500	µs	

Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. When the frequency of the system clock is 32 MHz.
Note 3. When the frequency of the system clock is 12 MHz.
Note 4. When the frequency of the system clock is 32 kHz.

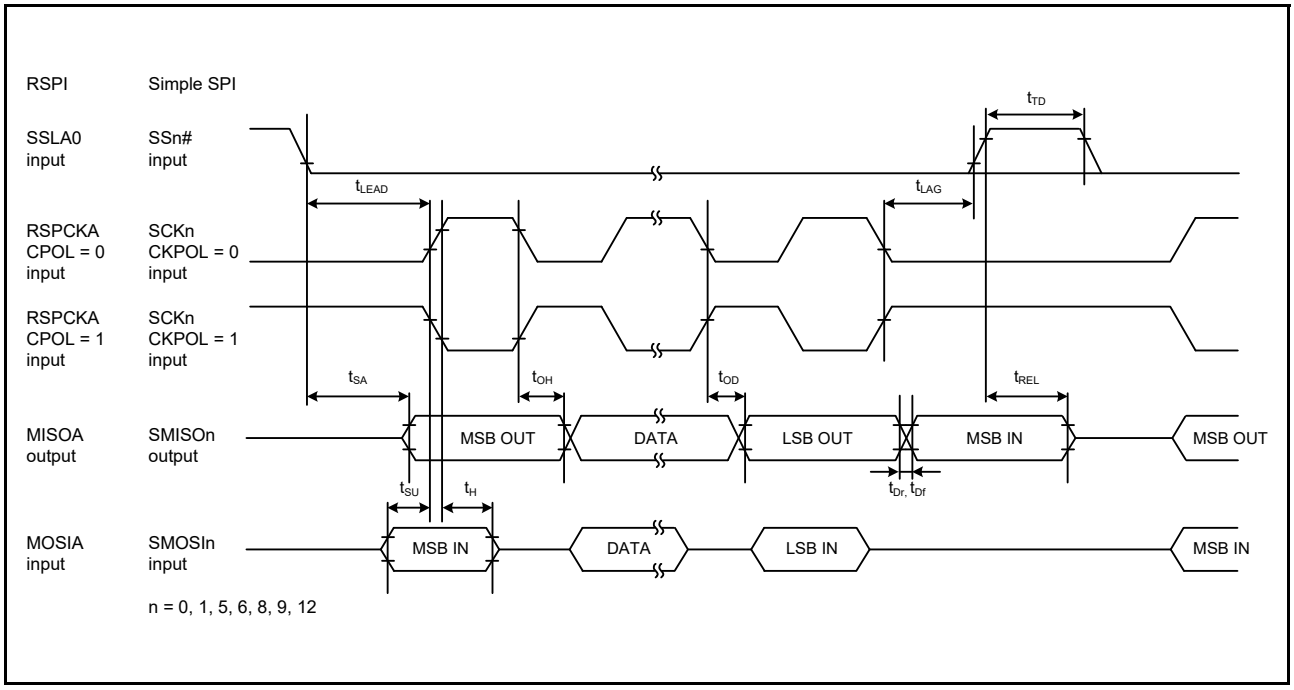


Figure 5.57 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

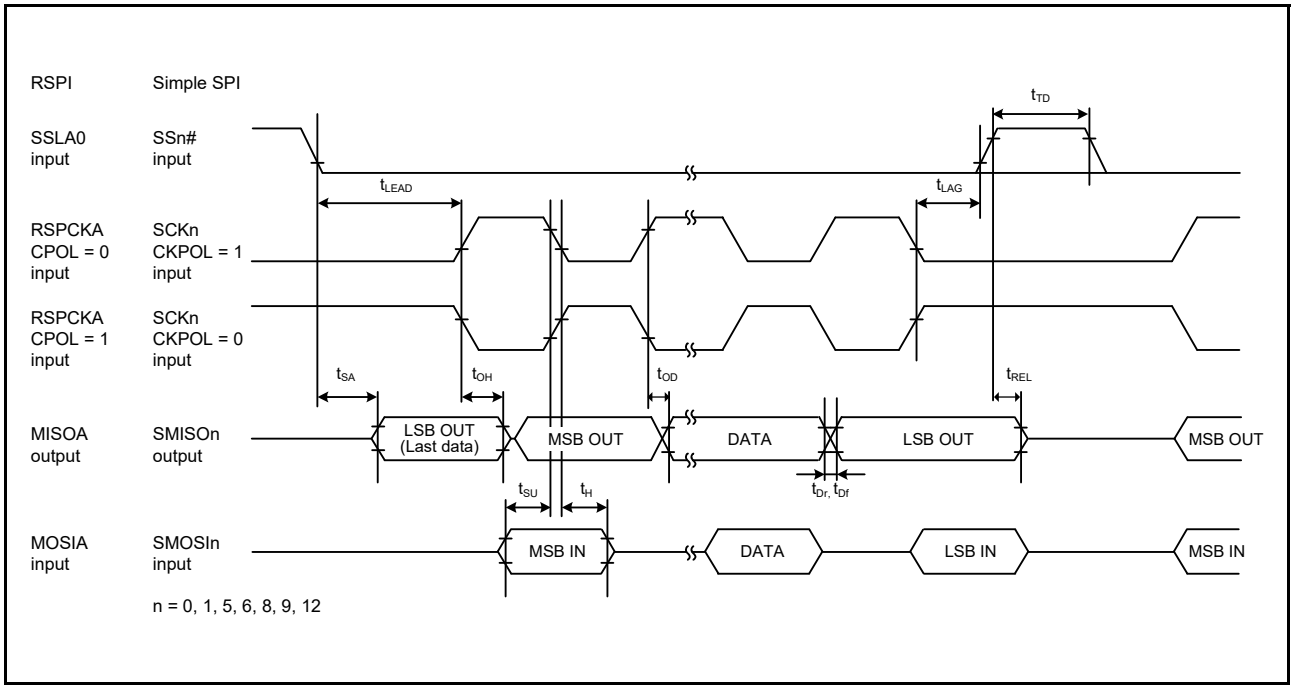


Figure 5.58 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)

Table 5.50 A/D Conversion Characteristics (5)

Conditions: 1.8V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5V, 1.8V ≤ VREFH0 ≤ AVCC0, VSS = AVSS0 = VSS_USB = 0V, reference voltage = VREFH0 selected, Ta = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance (Max.) = 5 kΩ	6.75	—	—	µs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 0Dh
		10.13	—	—		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 5.68
Analog input resistance	Rs	—	—	2.5	kΩ	Figure 5.68
Offset error		—	±1	±7.5	LSB	
Full-scale error		—	±1.5	±7.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential non-linearity error		—	±1.0	—	LSB	
INL integral non-linearity error		—	±1.25	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.51 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN007	AVCC0 = 1.8 to 5.5 V	Pins AN000 to AN007 cannot be used as digital outputs when the A/D converter is in use.
Normal-precision channel	AN016 to AN031		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 2.0 to 5.5 V	
Temperature sensor input channel	Temperature sensor output	AVCC0 = 2.0 to 5.5 V	

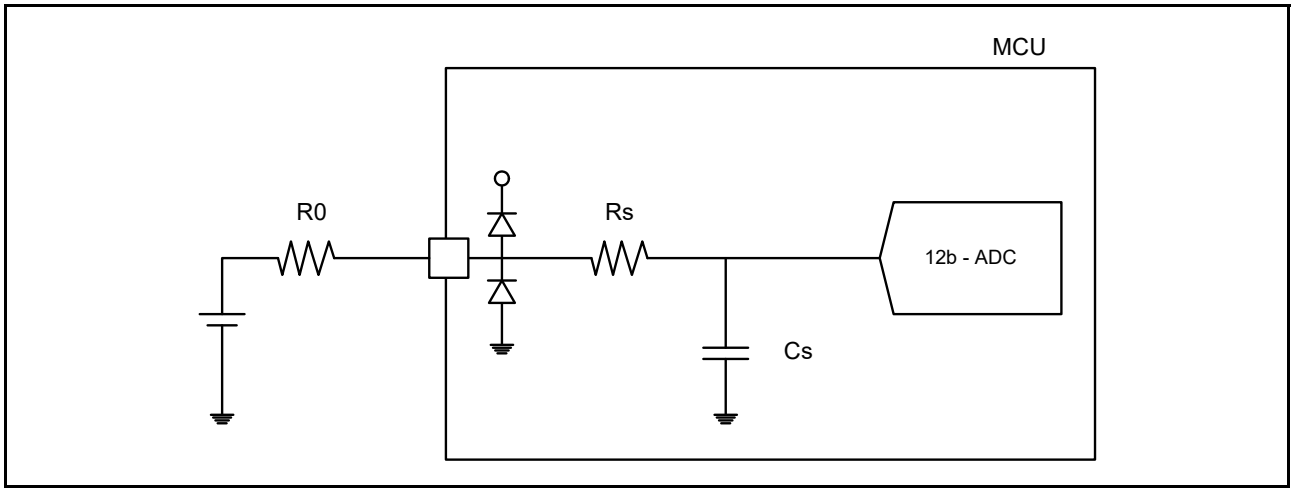


Figure 5.68 Equivalent Circuit

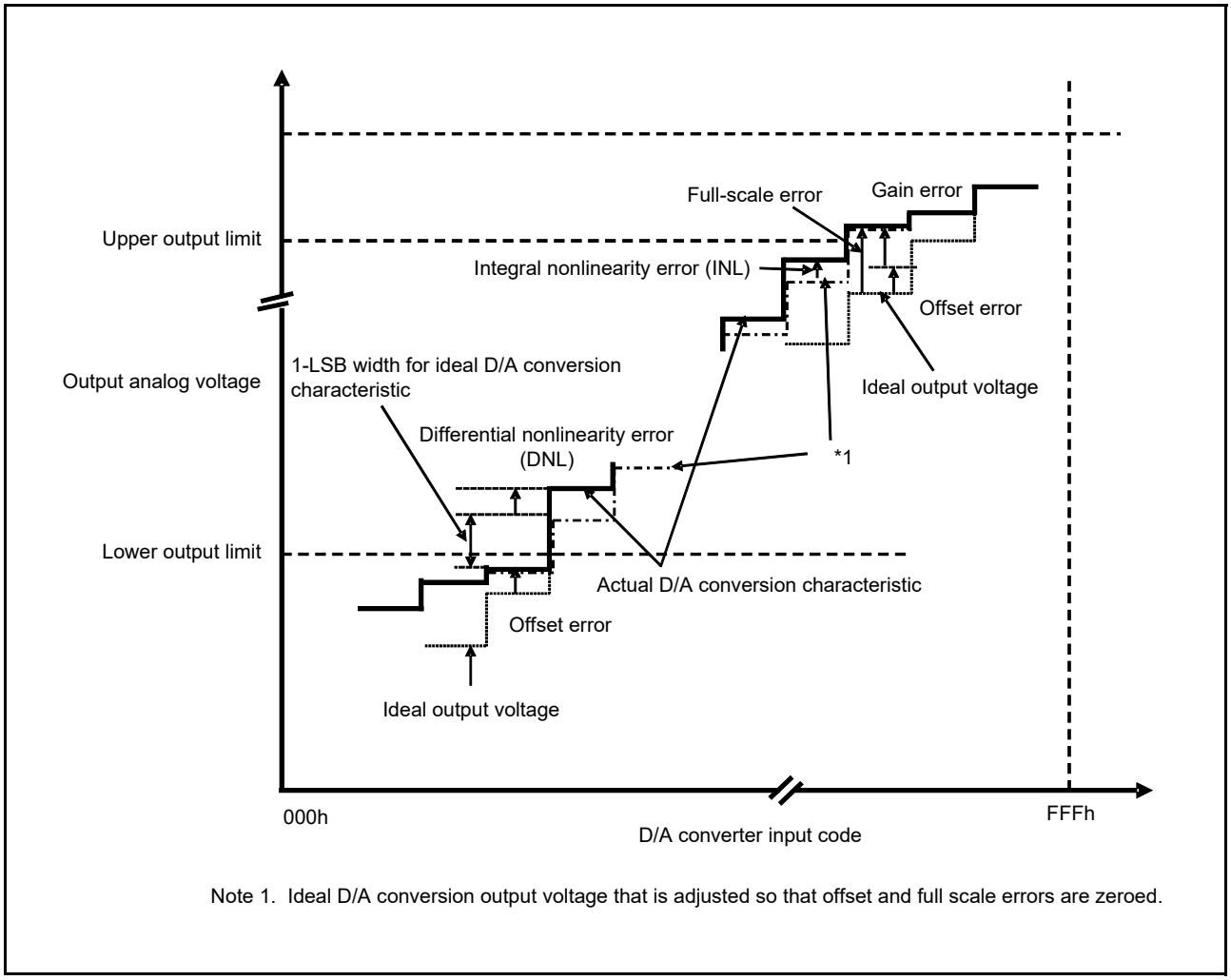


Figure 5.70 Illustration of D/A Converter Characteristic Terms

Integral non-linearity error (INL)

The integral non-linearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential non-linearity error (DNL)

The differential non-linearity error is the difference between 1-LSB width based on the ideal D/A conversion characteristics and the width of the actually output code.

Offset error

An offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

A full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

5.14 E2 DataFlash Characteristics (Flash Memory for Data Storage)

Table 5.65 E2 DataFlash Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	—	Times	
Data hold time	After 10000 times of N_{DPEC}	t_{DDRP}	20*2, *3	—	—	Year	T_a = +85°C
	After 100000 times of N_{DPEC}		5*2, *3	—	—	Year	
	After 1000000 times of N_{DPEC}		—	1*2, *3	—	Year	T_a = +25°C

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1000 times for different addresses in a 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristic when the flash memory programmer is used and the self-programming library is provided from Renesas Electronics.
Note 3. These results are obtained from reliability testing.

Table 5.66 E2 DataFlash Characteristics (2) : high-speed operating mode

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1 byte	t_{DP1}	—	95.0	797	—	40.8	376	µs
Erasure time	1 Kbyte	t_{DE1K}	—	19.5	498	—	6.2	230	ms
	8 Kbyte	t_{DE8K}	—	119.8	2556	—	12.9	368	ms
Blank check time	1 byte	t_{DBC1}	—	—	55.00	—	—	16.1	µs
	1 Kbyte	t_{DBC1K}	—	—	0.72	—	—	0.50	ms
Erase operation forced stop time		t_{DSED}	—	—	16.0	—	—	10.7	µs
DataFlash STOP recovery time		t_{DSTOP}	5.0	—	—	5.0	—	—	µs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be within ±3.5%.

Table 5.67 E2 DataFlash Characteristics (3) : middle-speed operating mode

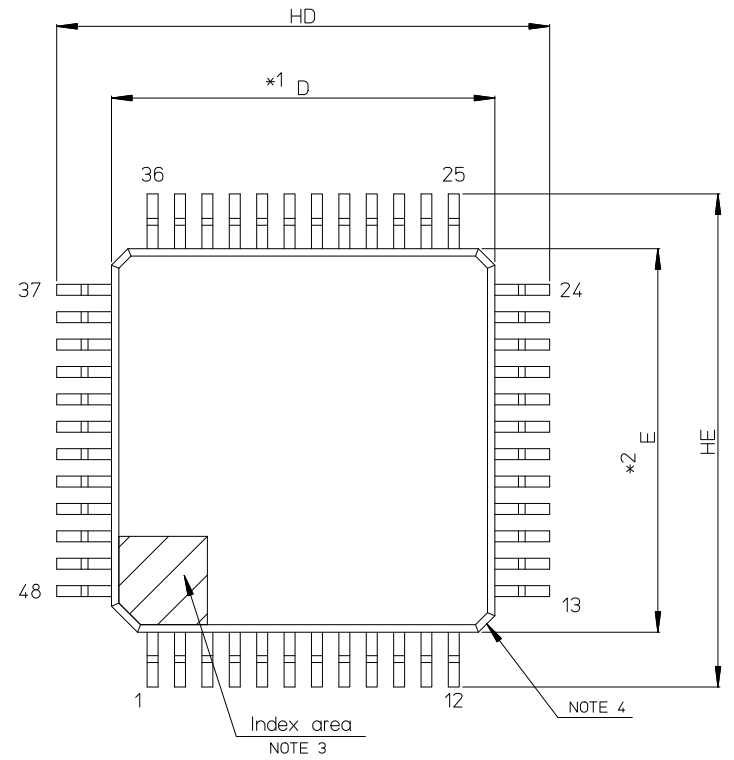
Conditions: 1.8 V ≤ VCC0 = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V

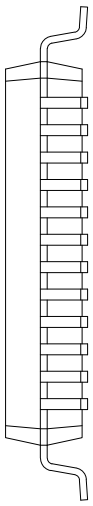
Temperature range for the programming/erasure operation: T_a = –40 to +85°C

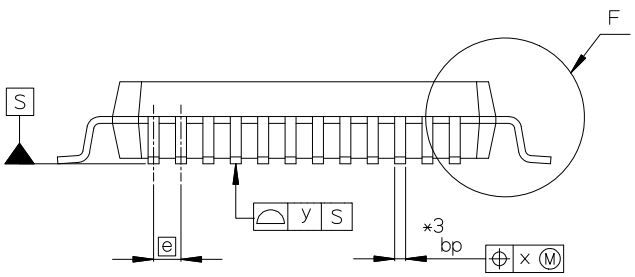
Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1 byte	t_{DP1}	—	135	1197	—	86.5	823	µs
Erasure time	1 Kbyte	t_{DE1K}	—	19.6	501	—	8.0	265	ms
	8 Kbyte	t_{DE8K}	—	120	2558		27.7	669	ms
Blank check time	1 byte	t_{DBC1}	—	—	85.0	—	—	50.9	µs
	1 Kbyte	t_{DBC1K}	—	—	0.72	—	—	1.45	ms
Erase operation forced stop time		t_{DSED}	—	—	28.0	—	—	21.3	µs
DataFlash STOP recovery time		t_{DSTOP}	0.72	—	—	0.72	—	—	µs

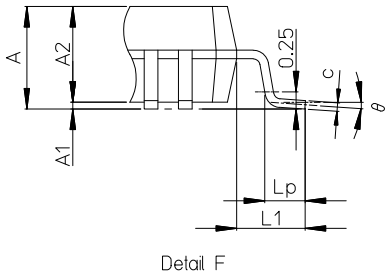
Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be within ±3.5%.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	——	0.2g









Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A2	——	1.4	——
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.17	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

Figure G 48 -Pin LFQFP (PLQP0048KB-B)

REVISION HISTORY	RX230 Group, RX231 Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Jun 24, 2015	—	First edition, issued	
1.10	Oct 30, 2015	1. Overview		
		3	Table 1.1 Outline of Specifications (2/4), changed	
		5	Table 1.1 Outline of Specifications (4/4): SD Host Interface (SDHIa) added	
		6	Table 1.2 Comparison of Functions for Different Packages: RX230 Group added	
		3. Address Space		
		39	Figure 3.1 Memory Map in Each Operating Mode, changed	
		4. I/O Registers		
		67	Table 4.1 List of I/O Registers (Address Order) (25 / 42), changed	TN-RX*-A139A/E
		83	Table 4.1 List of I/O Registers (Address Order) (41 / 42), changed	
		5. Electrical Characteristics		
		85	Table 5.1 Absolute Maximum Ratings, changed	TN-RX*-A137A/E
		86	Table 5.2 Recommended Operating Voltage Conditions, changed	
		87	Table 5.3 DC Characteristics (1), changed	TN-RX*-A137A/E
		88	Table 5.4 DC Characteristics (2), changed	
		88	Table 5.5 DC Characteristics (3), changed	
		89	Table 5.7 DC Characteristics (5), changed	
		91	Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data), changed	
		92	Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data), changed	
		93	Figure 5.3 Voltage Dependency in Low-Speed Operating Mode (Reference Data), changed	TN-RX*-A137A/E
		94	Table 5.8 DC Characteristics (6), changed Figure 5.4 Voltage Dependency in Software Standby Mode (Reference Data), changed	
		95	Figure 5.5 Temperature Dependency in Software Standby Mode (Reference Data), changed	
		96	Figure 5.6 Temperature Dependency of RTC Operation with VCC Off (Reference Data), changed Table 5.10 DC Characteristics (8): Conditions changed	
		97	Table 5.11 DC Characteristics (9), changed	TN-RX*-A137A/E
		99	Table 5.16 Permissible Output Currents (1), changed	TN-RX*-A137A/E
		100	Table 5.17 Permissible Output Currents (2), changed	
		101	Table 5.18 Output Values of Voltage (1), changed	
		101	Table 5.19 Output Values of Voltage (2), changed	TN-RX*-A137A/E
		101	Table 5.20 Output Values of Voltage (3), changed	TN-RX*-A137A/E
		105	Figure 5.13 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C When High-Drive Output is Selected (Reference Data), changed	TN-RX*-A137A/E
		108	Figure 5.18 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at Ta = 25°C (Reference Data)	TN-RX*-A137A/E
		110	Table 5.21 Operating Frequency Value (High-Speed Operating Mode) and Table 5.22 Operating Frequency Value (Middle-Speed Operating Mode), changed	TN-RX*-A137A/E
		112	Table 5.26 Clock Timing, changed	TN-RX*-A137A/E
		116	Table 5.27 Reset Timing, changed	
		131	Table 5.41 Timing of On-Chip Peripheral Modules (4): Note changed	
		132	Table 5.43 Timing of On-Chip Peripheral Modules (6), changed	
		138	Figure 5.61 SSI Transmission/Reception Timing (SSICP.SCKP=0), changed	TN-RX*-A137A/E
		139	Figure 5.62 SSI Transmission/Reception Timing (SSICP.SCKP=1), changed	TN-RX*-A137A/E
		142	Figure 5.66 VREFH0 Voltage Range vs. AVCC0, changed	

Rev.	Date	Description		Classification
		Page	Summary	
1.10	Oct 30, 2015	142	Table 5.45 A/D Conversion Characteristics (1): Conditions and Voltage Range of Analog Input (Max.), changed	
		143	Table 5.46 A/D Conversion Characteristics (2): Conditions changed	
		144	Table 5.47 A/D Conversion Characteristics (3): Conditions changed	
		145	Table 5.48 A/D Conversion Characteristics (4): Conditions changed	
		146	Table 5.49 A/D Conversion Characteristics (5): Conditions changed and Absolute accuracy (Test Conditions) deleted	
		153	Table 5.57 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (1), changed	TN-RX*-A137A/E
		154	Table 5.58 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (2), changed	
		155	Figure 5.73 Power-On Reset Timing and Figure 5.74 Voltage Detection Circuit Timing (Vdet0), changed	
		159	Table 5.62 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode: Note changed	
		160	Table 5.63 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating Mode: Note changed	
		161	Table 5.65 E2 DataFlash Characteristics (2): high-speed operating mode, Note changed	
		161	Table 5.66 E2 DataFlash Characteristics (3): middle-speed operating mode, Conditions and Note changed	
		163	Figure 5.79 Connecting Capacitors (100 Pins), changed	
		164	Figure 5.80 Connecting Capacitors (64 Pins), changed	
		165	Figure 5.81 Connecting Capacitors (48 Pins), changed	
		Appendix 1. Package Dimensions		
		167	Figure B 100 -Pin LQFP (PLQP0100KB-B), changed	TN-RX*-A137A/E
		170	Figure E 64 -Pin LQFP (PLQP0064KB-C), changed	TN-RX*-A137A/E
		172	Figure G 48 -Pin LQFP (PLQP0048KB-B), changed	TN-RX*-A137A/E
1.20	Sep 28, 2018	Features		
		1	SD host interface (optional: one channel) SD memory/ SDIO 1-bit or 4-bit SD bus supported, Note deleted	TN-RX*-A145A/E
		1. Overview		
		6	Table 1.2 Comparison of Functions for Different Packages, changed (deletion of IRQ2 on 64-pin package)	
		6	Table 1.2 Comparison of Functions for Different Packages, Note 1 added	TN-RX*-A145A/E
		7	Table 1.3 List of Products: D Version (Ta = –40 to +85°C) (1/2), changed	TN-RX*-A145A/E
		9	Table 1.4 List of Products: G Version (Ta = –40 to +105°C) (1/2), changed	TN-RX*-A145A/E
		11	Figure 1.1 How to Read the Product Part Number, changed	TN-RX*-A145A/E
		16	Table 1.5 Pin Functions (4/4), changed (changes in description for VCC_USB)	TN-RX*-A201A/E
		24	Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (2/3), changed (UPSEL was added to the column of P35)	
		24	Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (2/3), changed (USB0_VBUS was added to the column of PB5)	
		26	Table 1.7 List of Pins and Pin Functions (100-Pin LFQFP) (1/3), changed (UPSEL was added to the column of P35)	
		29	Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (1/2), changed (UPSEL was added to the column of P35)	
		30	Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (2/2), changed (USB0_VBUS was added to the column of PB5)	
		31	Table 1.9 List of Pins and Pin Functions (64-Pin LFQFP/HWQFN) (1/2), changed (UPSEL was added to the column of P35)	
		31	Table 1.9 List of Pins and Pin Functions (64-Pin LQFP/HWQFN) (1/2), changed (USB0_VBUS was added to the column of PB5)	
		33	Table 1.10 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (1/2), changed (UPSEL was added to the column of P35)	
		33	Table 1.10 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (1/2), changed	TN-RX*-A145A/E
		5. Electrical Characteristics		
		92	Table 5.18 Output Values of Voltage (1), changed	TN-RX*-A201A/E
		92	Table 5.19 Output Values of Voltage (2), changed	TN-RX*-A201A/E