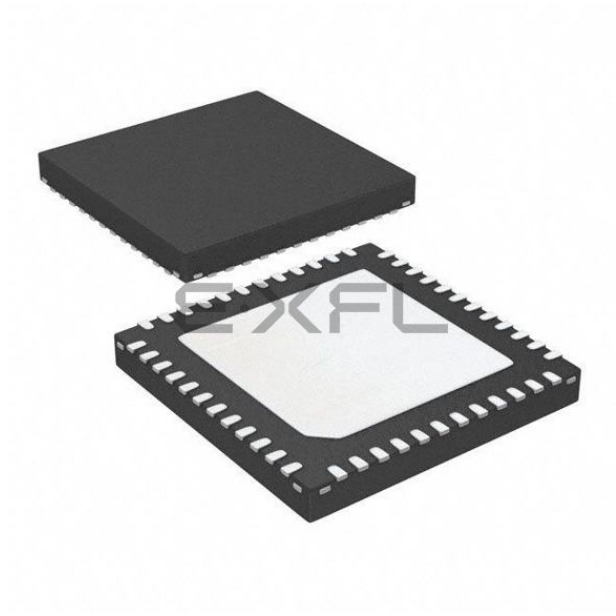
Renesas Electronics America Inc - R5F52306ADNE#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	I²C, IrDA, SCI, SPI, SSI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52306adne-u0

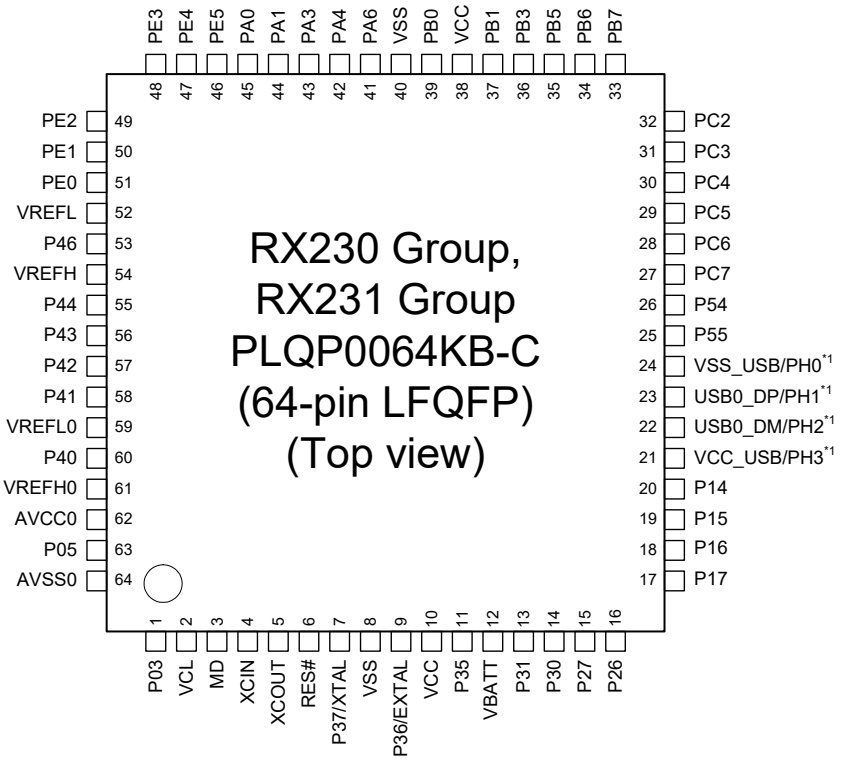
Table 1.1 Outline of Specifications (2/4)

Classification	Module/Function	Description
Low power consumption	Low power consumption functions	• Module stop function • Three low power consumption modes Sleep mode, deep sleep mode, and software standby mode • Low power timer that operates during the software standby state
	Function for lower operating power consumption	• Operating power control modes High-speed operating mode, middle-speed operating mode, and low-speed operating mode
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 167 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 7 (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, IWDT interrupt, and VBATT power monitoring interrupt) • 16 levels specifiable for the order of priority
External bus extension		• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS3) A chip-select signal (CS0# to CS3#) can be output for each area. Each area is specifiable as an 8-bit or 16-bit bus space The data arrangement in each area is selectable as little or big endian (only for data). Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function
I/O ports	General I/O ports	100-pin/64-pin/48-pin I/O: 79/43/30 (RX231 Group), 83/47/34 (RX230 Group) • Input: 1/1/1 Pull-up resistors: 79/43/30(RX231 Group), 83/47/34 (RX230 Group) • Open-drain outputs: 58/34/26 • 5-V tolerance: 8/5/5
Event link controller (ELC)		• Event signals of 61 types can be directly connected to the module • Operations of timer modules are selectable at event input • Capable of event link operation for port B and port E
Multi-function pin controller (MPC)		Capable of selecting the input/output function from multiple pins
Timers	16-bit timer pulse unit (TPUa)	• (16 bits × 6 channels) × 1 unit • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Supports the input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Support for buffered operation, phase-counting mode (two-phase encoder input) and cascade connected operation (32 bits × 2 channels) depending on the channel. • Capable of generating conversion start triggers for the A/D converters • Signals from the input capture pins are input via a digital filter • Clock frequency measuring method
	Multi-function timer pulse unit 2 (MTU2a)	• (16 bits × 6 channels) × 1 unit • Up to 16 pulse-input/output lines and three pulse-input lines are available based on the six 16-bit timer channels • Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Pulse output mode • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Capable of generating conversion start triggers for the A/D converter
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDTA)	• 14 bits x 1 channel • Select from among six counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX230 Group			RX231 Group		
		100 Pins	64 Pins	48 Pins	100 Pins	64 Pins	48 Pins
External bus	External bus	16 bit	Not supported		16 bit	Not supported	
Interrupts	External interrupts	NMI, IRQ0 to IRQ7	NMI, IRQ0, IRQ1, IRQ4 to IRQ7	NMI, IRQ0, IRQ1, IRQ4 to IRQ7	NMI, IRQ0 to IRQ7	NMI, IRQ0, IRQ1, IRQ4 to IRQ7	NMI, IRQ0, IRQ1, IRQ4 to IRQ7
DMA	DMA controller	4 channels (DMAC0 to DMAC3)			4 channels (DMAC0 to DMAC3)		
	Data transfer controller	Available			Available		
Timers	16-bit timer pulse unit	6 channels (TPU0 to TPU5)			6 channels (TPU0 to TPU5)		
	Multi-function timer pulse unit 2	6 channels (MTU0 to MTU5)			6 channels (MTU0 to MTU5)		
	Port output enable 2	POE0# to POE3#, POE8#			POE0# to POE3#, POE8#		
	8-bit timer	2 channels× 2 units			2 channels× 2 units		
	Compare match timer	2 channels× 2 units			2 channels× 2 units		
	Low power timer	1 channel			1 channel		
	Realtime clock	Available		Not supported	Available		Not supported
	Watchdog timer	Available			Available		
	Independent watchdog timer	Available			Available		
Communication functions	Serial communications interfaces (SCIg)	6 channels (SCI0, 1, 5, 6, 8, 9)	5 channels (SCI1, 5, 6, 8, 9)	4 channels (SCI1, 5, 6, 8)	6 channels (SCI0, 1, 5, 6, 8, 9)	5 channels (SCI1, 5, 6, 8, 9)	4 channels (SCI1, 5, 6, 8)
	IrDA interface	1 channel (SCI5)			1 channel (SCI5)		
	Serial communications interfaces (SCIh)	1 channel (SCI12)			1 channel (SCI12)		
	I²C bus interface	1 channel			1 channel		
	CAN module	Not supported			1 channel*1		
	Serial peripheral interface	1 channel			1 channel		
	USB 2.0 host/function module	Not supported			1 channel		
	Serial sound interface	1 channel			1 channel		
	SD Host Interface	Not supported			1 channel*1		Not supported
Capacitive touch sensing unit		24 channels	10 channels	6 channels	24 channels	10 channels	6 channels
12-bit A/D converter (including high-precision channels)		24 channels (8 channels)	12 channels (6 channels)	8 channels (4 channels)	24 channels (8 channels)	12 channels (6 channels)	8 channels (4 channels)
Temperature sensor		Available			Available		
D/A converter		2 channels		Not supported	2 channels		Not supported
CRC calculator		Available			Available		
Event link controller		Available			Available		
Comparator B		4 channels			4 channels		
Packages		100-pin TFLGA 100-pin LFQFP	64-pin WFLGA 64-pin HWQFN 64-pin LFQFP	48-pin HWQFN 48-pin LFQFP	100-pin TFLGA 100-pin LFQFP	64-pin WFLGA 64-pin HWQFN 64-pin LFQFP	48-pin HWQFN 48-pin LFQFP

Note 1. Only for chip version B



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin LFQFP/HWQFN)”.

Note 1. RX230: PH0, PH1, PH2, PH3
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Figure 1.7 Pin Assignments of the 64-Pin LFQFP

Table 4.1 List of I/O Registers (Address Order) (16/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 C023h	PORT3	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C024h	PORT4	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C025h	PORT5	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C02Ah	PORTA	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C02Bh	PORTB	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C02Ch	PORTC	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C02Dh	PORTD	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C02Eh	PORTE	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C031h	PORTH	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C032h	PORTJ	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C040h	PORT0	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C041h	PORT1	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C042h	PORT2	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C043h	PORT3	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C044h	PORT4	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C045h	PORT5	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C04Ah	PORTA	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C04Bh	PORTB	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C04Ch	PORTC	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C04Dh	PORTD	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C04Eh	PORTE	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C051h	PORTH	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C052h	PORTJ	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C060h	PORT0	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C061h	PORT1	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C062h	PORT2	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C063h	PORT3	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C064h	PORT4	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C065h	PORT5	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C06Ah	PORTA	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C06Bh	PORTB	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C06Ch	PORTC	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C06Dh	PORTD	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C06Eh	PORTE	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C071h	PORTH	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C072h	PORTJ	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C082h	PORT1	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C083h	PORT1	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C084h	PORT2	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C08Ah	PORT5	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C08Bh	PORT5	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C098h	PORTC	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C099h	PORTC	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C09Dh	PORTE	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (29/33)

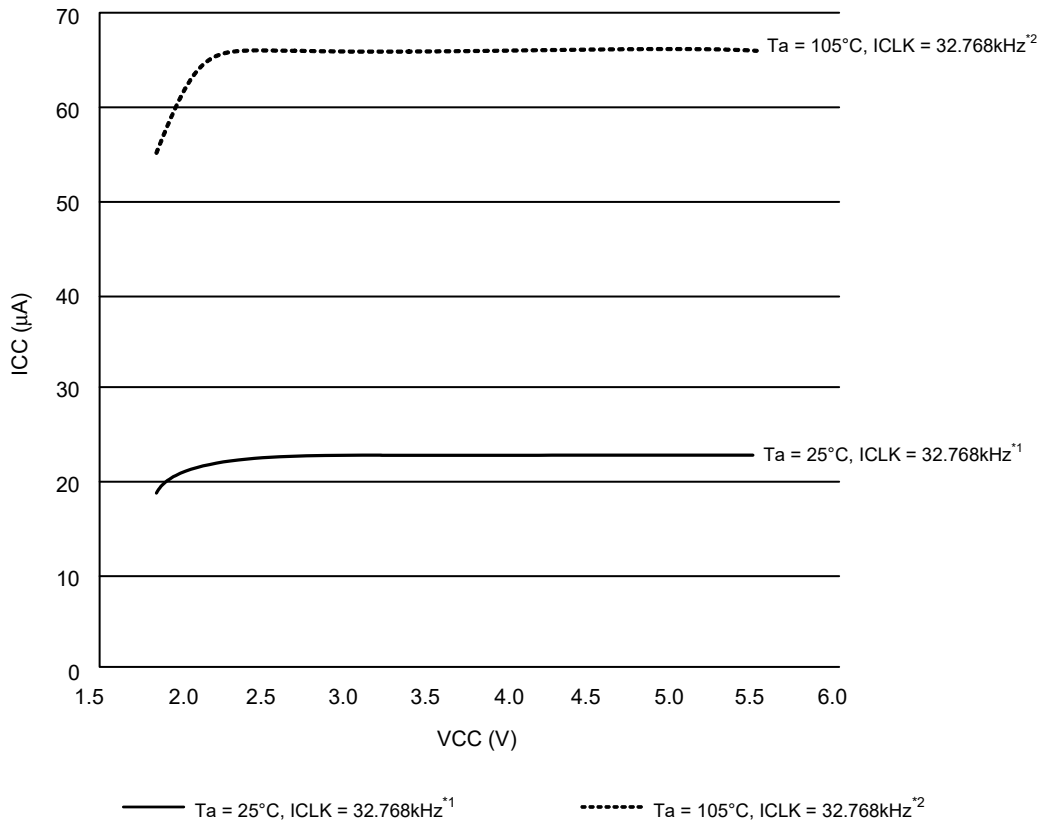
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
000A 8494h	RSCAN	Receive Buffer Register 15BL	RMTS15	16	16	2 or 3 PCLKB	2 ICLK
000A 8496h	RSCAN	Receive Buffer Register 15BH	RMPTR15	16	16	2 or 3 PCLKB	2 ICLK
000A 8498h	RSCAN	Receive Buffer Register 15CL	RMDF015	16	16	2 or 3 PCLKB	2 ICLK
000A 849Ah	RSCAN	Receive Buffer Register 15CH	RMDF115	16	16	2 or 3 PCLKB	2 ICLK
000A 849Ch	RSCAN	Receive Buffer Register 15DL	RMDF215	16	16	2 or 3 PCLKB	2 ICLK
000A 849Eh	RSCAN	Receive Buffer Register 15DH	RMDF315	16	16	2 or 3 PCLKB	2 ICLK
000A 8580h to 000A 859Fh	RSCAN	RAM Test Register 0 to RAM Test Register 15	RPGACC0 to RPGACC15	16	16	2 or 3 PCLKB	2 ICLK
000A 85A0h	RSCAN	Receive FIFO Access Register 0AL	RFIDL0	16	16	2 or 3 PCLKB	2 ICLK
000A 85A0h	RSCAN	RAM Test Register 16	RPGACC16	16	16	2 or 3 PCLKB	2 ICLK
000A 85A2h	RSCAN	Receive FIFO Access Register 0AH	RFIDH0	16	16	2 or 3 PCLKB	2 ICLK
000A 85A2h	RSCAN	RAM Test Register 17	RPGACC17	16	16	2 or 3 PCLKB	2 ICLK
000A 85A4h	RSCAN	Receive FIFO Access Register 0BL	RFTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 85A4h	RSCAN	RAM Test Register 18	RPGACC18	16	16	2 or 3 PCLKB	2 ICLK
000A 85A6h	RSCAN	Receive FIFO Access Register 0BH	RFPTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 85A6h	RSCAN	RAM Test Register 19	RPGACC19	16	16	2 or 3 PCLKB	2 ICLK
000A 85A8h	RSCAN	Receive FIFO Access Register 0CL	RFDF00	16	16	2 or 3 PCLKB	2 ICLK
000A 85A8h	RSCAN	RAM Test Register 20	RPGACC20	16	16	2 or 3 PCLKB	2 ICLK
000A 85AAh	RSCAN	Receive FIFO Access Register 0CH	RFDF10	16	16	2 or 3 PCLKB	2 ICLK
000A 85AAh	RSCAN	RAM Test Register 21	RPGACC21	16	16	2 or 3 PCLKB	2 ICLK
000A 85ACh	RSCAN	Receive FIFO Access Register 0DL	RFDF20	16	16	2 or 3 PCLKB	2 ICLK
000A 85ACh	RSCAN	RAM Test Register 22	RPGACC22	16	16	2 or 3 PCLKB	2 ICLK
000A 85AEh	RSCAN	Receive FIFO Access Register 0DH	RFDF30	16	16	2 or 3 PCLKB	2 ICLK
000A 85AEh	RSCAN	RAM Test Register 23	RPGACC23	16	16	2 or 3 PCLKB	2 ICLK
000A 85B0h	RSCAN	Receive FIFO Access Register 1AL	RFIDL1	16	16	2 or 3 PCLKB	2 ICLK
000A 85B0h	RSCAN	RAM Test Register 24	RPGACC24	16	16	2 or 3 PCLKB	2 ICLK
000A 85B2h	RSCAN	Receive FIFO Access Register 1AH	RFIDH1	16	16	2 or 3 PCLKB	2 ICLK
000A 85B2h	RSCAN	RAM Test Register 25	RPGACC25	16	16	2 or 3 PCLKB	2 ICLK
000A 85B4h	RSCAN	Receive FIFO Access Register 1BL	RFTS1	16	16	2 or 3 PCLKB	2 ICLK
000A 85B4h	RSCAN	RAM Test Register 26	RPGACC26	16	16	2 or 3 PCLKB	2 ICLK
000A 85B6h	RSCAN	Receive FIFO Access Register 1BH	RFPTR1	16	16	2 or 3 PCLKB	2 ICLK
000A 85B6h	RSCAN	RAM Test Register 27	RPGACC27	16	16	2 or 3 PCLKB	2 ICLK
000A 85B8h	RSCAN	Receive FIFO Access Register 1CL	RFDF01	16	16	2 or 3 PCLKB	2 ICLK
000A 85B8h	RSCAN	RAM Test Register 28	RPGACC28	16	16	2 or 3 PCLKB	2 ICLK
000A 85BAh	RSCAN	Receive FIFO Access Register 1CH	RFDF11	16	16	2 or 3 PCLKB	2 ICLK
000A 85BAh	RSCAN	RAM Test Register 29	RPGACC29	16	16	2 or 3 PCLKB	2 ICLK
000A 85BCh	RSCAN	Receive FIFO Access Register 1DL	RFDF21	16	16	2 or 3 PCLKB	2 ICLK
000A 85BCh	RSCAN	RAM Test Register 30	RPGACC30	16	16	2 or 3 PCLKB	2 ICLK
000A 85BEh	RSCAN	Receive FIFO Access Register 1DH	RFDF31	16	16	2 or 3 PCLKB	2 ICLK
000A 85BEh	RSCAN	RAM Test Register 31	RPGACC31	16	16	2 or 3 PCLKB	2 ICLK
000A 85C0h to 000A 85DEh	RSCAN	RAM Test Register 32 to RAM Test Register 47	RPGACC32 to RPGACC47	16	16	2 or 3 PCLKB	2 ICLK
000A 85E0h	RSCAN0	Transmit/Receive FIFO Access Register 0AL	CFIDL0	16	16	2 or 3 PCLKB	2 ICLK
000A 85E0h	RSCAN	RAM Test Register 48	RPGACC48	16	16	2 or 3 PCLKB	2 ICLK
000A 85E2h	RSCAN0	Transmit/Receive FIFO Access Register 0AH	CFIDH0	16	16	2 or 3 PCLKB	2 ICLK
000A 85E2h	RSCAN	RAM Test Register 49	RPGACC49	16	16	2 or 3 PCLKB	2 ICLK
000A 85E4h	RSCAN0	Transmit/Receive FIFO Access Register 0BL	CFTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 85E4h	RSCAN	RAM Test Register 50	RPGACC50	16	16	2 or 3 PCLKB	2 ICLK
000A 85E6h	RSCAN0	Transmit/Receive FIFO Access Register 0BH	CFPTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 85E6h	RSCAN	RAM Test Register 51	RPGACC51	16	16	2 or 3 PCLKB	2 ICLK
000A 85E8h	RSCAN0	Transmit/Receive FIFO Access Register 0CL	CFDF00	16	16	2 or 3 PCLKB	2 ICLK
000A 85E8h	RSCAN	RAM Test Register 52	RPGACC52	16	16	2 or 3 PCLKB	2 ICLK

5.2 DC Characteristics

Table 5.3 DC Characteristics (1)

Conditions: 2.7 V ≤ VCC = VCC_USB ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)		V_{IH}	VCC × 0.7	—	5.8	V	
	Ports 12, 13, 16, 17, port B5 (5 V tolerant)			VCC × 0.8	—	5.8		
	Ports 14 to 15, ports 20 to 27, ports 33 to 37, ports 50 to 55, ports A0 to A7, ports B0 to B4, B6, B7 ports C0 to C7, ports D0 to D7, ports E0 to E7, port J3, Ports 30 to 32 (when time capture event input is not selected), RES#			VCC × 0.8	—	VCC + 0.3		
	Ports 03, 05, 07, ports 40 to 47			AVCC0 × 0.8	—	AVCC0 + 0.3		
	Ports 30 to 32 (when time capture event input is selected)	When VCC is supplied		VCC × 0.8	—	VCC + 0.3		
		When VBATT is supplied		VBATT × 0.8	—	VBATT + 0.3		
	Ports 03, 05, 07, ports 40 to 47		V_{IL}	–0.3	—	AVCC0 × 0.2		
	RIIC input pin (except for SMBus)			–0.3	—	VCC × 0.3		
	Other than RIIC input pin or ports 30 to 32			–0.3	—	VCC × 0.2		
	Ports 30 to 32 (when time capture event input is selected)	When VCC is supplied		–0.3	—	VCC × 0.3		
		When VBATT is supplied		–0.3	—	VBATT × 0.3		
	Ports 03, 05, 07, ports 40 to 47		ΔV_T	AVCC0 × 0.1	—	—		
	RIIC input pin (except for SMBus)			VCC × 0.05	—	—		
	Ports 12, 13, 16, 17, Port B5			VCC × 0.05	—	—		
	Other than RIIC input pin			VCC × 0.1	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD		V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL (external clock input)			VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (SMBus)			2.1	—	VCC + 0.3		
	MD		V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL (external clock input)			–0.3	—	VCC × 0.2		
	RIIC input pin (SMBus)			–0.3	—	0.8		



Note 1. All peripheral operations except any BGO operation are operating normally. Indicates the average of the typical samples through actual measurement during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. Indicates the average of the upper-limit samples through actual measurement during product evaluation.

Figure 5.3 Voltage Dependency in Low-Speed Operating Mode (Reference Data)

Table 5.16 Permissible Output Currents (1)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +85°C

Item			Symbol	Max.	Unit
Permissible output low current (average value per pin)	Ports 40 to 47, ports 03, 05, 07, port 36, 37		I_{OL}	4.0	mA
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current (maximum value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37			4.0	
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current	Total of ports 40 to 47, ports 03, 05, 07		ΣI_{OL}	40	
	Total of ports 12 to 17, ports 20 to 27, ports 30 to 37, port PJ3			40	
	Total of ports 50 to 55, ports C0 to C7, ports B0 to B7			40	
	Total of ports E0 to E7, ports A0 to A7, ports D0 to D4			40	
	Total of all output pins			80	
Permissible output high current (average value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37		I_{OH}	–4.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current (maximum value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37			–4.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current	Total of ports 40 to 47, ports 03, 05, 07		ΣI_{OH}	–40	
	Total of ports 12 to 17, ports 20 to 27, ports 30 to 37, port PJ3			–40	
	Total of ports 50 to 55, ports C0 to C7, ports B0 to B7			–40	
	Total of ports E0 to E7, ports A0 to A7, ports D0 to D4			–40	
	Total of all output pins			–80	

Note: Do not exceed the permissible total supply current.

Table 5.17 Permissible Output Currents (2)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item			Symbol	Max.	Unit
Permissible output low current (average value per pin)	Ports 40 to 47, ports 03, 05, 07, port 36, 37		I_{OL}	4.0	mA
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current (maximum value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37			4.0	
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current	Total of ports 40 to 47, ports 03, 05, 07		ΣI_{OL}	30	
	Total of ports 12 to 17, ports 20 to 27, ports 30 to 37, port PJ3			30	
	Total of ports 50 to 55, ports C0 to C7, ports B0 to B7			30	
	Total of ports E0 to E7, ports A0 to A7, ports D0 to D4			30	
	Total of all output pins			60	
Permissible output high current (average value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37		I_{OH}	–4.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current (maximum value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37			–4.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current	Total of ports 40 to 47, ports 03, 05, 07		ΣI_{OH}	–30	
	Total of ports 12 to 17, ports 20 to 27, ports 30 to 37, port PJ3			–30	
	Total of ports 50 to 55, ports C0 to C7, ports B0 to B7			–30	
	Total of ports E0 to E7, ports A0 to A7, ports D0 to D4			–30	
	Total of all output pins			–60	

Note: Do not exceed the permissible total supply current.

5.2.3 Normal I/O Pin Output Characteristics (3)

Figure 5.18 to Figure 5.21 show the characteristics of the RIIC output pin.

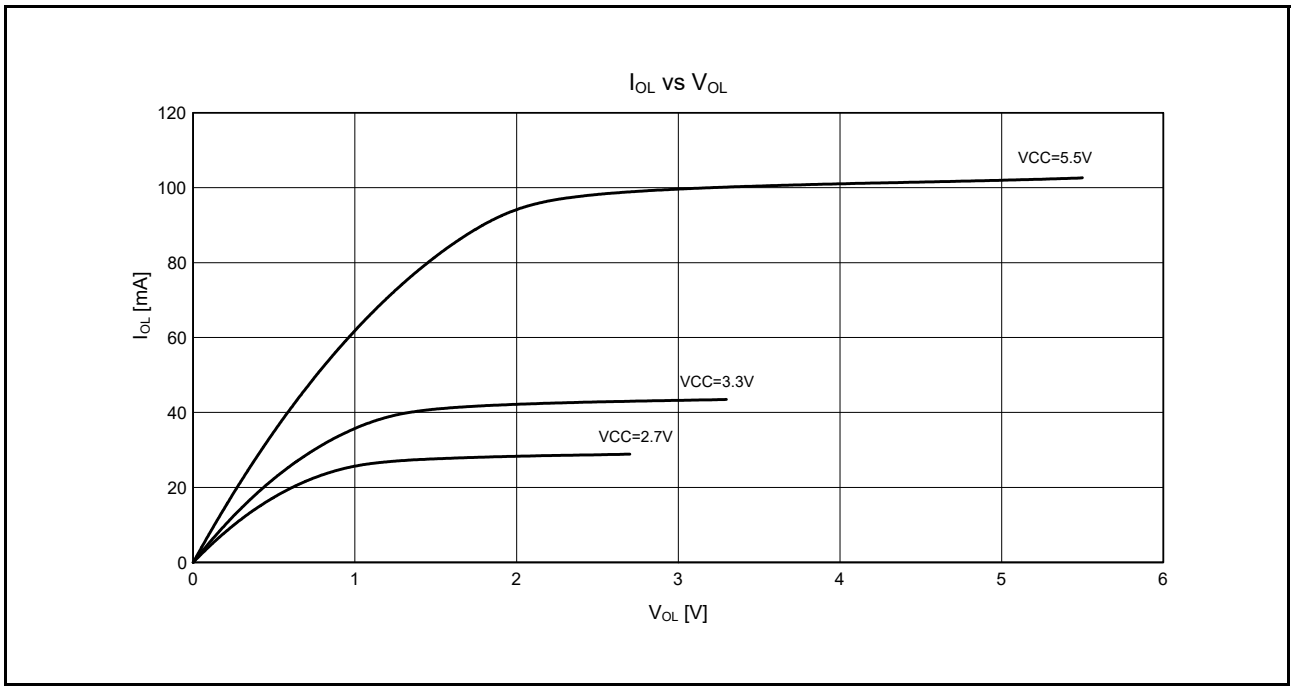


Figure 5.18 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at T_a = 25°C (Reference Data)

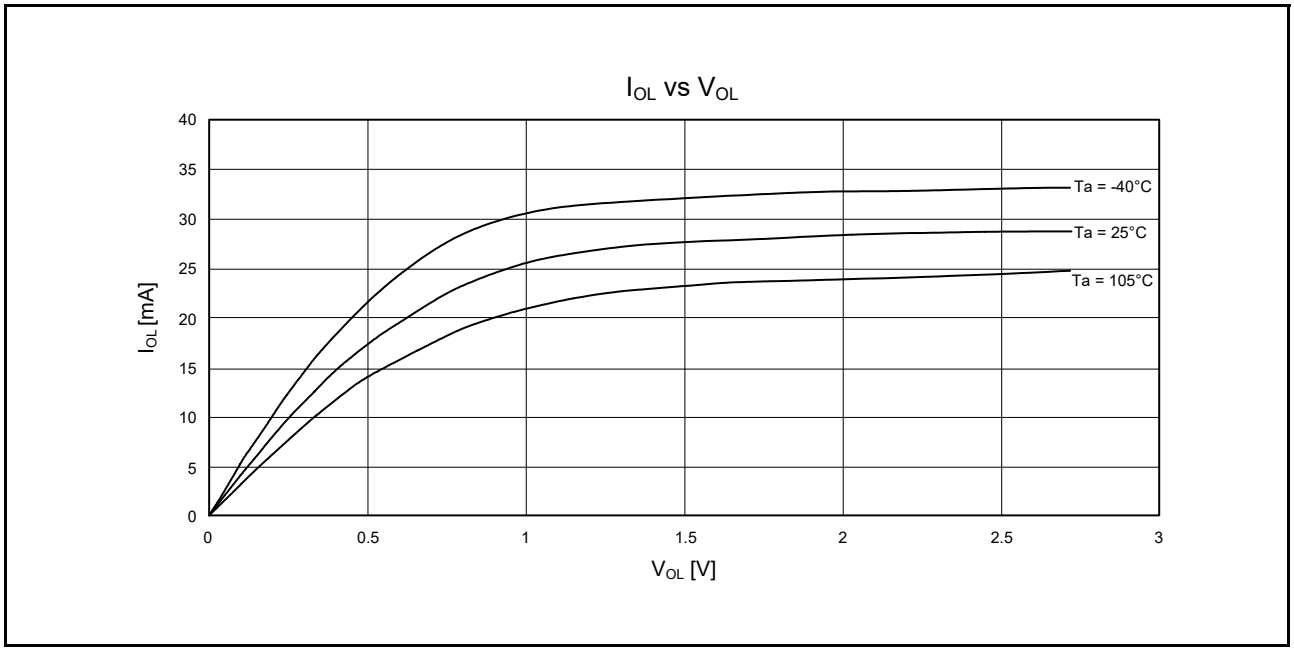


Figure 5.19 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)

Table 5.26 Clock Timing

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{Xcyc}	50	—	—	ns	Figure 5.23
EXTAL external clock input high pulse width		t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{XL}	20	—	—	ns	
EXTAL external clock rise time		t_{Xr}	—	—	5	ns	
EXTAL external clock fall time		t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{XWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency*2	2.4 ≤ VCC ≤ 5.5	f_{MAIN}	1	—	20	MHz	
	1.8 ≤ VCC < 2.4		1	—	8		
Main clock oscillation stabilization time (crystal)*2		$t_{MAINOSC}$	—	3	—	ms	Figure 5.24
Main clock oscillation stabilization time (ceramic resonator)*2		$t_{MAINOSC}$	—	50	—	μs	
LOCO clock oscillation frequency		f_{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation stabilization time		t_{LOCO}	—	—	0.5	μs	Figure 5.25
IWDT-dedicated clock oscillation frequency		f_{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time		t_{ILOCO}	—	—	50	μs	Figure 5.26
HOCO clock oscillation frequency		f_{HOCO} (32 MHz)	31.52	32	32.48	MHz	T_a = –40 to + 85°C
			31.68	32	32.32		T_a = 0 to + 55°C
			31.36	32	32.64		T_a = –40 to +105°C
		f_{HOCO} (54 MHz)	53.19	54	54.81	MHz	T_a = –40 to + 85°C
			53.46	54	54.54		T_a = 0 to + 55°C
			52.92	54	55.08		T_a = –40 to +105°C
HOCO clock oscillation stabilization time		t_{HOCO}	—	—	30	μs	Figure 5.28
PLL input frequency*3		f_{PLLIN}	4	—	12.5	MHz	
PLL circuit oscillation frequency*3		f_{PLL}	24	—	54	MHz	
PLL clock oscillation stabilization time		t_{PLL}	—	—	50	μs	Figure 5.29
PLL free-running oscillation frequency		f_{PLLFR}	—	8	—	MHz	
USBPLL input frequency*5		f_{PLLIN}	—	6, 8*6	—	MHz	
USBPLL circuit oscillation frequency*5		f_{PLL}	—	48*6	—	MHz	
USBPLL clock oscillation stabilization time		t_{PLL}	—	—	50	μs	Figure 5.29
Sub-clock oscillator oscillation frequency*7		f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*4		t_{SUBOSC}	—	0.5	—	s	Figure 5.30

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating).

Note 2. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After the MOSCCR.MOSTP bit is changed to enable the main clock oscillator, confirm that the OSCOVFSR.MOOVF flag has become 1, and then start using the main clock.

Note 3. The VCC range should be 2.4 to 5.5 V when the PLL is used.

Note 4. Reference values when a 32.768-kHz resonator is used.
After the setting of the SOSCCR.SOSTP bit or RCR3.RTCEN bit is changed to operate the sub-clock oscillator, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.

Note 5. The VCC range should be 3.0 to 5.5 V when the USBPLL is used.

Note 6. The input frequency can be set to 6 or 8 MHz and the oscillation frequency can be set to 48 MHz only.

Note 7. Only 32.768 kHz can be used.

5.3.4 Control Signal Timing

Table 5.33 Control Signal Timing

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter is disabled (NMIFLTE.NFLTEN = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		NMI digital filter is enabled (NMIFLTE.NFLTEN = 1)	t_{NMICK} × 3 ≤ 200 ns
		t_{NMICK} × 3.5*2	—	—			t_{NMICK} × 3 > 200 ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter is disabled (IRQFLTE0.FLTENi = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		IRQ digital filter is enabled (IRQFLTE0.FLTENi = 1)	t_{IRQCK} × 3 ≤ 200 ns
		t_{IRQCK} × 3.5*3	—	—			t_{IRQCK} × 3 > 200 ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

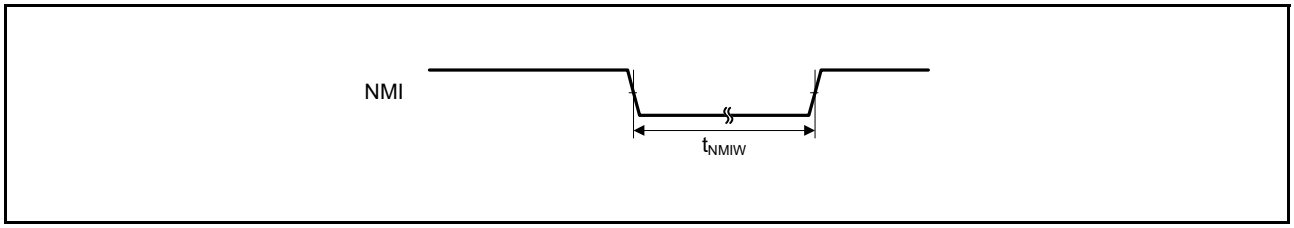


Figure 5.36 NMI Interrupt Input Timing

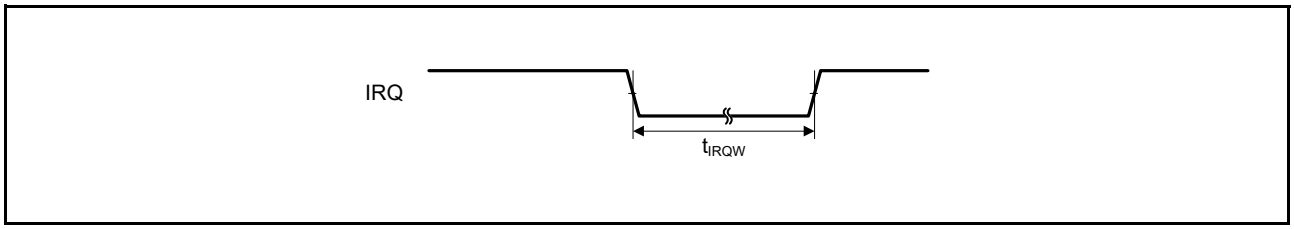


Figure 5.37 IRQ Interrupt Input Timing

5.3.5 Bus Timing

Table 5.34 Bus Timing (1)

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V,
fBCLK ≤ 32 MHz (BCLK pin output frequency ≤ 16 MHz), T_a = –40 to +105°C, V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5,
I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C_L = 30 pF, when normal output is selected by the drive capacity control register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	55	ns	Figure 5.38 to Figure 5.41
Byte control delay time	t_{BCD}	—	55	ns	
CS# delay time	t_{CSD}	—	55	ns	
RD# delay time	t_{RSD}	—	55	ns	
Read data setup time	t_{RDS}	40	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	55	ns	
Write data delay time	t_{WDD}	—	55	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	40	—	ns	Figure 5.42
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.35 Bus Timing (2)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 < 2.7 V, VSS = AVSS0 = VSS_USB = 0 V,
fBCLK ≤ 16 MHz (BCLK pin output frequency ≤ 8 MHz), T_a = –40 to +105°C, V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5,
I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C_L = 30 pF, when normal output is selected by the drive capacity control register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	90	ns	Figure 5.38 to Figure 5.41
Byte control delay time	t_{BCD}	—	90	ns	
CS# delay time	t_{CSD}	—	90	ns	
RD# delay time	t_{RSD}	—	90	ns	
Read data setup time	t_{RDS}	60	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	90	ns	
Write data delay time	t_{WDD}	—	90	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	60	—	ns	Figure 5.42
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.36 Bus Timing (Multiplex bus) (1)

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V,
fBCLK ≤ 32 MHz (BCLK pin output frequency ≤ 16 MHz), T_a = –40 to +105°C, V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5,
I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C_L = 30 pF, when normal output is selected by the drive capacity control register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	55	ns	Figure 5.43, Figure 5.44
Byte control delay time	t_{BCD}	—	55	ns	
CS# delay time	t_{CSD}	—	55	ns	
RD# delay time	t_{RSD}	—	55	ns	
ALE delay time	t_{ALED}	—	55	ns	
Read data setup time	t_{RDS}	40	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	55	ns	
Write data delay time	t_{WDD}	—	55	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	40	—	ns	Figure 5.42
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.37 Bus Timing (Multiplex bus) (2)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 < 5.5 V, VSS = AVSS0 = VSS_USB = 0 V,
fBCLK ≤ 16 MHz (BCLK pin output frequency ≤ 8 MHz), T_a = –40 to +105°C, V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5,
I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C_L = 30 pF, when normal output is selected by the drive capacity control register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	90	ns	Figure 5.43, Figure 5.44
Byte control delay time	t_{BCD}	—	90	ns	
CS# delay time	t_{CSD}	—	90	ns	
RD# delay time	t_{RSD}	—	90	ns	
ALE delay time	t_{ALED}	—	90	ns	
Read data setup time	t_{RDS}	60	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	90	ns	
Write data delay time	t_{WDD}	—	90	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	60	—	ns	Figure 5.42
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.39 Timing of On-Chip Peripheral Modules (2)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C, C = 30 pF, when high-drive output is selected by the drive capacity control register

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}*1	Figure 5.54
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	2.7 V or above	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	1	µs	
	Data input setup time	Master	2.7 V or above	t_{SU}	10	—	ns	Figure 5.55 to Figure 5.58
			1.8 V or above		30	—		
		Slave			$25 - t_{Pcyc}$	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	$-30 + N^{*2} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	$-30 + N^{*3} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V or above	t_{OD}	—	14	ns	
			1.8 V or above		—	30		
		Slave	2.7 V or above		—	$3 \times t_{Pcyc} + 65$		
			1.8 V or above		—	$3 \times t_{Pcyc} + 105$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	2.7 V or above	t_{Dr}, t_{Df}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	1	µs	
	SSL rise/fall time	Output	2.7 V or above	t_{SSLr}, t_{SSLf}	—	10	ns	
			1.8 V or above		—	15	ns	
		Input			—	1	µs	
	Slave access time		2.7 V or above	t_{SA}	—	6	t_{Pcyc}	Figure 5.57, Figure 5.58
			1.8 V or above		—	7		
	Slave output release time		2.7 V or above	t_{REL}	—	5	t_{Pcyc}	
			1.8 V or above		—	6		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

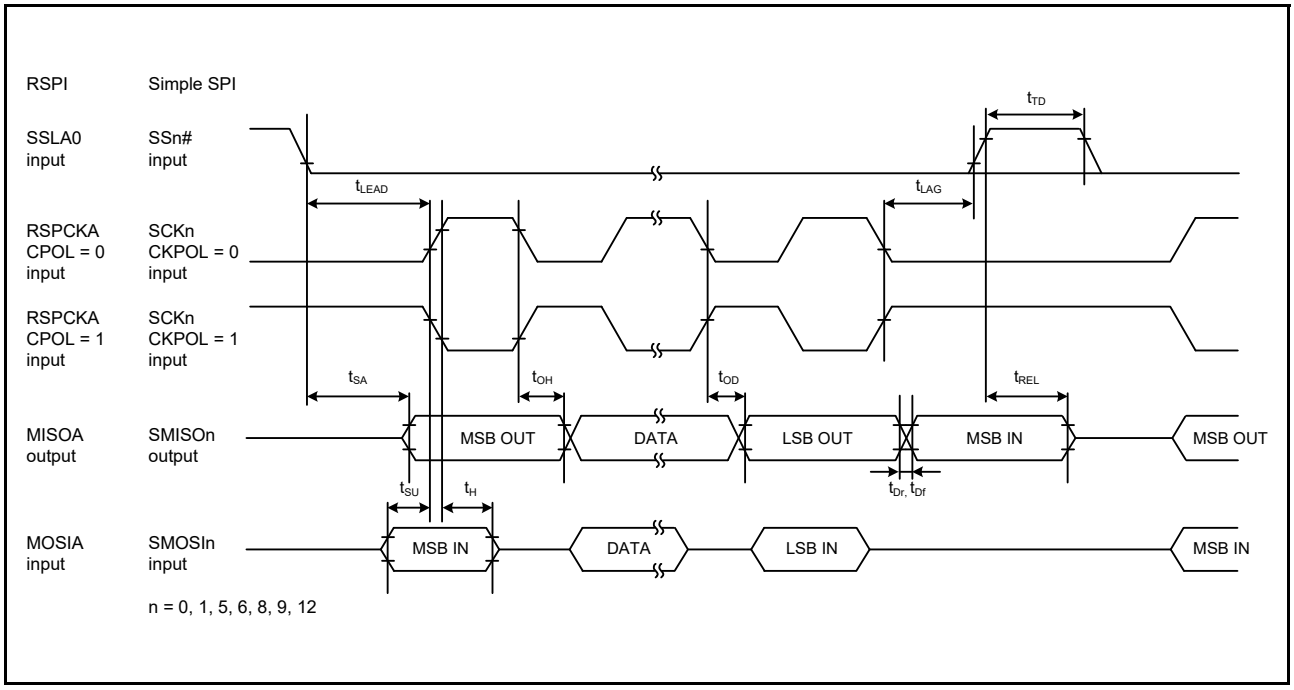


Figure 5.57 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

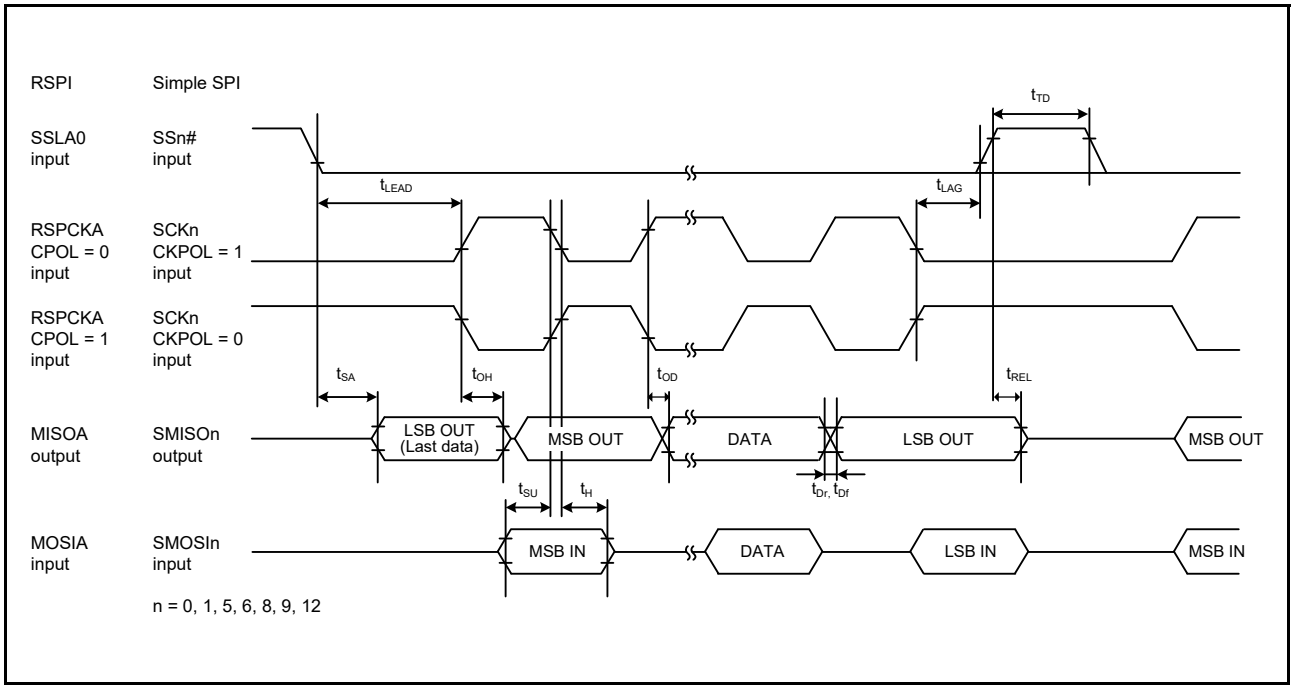


Figure 5.58 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)

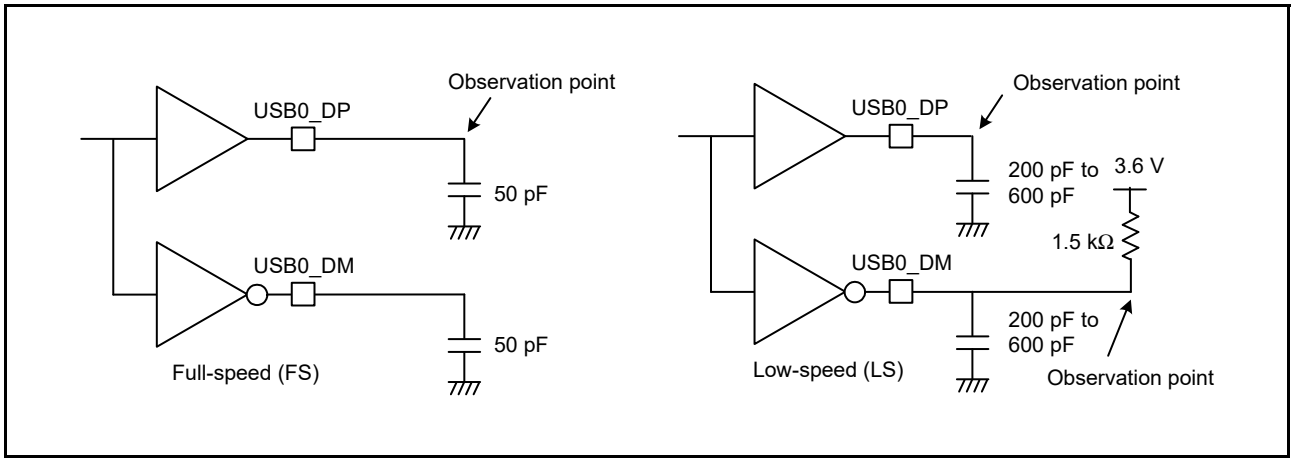


Figure 5.66 Test Circuit

5.11 Oscillation Stop Detection Timing

Table 5.60 Oscillation Stop Detection Timing

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.78

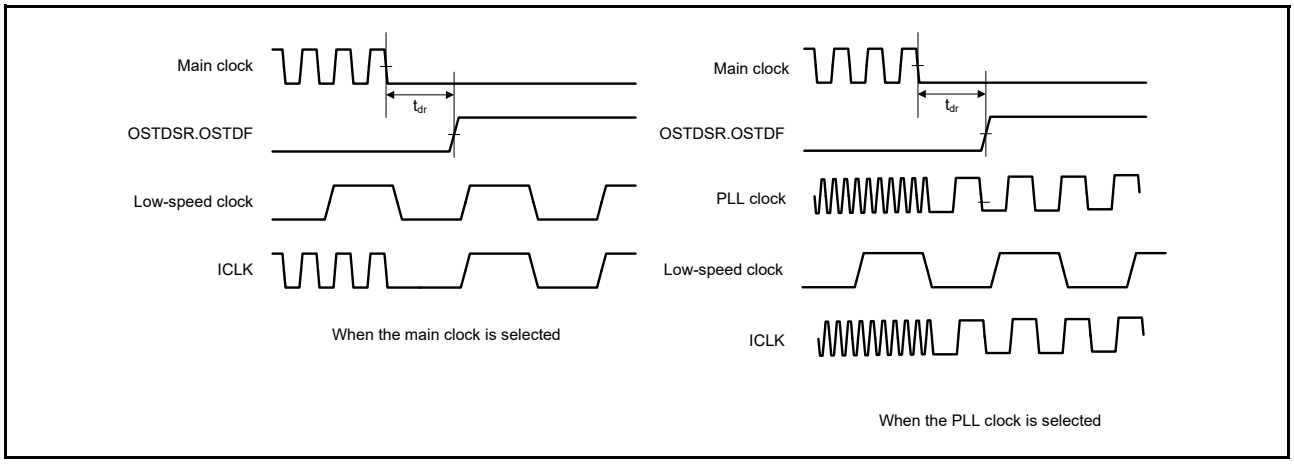
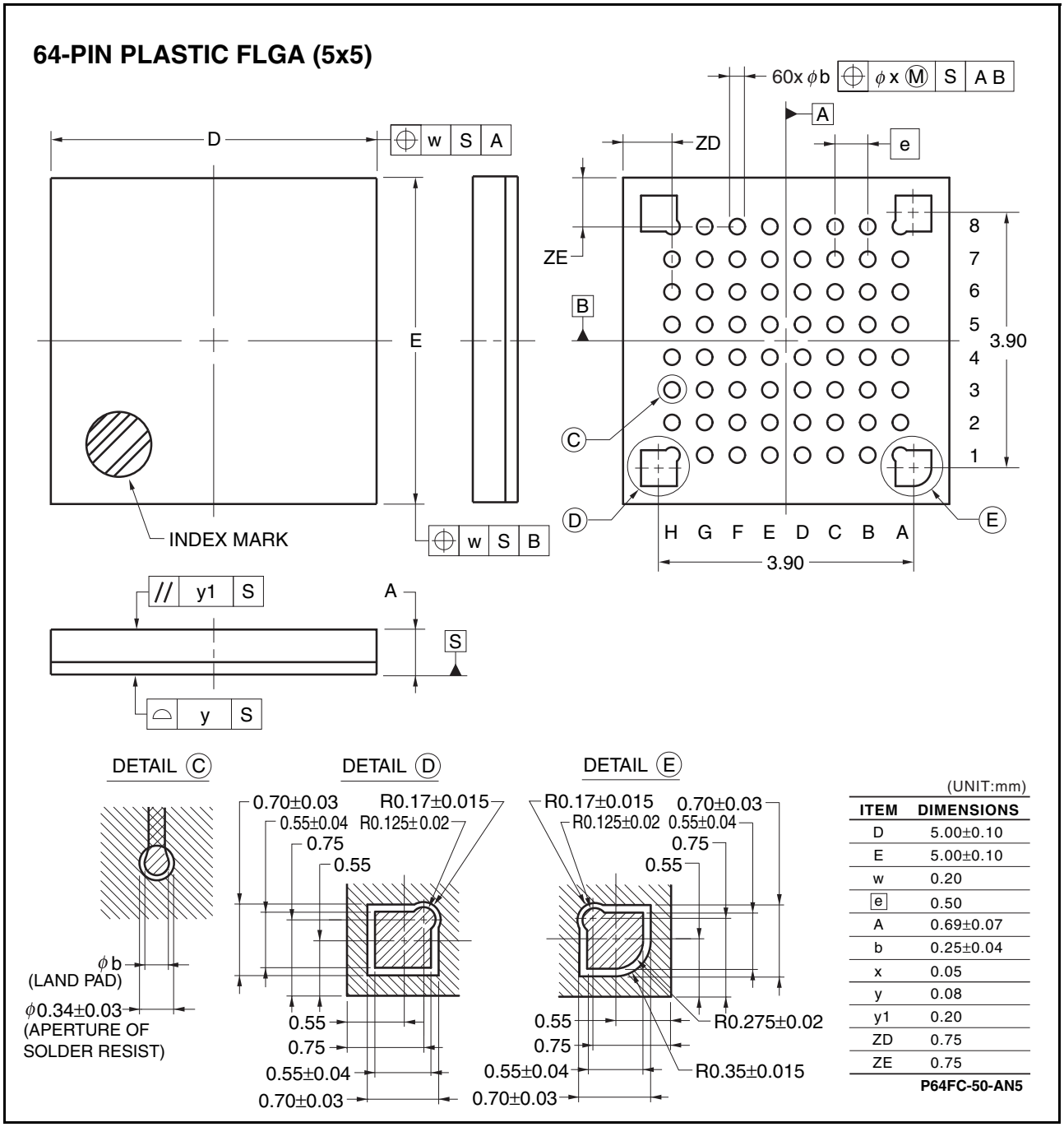


Figure 5.78 Oscillation Stop Detection Timing



(UNIT:mm)

ITEM	DIMENSIONS
D	5.00±0.10
E	5.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.25±0.04
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

P64FC-50-AN5

Figure C 64 -Pin WFLGA (PWLG0064KA-A)

Rev.	Date	Description		Classification
		Page	Summary	
1.20	Sep 28, 2018	95	Figure 5.12 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 5.5 V When Normal Output is Selected (Reference Data), changed	TN-RX*-A201A/E
		124	Table 5.44 Timing of On-Chip Peripheral Modules (7), added	TN-RX*-A197A/E
		131	Figure 5.64 SD Host Interface Input/Output Signal Timing, added	TN-RX*-A197A/E
		132	Table 5.45 USB Characteristics (USB0_DP and USB0_DM Pin Characteristics) conditions, changed	